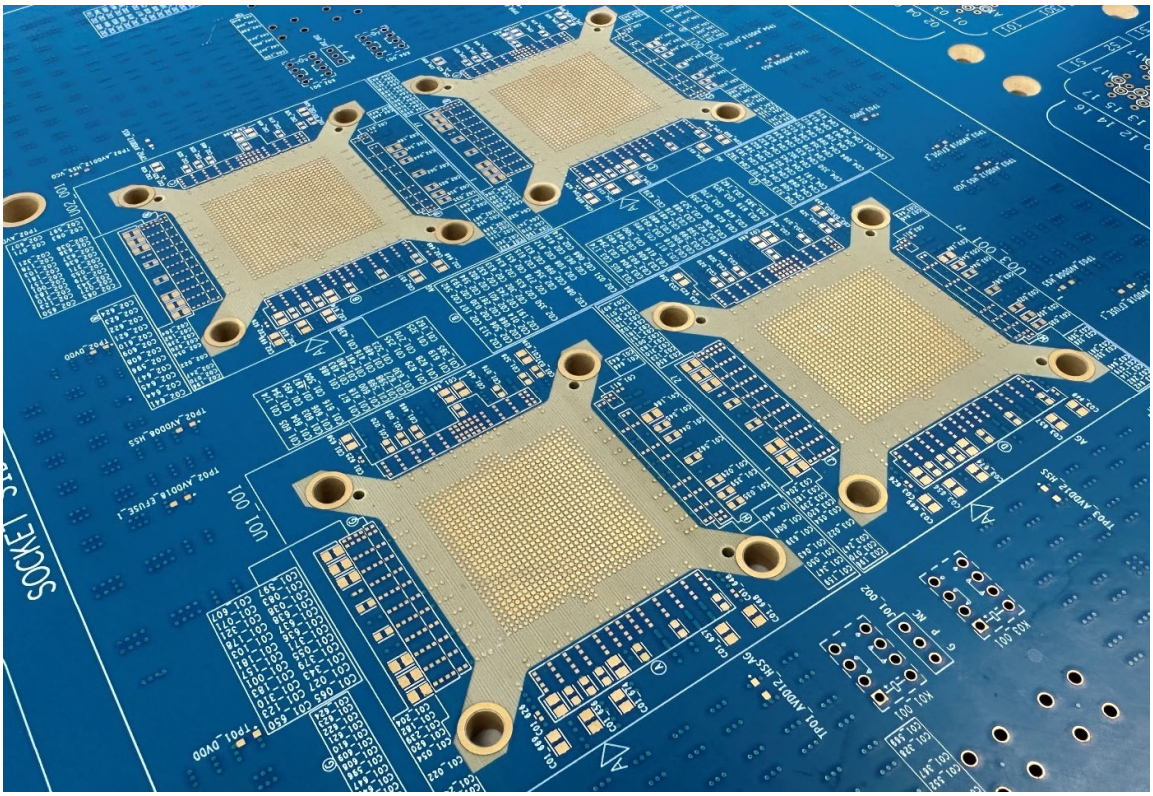
Sunshine Global Circuits
PCB Design Guidelines



Sunshine Global Circuits, Engineering Dept.

February 2024

PCB Design Guidelines

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1. Introduction

This document is intended to help the board designer to better understand the process capabilities and offerings of Sunshine for rigid printed circuit boards. We strongly believe early design involvement is mutually beneficial and will help improve manufacturability, reduce cycle time, and lower overall cost. By following these guidelines, the PCB designer will be able to avoid potential issues and unnecessary delays during the Design and DFM/EQ process.

We appreciate you taking the time to read and apply this document. As always, please feel free to contact Sunshine Field Application Engineering or Sales Rep if any questions.

2. Incoming Data Requirements

Below are the preferred data formats and required documentation when issuing orders to Sunshine.

2.1 Data and Documentation Formats

Accepted Image Data Formats	
Data formats	Gerber RS274-X ODB++ (Valor Backup) Gerber 274-D – Must include aperture table IPC-2581 Rev B
Data Type	ASCII
Units	Imperial or Metric

Aperture Information	
Formats	Columnated ASCII Legible Document
Units	Imperial or Metric

NC Drill Data	
Formats	Excellon II Plot Data Format
Data Type	ASCII
Units	Imperial or Metric

Fabrication Drawings

Formats	Autocad DWG or DXF.*, .dwg,*, .dxf Portable Data Format: *.pdf Raster File: *.mil, *.tif, *.gif

Readme Document and/or Special Instructions	
Formats	ASCII Text File Embedded within Aperture Information Legible Document

Net List Data	
Formats	IPC-D-356A
Units	Imperial or Metric

3. Base Materials

3.1 Copper Foil

Cu Foil Type	Full Name	Available Thickness (oz)	Prepreg Side Roughness, Rz for H oz (um)	Core Side Roughness, Rz for Hoz (um)
HTE	High Temperature Elongation	1/3, 1/2, 1.0, 2.0, 3.0, 4.0, 5.0	< 2.5	< 8.5
RTF	Reverse Treated Foil	1/3, 1/2, 1.0	< 6.0	< 3.5
VLP	Very Low Profile	1/3, 1/2, 1	< 2.0	< 3.0
HVLP	Hyper Very Low-Profile	1/3, 1/2, 1	< 2.0	< 2.0
HVLP2	Hyper Very Low-Profile 2	1/3, 1/2, 1	< 1.5	< 1.5

Standard electrodeposited HTE copper foil works for most applications. It has the smooth drum side facing up and the rough plated side facing the core providing high peel strength. RTF® has the rough plated side facing up and the drum side (with treatment) facing the core.

As signal speeds increased and skin effect became better understood, copper foil vendors came out with foils with increasingly smoother surfaces. This helps to lower signal losses due to skin effect but the trade-off is lower peel strength. Sunshine recommends the use of RTF or VLP foil for mid-loss applications (5-25 Gbps) and HVLP for low-loss applications (>50 Gbps). Most low loss materials (see next page) will come with VLP or HVLP foils as standard.

For thickness of copper layers after processing, please reference IPC-6012 Table 3-13 for internal layers and Table 3-14 for external layers. Please note copper thickness is not .0014” for 1 oz due to processing, and all plated layers will see an increase in copper thickness due to the plating.

3.2 Recommended Base Materials

Type and Df Range	Supplier	Product	Tg	Dk	Df	Preferred	UL	Lam Cycles	Layer Count
MidTg FR4	ShengYi	S1000-H	160	4.6	0.011	✓	Y	2	<16L
	EMC	EM-370(5)	155	4.3	0.013	✓	Y	4	16-32
HiTg FR4 Std Loss .019-.025	ShengYi	S1000-2M	180	4.3	0.020	✓	Y	4	>32L
	EMC	EM-827	180	4.3	0.019	✓	Y	4	16-32
	Isola	185HR	180	3.88	0.024		Y	4	16-32
		370HR	180	3.92	0.025	✓	Y	6	>32
Mid Loss .010-.015	EMC	EM-370(D), EM-370(Z)	180	4.1	0.015	✓	Y	4	16-32
		EM-828(G)	170	3.8	0.011		Y	2	16-32
		EM-390	165	3.4	0.009	✓	Y	7	16-32
	Isola	FR408	180	3.65	0.013	✓	Y	2	16-32
	TUC	TU-862HF	200	4.4	0.015		Y	2	16-32
		TU-862T	190	4.4	0.015		Y	5	16-32
		TU-865	200	4.4	0.014	✓	Y	5	>36
Low Loss .006-.010	Panasonic	R-5725 Megtron 4	176	3.8	0.008		Y	6	16-32
	EMC	EM-888, EM-888(S)	170	3.7	0.007		Y	2	16-32
		EM-526	230	3.9	0.007	✓	Y	4	16-32
		EM-528	220	3.9	0.006	✓	Y	4	16-32
	Isola	FR408HR	190	3.65	0.010	✓	Y	4	16-32
		I-Speed	180	3.63	0.007	✓	Y	4	16-32
	TUC	TU-863+ ThunderClad 1+	180	4.0	0.008		Y	5	16-32
Very Low Loss .004-.006	Panasonic	R-5775 Megtron 6	185	3.4	0.004	✓	Y	10	>32
	EMC	EM-888K	170	3.2	0.006		Y	2	16-32
		EM-891	170	3.6	0.005	✓	Y	4	16-32
		EM-528K	220	3.4	0.004	✓	Y	4	16-32
	Isola	I-Tera MT40	200	3.75	0.004	✓	Y	8	>32
	TUC	TU-883 Thunderclad 2	180	3.6	0.005		Y	5	16-32
Ultra Low Loss <.004	Panasonic	R-5785 Megtron 7	200	3.4	0.002	✓	Y	10	44
	EMC	EM-891K	170	3.1	0.003	✓	Y	4	>32
	Isola	Tachyon 100G	200	3.0	0.002	✓	Y	8	>32
	TUC	TU-883SP Thunderclad 2SP	170	3.22	0.003		Y	5	16-32
		TU-933 Thunderclad 3)	170	3.4	0.003		Y	5	>32
		TU-933+ Thunderclad 3+	170	3.16	0.002		Y	5	>32
Extreme Low Loss <.002	Panasonic	R-5795 Megtron 8U	220	3.08	.0012		IP	5	>32
	EMC	EM-892K	215	3.0	.0015		IP	5	>32
	TUC	TU-943SN Thunderclad 4SN	225	3.16	.0014		IP	5	>32
	ITEQ	IT-998GSE	TBD	TBD	TBD		IP	5	>32

Sunshine also offers High Frequency Laminates including : Rogers 3000/4000, Arlon, Taconic, and Neltec.

Notes for Materials Table:

1. UL "Yes" above means Sunshine has UL certification for this material. “IP” means application is in process.
2. Layer count stated is maximum layer count recommended from SGC Engineering or supplier.
3. Preferred materials are selected based on availability, cost, and performance.
4. Material leadtimes depends on the market conditions, limited quantities may be in Sunshine stock.
5. Dk & Df values are by cavity resonator or Bereskin Stripline methods, 50-70% RC, 1G to 10G.
6. Tg are in deg. C, are approximate, and may come from different test methods: DSC, TMA, DMA.

4. Engineering Services

Sunshine offers engineering services from early design phases through product end-of-life. Sunshine's goal is to be involved with our customers and PCB designers during early product development so that we may help minimize the number of design iterations and thus minimize time to market. These services include Field Application Engineering, In-House Application Engineering, Planning Engineers, and Product Engineers.

Field Application Engineers and In-House Applications Engineers assist customers with interpretation of capabilities and how processes and methods may be adapted to meet the needs of specific products. This includes the selection of the most cost-effective material to meet the demands of the design and application. Sunshine engineers provide stack-up and impedance modeling from initial design phase through final layout, with detailed info including dielectric thickness, retained copper percentage after etch, and line widths for specified impedance values (see Section 8.3).

Sunshine's Planning Engineers conduct design rule checks (DRC's) on all incoming Gerber data files as an early check for compatibility with standard manufacturing capabilities. When netlists are provided by our customers, Sunshine's CAM Engineers compare the netlist with the Gerber extracted netlist to insure the PWB we build electrically matches your design. In addition, CAM and Planning Engineering are on-duty 24 hours/day, Monday through Saturday, to assist with "time critical" data issues.

If your design requirements need advanced capabilities or if multiple design parameters push process limits, our design for manufacturability (DFM) evaluation services are also available. Please contact your sales person or account manager if you require any of the following:

- Material selection recommendations
- DFM report
- Stackup Diagram (see Section 8.3 of this document)
- Impedance Simulation
- Panelization recommendation or drawing
- Design for Cost recommendations

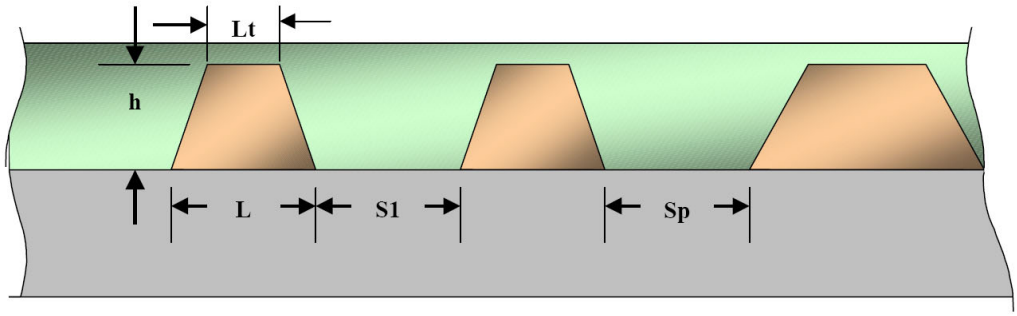
Also see the end of this document for contact information for Sunshine Application Engineering.

5. PWB Design Guidelines

The following guidelines are provided with “Standard” and “Advanced” options. Items in the Standard column are current capabilities and can move easily into volume production. Items in the Advanced column are within our capability but may require additional engineering oversight and may impact production capacity, lead-time, and cost. We are constantly striving to improve our manufacturing capabilities. If you have questions regarding these guidelines, please reach out to our Application Engineers or Sales Rep and we will work with you to develop a solution.

All dimensions are in inches unless otherwise noted.

5.1 Outer Layer



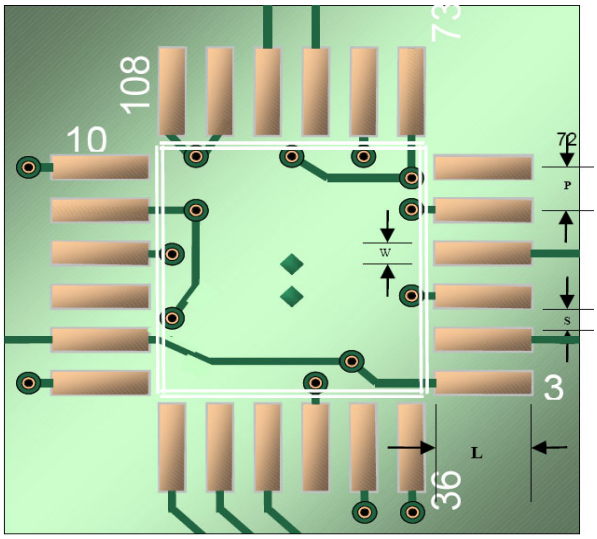
Line Width and Spacing (based on H oz starting copper foil)

Item	Parameter
L	Minimum Line Width
S1	Minimum Space (line to line)
Sp	Minimum Space (isolated line array)
h	Height of Trace

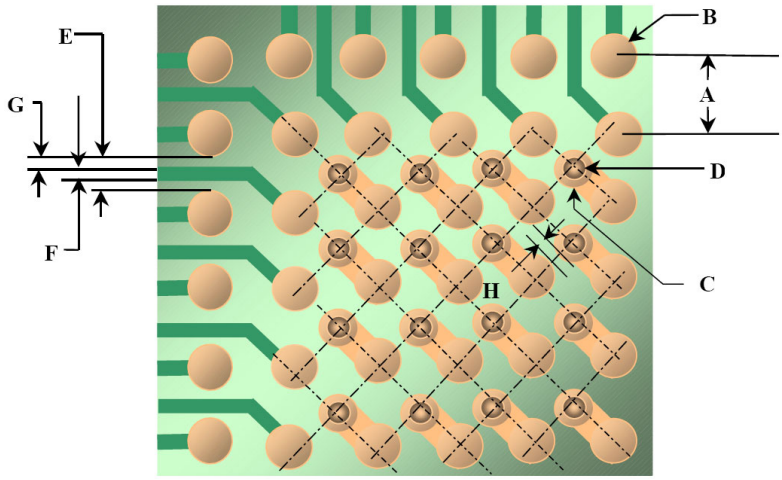
Outer Layer Line Width and Spacing (based on base copper thickness)

Base Copper	Minimum Requirement at Design	Standard	Advanced
0.33oz	Line Width/Spacing	0.003”/0.0035”	0.0025”/0.0025”
0.5oz	Line Width/Spacing	0.0035”/0.004”	0.0035”/0.0035”
1.0oz	Line Width/Spacing	0.004”/0.0045”	0.0035”/0.004”
2.0oz	Line Width/Spacing	0.007”/0.007”	0.0065”/0.0065”
3.0oz	Line Width/Spacing	0.009”/0.009”	0.0085”/0.0085”
4.0oz	Line Width/Spacing	0.011”/0.011”	0.0105”/0.0105”
5.0oz	Line Width/Spacing	0.012”/0.012”	0.0115”/0.0115”

In-Line & Quad Flat Packs (QFP's)



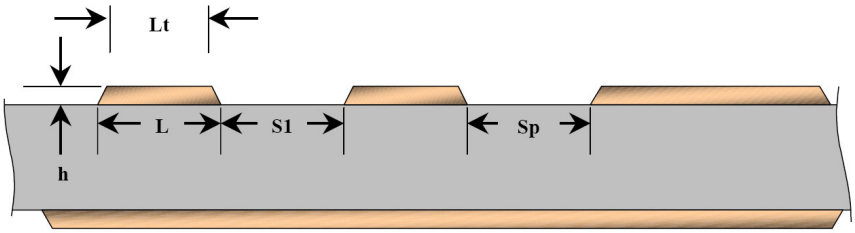
Item	Parameter	Standard	Advanced
P	Minimum Pitch (Center to Center)	0.016"	0.010"
S	Minimum Space (pad to pad)	0.007"	0.005"
W	Minimum Pad Width	0.008"	0.005"
L	Minimum Pad Length	0.016"	0.010"



Item	Parameter	Standard	Advanced
A	Pitch (Center to Center)	0.0315"	0.0197"
B	Solder Pad Dia	0.010"	0.008"
C	Drill Land Dia	0.014"	0.0098"
D	PTH Drill Dia	0.006"	0.005"
E	Space (Solder Pad to Solder Pad)	0.0094"	0.0079"
F	O/L Line Width (1 Line/channel)	0.003"	0.0025"
G	Space (Solder Pad to Line)	0.0032"	0.0026"
H	Space (Drill Land to Solder Pad)	0.0042"	0.0031"

The diagram above is for reference, and may be adjusted to customer's design.

5.2 Inner Layer



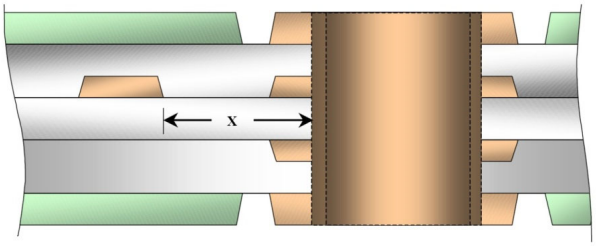
Line Width and Space (based on H oz. copper foil)

Item	Parameter
L	Minimum Line Width
Sl	Minimum Space (line to line)
Sp	Minimum Space (line to via land)
h	Height of Trace

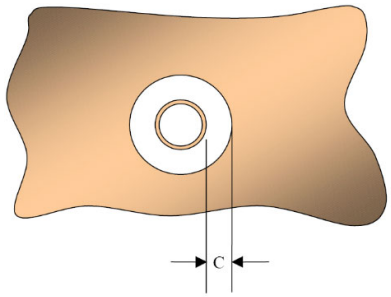
Inner Layer Line Width and Spacing (based on copper foil thickness)

Copper Foil	Minimum Requirement at Design	Standard	Advanced
0.5oz	Line Width/Spacing	.003”/.003”	.0025”/00025”
1.0oz	Line Width/Spacing	0.0035”/0.0035”	0.003”/0.003”
2.0oz	Line Width/Spacing	0.006”/0.006”	0.0055”/0.0055”
3.0oz	Line Width/Spacing	0.008”/0.008”	0.0075”/0.0075”
4.0oz	Line Width/Spacing	0.010”/0.010”	0.095”/0.095”
5.0oz	Line Width/Spacing	0.012”/0.012”	0.0115”/0.0115”
6.0oz	Line Width/Spacing	0.013”/0.013”	0.0125”/0.0125”

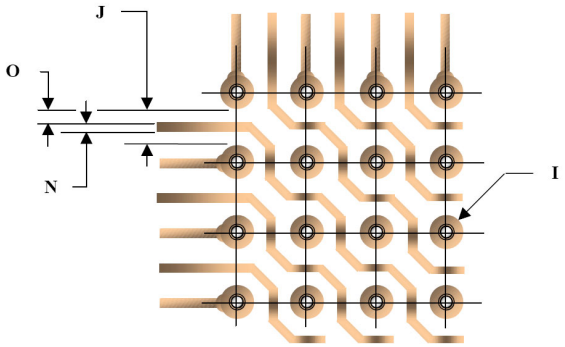
Plated Drill to Copper



Item	Parameter	Standard	Advanced
X	Drill PTH to Copper Feature	0.008"	0.006"

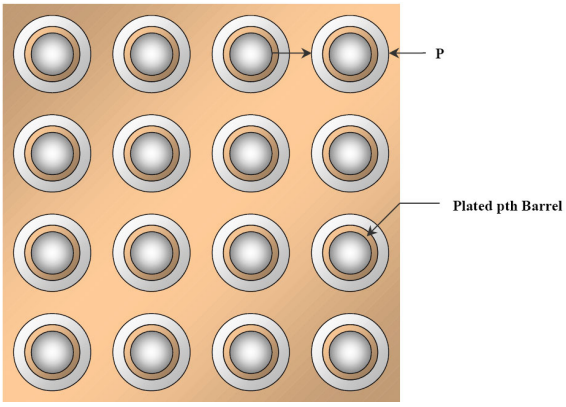


Item	Parameter	Standard	Advanced
C	Drilled PTH to Plane	0.008"	0.006"



Item	Parameter	Standard	Advanced
I	I/L Land Diameter	0.0167"	0.0118"
J	I/L Space (Land to Land)	0.0148"	0.0079"
N	I/L Line Width (1 lines/channel)	0.0049"	0.0026"
O	I/L Space (Pad to Line)	0.0049"	0.0025"

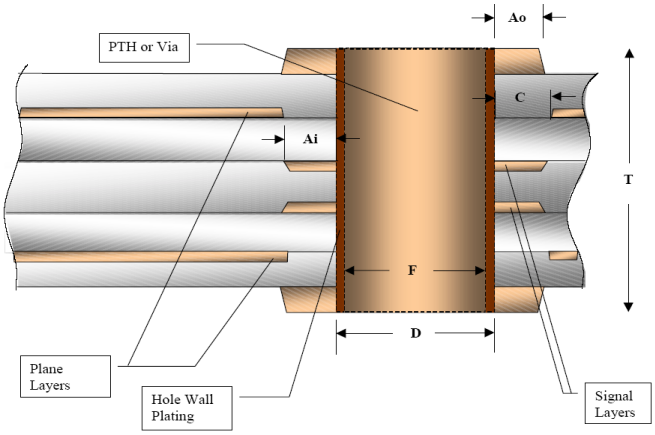
The diagram above is for reference, and it can be adjusted to customer's design.



Item	Parameter	Standard
P	Plane Clearance (Antipad)	0.004"

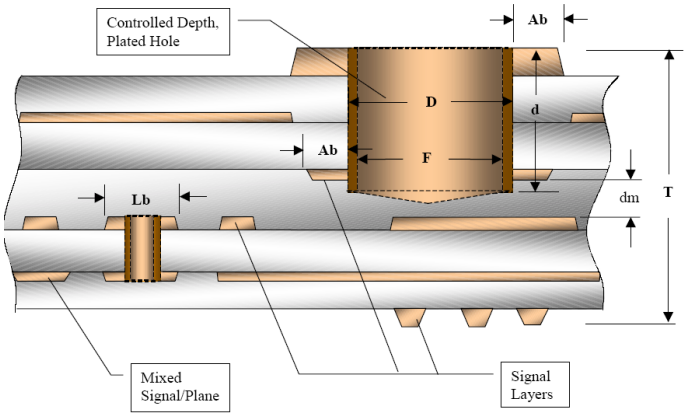
5.3 Drilling

Mechanical Drill



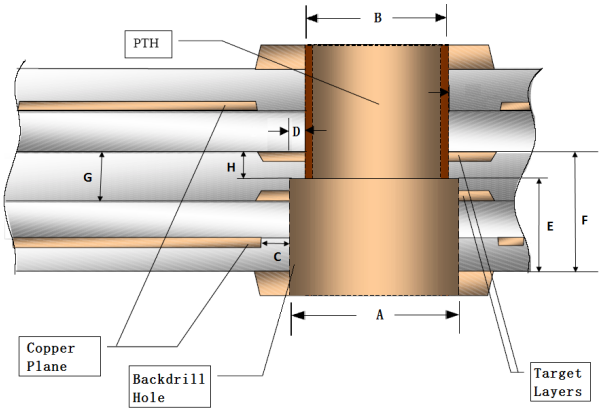
Item	Parameter	Standard	Advanced
D	Minimum Drilled Hole Diameter	0.008"	0.005"
	Maximum Drilled Hole Diameter	0.256"	0.256"
F	Minimum Finished Hole Diameter	0.006"	0.004"
Ao	Minimum Outer Layer Annular Ring	0.004"	0.003"
	O/L Land = Drill +2(Ao)	0.016"	0.011"
Ai	Minimum Inner Layer Annular Ring	0.005"	0.004"
	I/L Land = Drill+2(Ai)	0.02"	0.016"
C	Clearance (Drill to Plane)	0.008"	0.006"
	Minimum Antipad = Dill+2C	0.024"	0.020"
AR*	Maximum Aspect Ratio = T/D	10:1	20:1

Mechanical Blind Vias (Controlled Depth) and Buried Vias



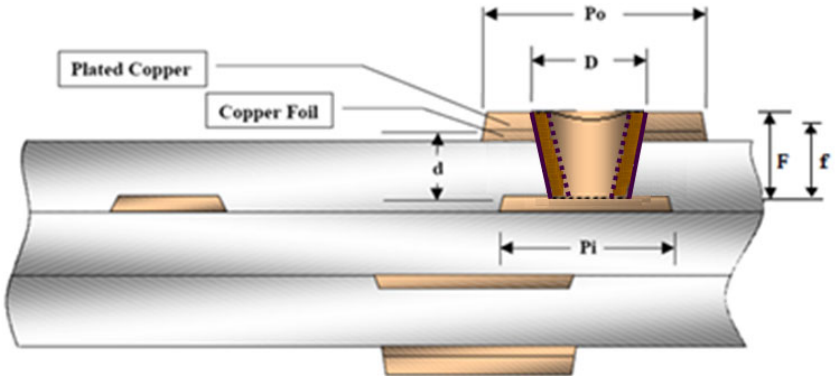
Item	Parameter	Standard	Advanced
T	Board Thickness (min/max)	0.020/0.240"	0.010/0.320"
D	Minimum Drilled Hole Diameter	0.010"	0.006"
F	Minimum Finished Hole Diameter	0.008"	0.004"
d	Dielectric Thickness	0.008"	0.005"
dm	Controlled Depth Margin (min.)	0.005"	0.003"
AR	Blind AR = d/D (max)	0.8:1	1:1
Ab	Minimum Blind/Buried Annular Ring	0.005"	0.004"
Lb	Minimum Blind/Buried Land	0.020"	0.014"

Back Drilling



Item	Parameter	Standard
A	Back Drill	0.008" over primary
B	Primary Drill	0.004" over finished size callout
C	Copper to Back Drill	0.006"
D	Stub Length Range	0.002” - 0.010”
E	Back Drill Depth	Design dependent
F	Signal Layer	Design dependent
G	Target Dielectric	0.008" preferred, 0.006" minimum
H	Stub Length	Typical 0.006" to 0.010"

Laser Drilled Micro-Vias



Item	Parameter	Standard	Advanced
D	Laser Drill Diameter	0.004"	0.003"
F	Plating filled percentage f/F x100%	90%	100%
Po	Minimum Outer Layer Pad Diameter	D+0.006"	D+0.004"
	Minimum O/L Annular Ring	0.003"	0.002"
Pi	Minimum Capture Pad Diameter	D+0.006"	D+0.004"
	Minimum I/L Annular Ring	0.002"	0.001"
C	Drill to Plane Clearance	0.008"	0.006"
	Minimum Antipad = Drill+2C	0.018"	0.015"
d	Drill Depth	.003”	.004”
AR*	Maximum Aspect Ratio = d/D	0.8:1	1:1
	Surface Base Copper	1/3 oz	1/2 oz
	Inner Layer Copper Foil	1/2 oz	1/2 oz

5.4 Solder Mask

Sunshine offers various types of solder mask based on customer requirements. If any other specific solder mask is required, please contact us.

Ink Type	Colors	Isolation Voltage	Halogen free	Suppliers
Solder Mask	**Green / Matte Green** **Semi-matte Green / Semi-bright Green** **Blue / Matte Blue** **Red / Matte Red** **Black / Matte Black** **White / Matte White**	≥500VDC/mil	**Y / N**	ABQ/ANRANSENG/Coates/ Fujita/GREENCURE/ HUNTSMAN /Kuangchun/LANBANG/Nanya /RONGDA/SUNCHEMICAL /TAIYO/TAMURA /YANMO
		≥1000VDC/mil	**Y / N**	
		≥1900VDC/mil	**Y / N**	
		≥3000VDC/mil	**N**	

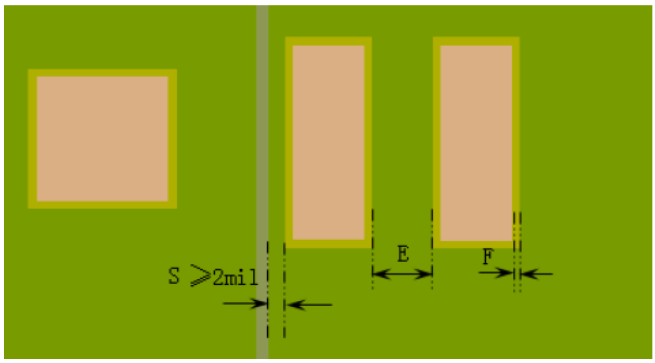
Minimum Solder Mask Bridge (Web) and Opening Around Pads

Base copper	Soldermask Color	Opening F	Solder Bridge E	Minimum Pad to Pad Spacing at Design
0.33 to 1.0 oz	Green	0.0015"	0.003"	.006”
	Blue	0.0015"	0.003"	.0065”
	Red	0.0015"	0.004"	.0065”
	White	0.0015"	0.004"	.007”
	Black	0.0015"	0.004"	.007”
	Others	0.0015"	0.004"	.0065”
2oz or higher	Green	0.002"	0.003"	Add 0.0015” spacing at design per each 1 ounce increase in the base copper thickness.
	Blue	0.002"	0.003"	
	Red	0.002"	0.004"	
	White	0.002"	0.004"	
	Black	0.002"	0.004"	
	Others	0.002"	0.004"	

Soldermask registration by using standard imaging is ±0.003”.

Soldermask registration by direct imaging (LDI) is ±0.001”.

Solder bridges between golden fingers are not suggested. If required, then F ⩾0.004".

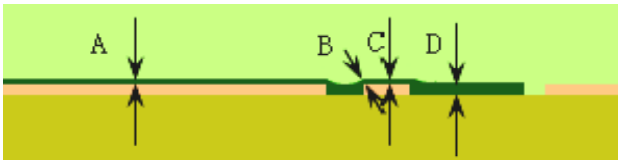


Space between feature covered by ink to opening S

Standard trace and pad S = 0.003" minimum, and preference is for S to be as large as the design will allow.
For immersion gold or solder immersion pad, S = 0.004" minimum.
For non-standard requests, please consult our engineers.

Solder Mask Thickness

Minimum soldermask thickness depends on copper thickness and where it is measured.



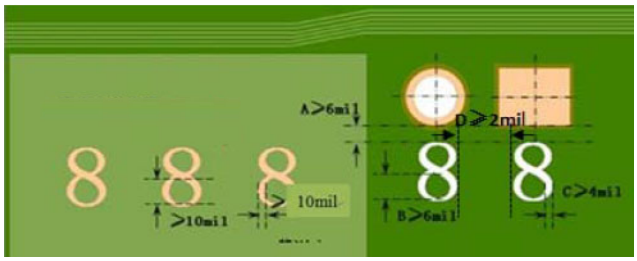
Copper Thickness (Outerlayer)	Over Ground A	At Trace Corner B	On Top of Trace C	Over Base material D
H oz	15-35um	10-35um	10-35um	15-35um
1 oz	15-35um	10-35um	8-35um	15-35um
1.5-2 oz	15-35um	10-35um	5-35um	15-35um
2.0-2.5 oz	15-50um	10-35um	8-35um	30-70um
3.0-3.5 oz	30-70um	10-50um	15-60um	30-100um
4 oz or above	30-70um	10-50um	15-60um	30-150um

5.5 Silkscreen and Carbon Ink

Sunshine offers several silkscreen inks and colors. Our process uses primarily inkjet printing for legend but silkscreen or screenprint is also used in some cases.

Color	Supplier	Ink type	Range of Application	Note
Green	ANRANSHENG	AT-600G03	Plug Via + thermal cure after surface treatment	Thermal cure
White	TAIYO	IJR-4000 MW300	Standard lettering on Rigid PCB's	
White	TAIYO	S-200W N30/HD-3	Standard lettering on Rigid PCB's	
White	TAIYO	S-411W/HD-C	Standard lettering on Rigid PCB's	Halogen free
Yellow	TAIYO	S-200Y ND/HD-3	Standard lettering on Rigid PCB's	
Black	TAIYO	S-200E/HD-3	Standard lettering on Rigid PCB's	
Red	ANRANSHENG	ATA-5000R05/AT-600H	Standard lettering on Rigid PCB's	

Below are standard and minimum characters size and spacing.



Please note lettering on ground areas by developed image of soldermask require larger width and spacing than lettering printed with white ink.

Item	Finished Copper Thickness	Letter Capability	
		Inkjet printing	Silkscreen printing
Minimum letter line width (C)	≤70um	3.5 mils	4 mils
	71-140um	4 mils	6 mils
	>140um	4 mils	10 mils
Scale of Letter high/line width	/	Line width ≥ 4 mil ≥ 8:1 Line width < 4 mil ≥ 7:1	≥ 7:1
Minimum Letter inner spacing	≤70um	4 mils	6 mils
	71-140um	4 mils	8 mils
	>140um	4 mils	10 mils
Letter to letter	/	2.5 mils	2.5 mils
Silkscreen to Cu Pad	/	4 mils	6 mils
Silkscreen to outline or V-cut	/	≥6 mils	≥8 mils
Location accuracy	/	4 mils	6 mils
Silkscreen ink thickness	/	10-20 um	10-20 um
Silkscreen color	/	White	White, Black, Yellow
Silkscreen block	/	5*12mil	5*12mil

We have 2D barcode or QR code printing capability with minimum QR code size of 5mm x 5mm.
Minimum area to add date code and UL markings is 10x15mm.

Carbon Paste

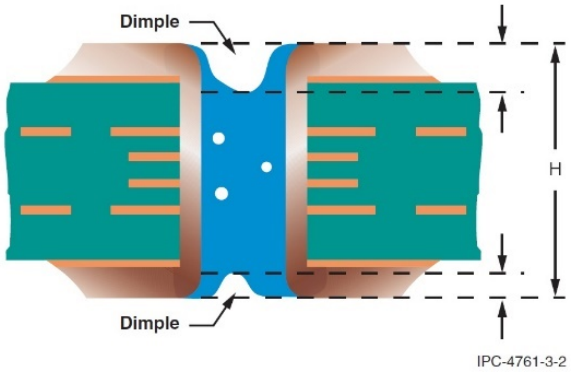
Item	Type	Supplier	Range of Application	Note
Carbon paste	MRX-713J-A	TAMURA	1.PCB's without special resistivity requirements 2.PCB's with low resistivity (Sheet resistivity ≤25Ω)	Thickness 15um and Sheet resistivity 15-25Ω
Carbon paste	CAPITON-901B	ShengTianFeng	Carbon paste with high resistivity (Sheet resistivity 400Ω)	Thickness 25um and Sheet resistivity 400Ω
Peelable Mask	SD-2955	PETERS	All applications requiring peelable mask	/

Peelable Mask	XBD-620BG	Xinbodun	All applications requiring peelable mask	/

5.6 Via Plugging of Through Holes

We recommend designers reference IPC-4761 on Protection of Via Structures. This document explains several types of via plugging method, and provides diagrams and application guidelines for each.

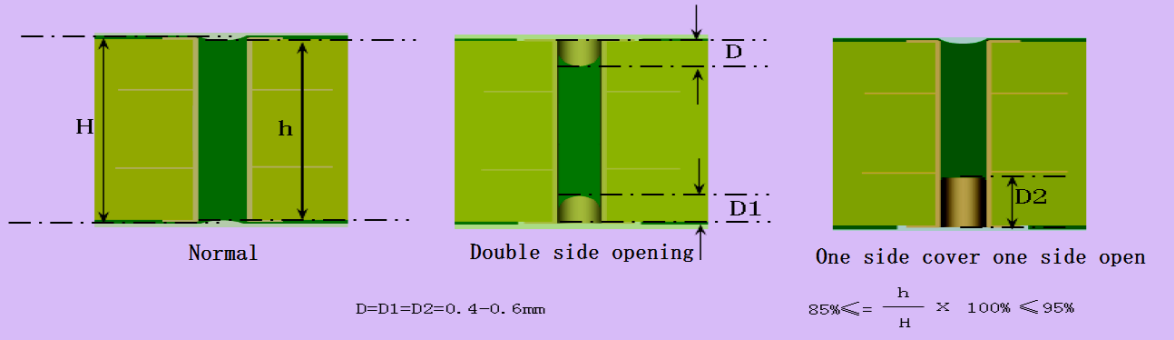
Sunshine offers several methods of plugging PTH's or vias. Generally, the lowest cost method of via plugging is by using soldermask to fill the via and both sides are closed or covered by soldermask. This method has no cost adder but it cannot guarantee full plugs and there may be dimples, voids or cracks in the final plug (see diagram below).



For Via-in-Pad designs where a solid via fill or fully metallized pad is required, we recommend using NCVF or POFV process (see below). This process is described in IPC-4761 as Type VII. This process allows you to select which vias are plugged/capped but the drawbacks are higher cost and cycle time. Sunshine does not recommend or offer tenting of vias (IPC-4761 Types I and II). Dry film soldermask is not commonly available and tenting can result in blowholes or outgassing during assembly.

In all cases, Sunshine strongly advises against the use of singled-sided plugs, where the via is partially plugged and the soldermask opening is covered on 1 side and opened on the other side. The reason is single-sided plugs can result in solution entrapment during fabrication or assembly, resulting in corrosion of the plated barrel over time. We recommend via to be either plugged and closed on both sides, or unplugged and opened on both sides to allow process chemistries to rinse through and the holes to be dried completely.

5.6.1 Soldermask Plug



Type	Board Thickness	Hole Size	h/H
SM filling (Both sides covered)	0.5-4.0mm	≤0.65mm（A/R≤10:1）	≥85%
SM filling (Both sides opened)	0.6-2.8mm	≤0.50mm（A/R≤10:1）	≥15%

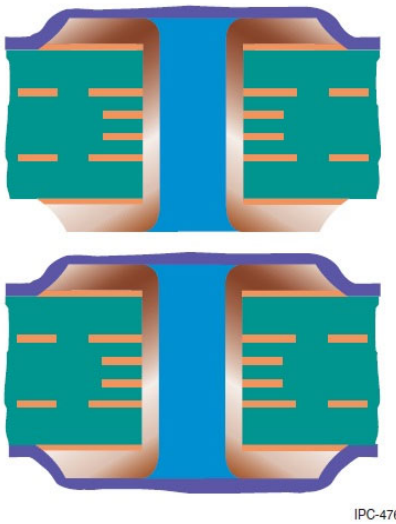
5.6.2 POFV (Plated Over Filled Via)

This process has several names: VIP (via in pad), POFV (Plated Over Filled Via), or NCVF (Non-Conductive Via Fill) – these all refer to the same process. This method is required for Via-in-Pad designs where the via is fully plugged and the surface must be metallized. The holes are filled with non-conductive epoxy, cured, planarized, and plated over. This process has becoming increasingly popular over the years, and Sunshine China factories have specialized equipment to perform all steps internally.

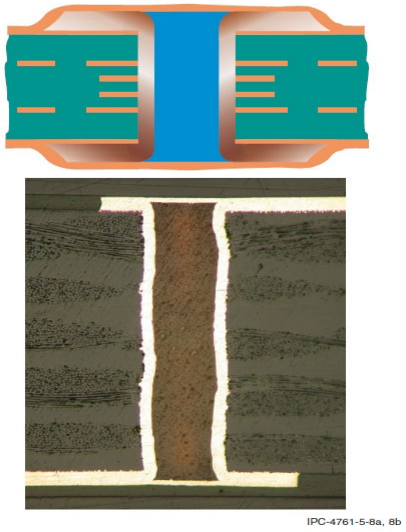
Please reference IPC-6012D (3.6.2.11) for IPC specifications for cap plating thickness, max dimple depth, and copper wrap requirements, which are followed by Sunshine.

Design suggestions are:

Panel size	Board Thickness	Hole Type	Hole Size (Finished)	Aspect Ratio
Max: 630*780mm Min:110*110mm	0.1-12.0mm	Through hole	≤1.0mm	≤30:1
		Blind via	≥0.05mm	Laser A/R≤2:1 Mechanical A/R≤3:1
		Back drill	≤0.50mm	≤10:1



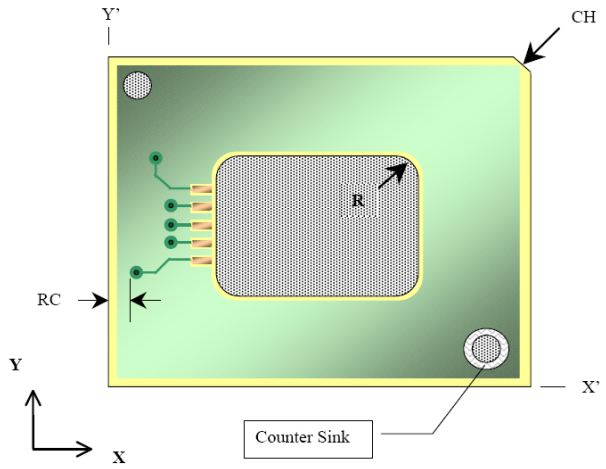
Soldermask Plug and Coat



POFV (Plated Over Filled Via)

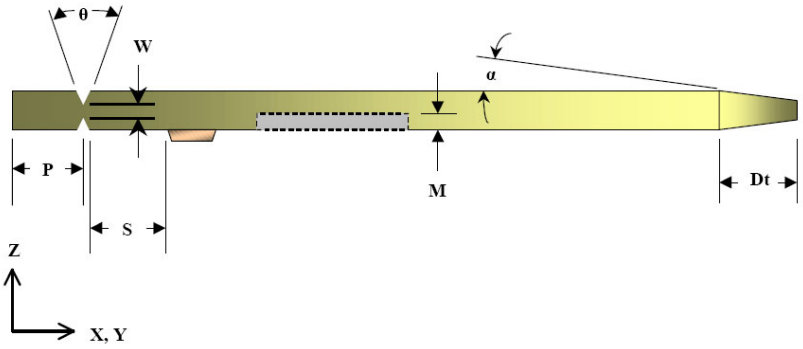
Diagrams are from IPC-4761

5.7 NC Rout



Item	Parameter	Standard	Advanced
R	Internal Radius	0.4-2.4mm	
RC	Min. Rout to Copper Spacing	0.2mm	
CS	Counter Sink (included angle)	±0.15mm	±0.1mm
CH	Chamfer Tolerance to Nominal	±0.15mm	±0.1mm
X',Y'	Fabrication Tolerance to Nominal	0.1mm	
D	Router Bit Diameter	Max. 2.4 mm, Min. 0.6 mm	
Other	Minimum Rout Width for Alum material	1.60mm	

5.8 V-Score



Item	Parameter	Standard
θ	Score Blade Angle	30 45 60 degrees
P	X & Y Positional Tolerance	0.1mm
W	Scored Web	About 1/3 board thickness
	Score Depth Tolerance	±0.1mm
S	Score to Nearest Copper Feature	0.4mm

	Jump Score Positional Tolerance	±0.1mm
T	Minimum board thickness for Score Maximum board thickness for Score	0.40mm≤T≤3.20mm
Dt	Bevel Angle	30, 45, 60 degrees
	Bevel Dimensional Tolerance	±0.1mm
M	Control Depth Mill Tolerance	±0.1mm
T	Minimum board thickness for Bevel Maximum board thickness for Bevel	0.80mm≤T≤6.00mm

6. Surface Finishes

Individual Types	Suggested Parameters	
Hot Air Solder Level(HASL)	1-40um	
Electrolytic Nickel/Gold	Ni:100 µ" min	Flash Au:3-10 µ"
		Hard Au: 10-50 µ"
		Soft Au: 3-30 µ"
Electroless Nickel Immersion Gold (ENIG)	Ni: 118 – 236 µ"	Au: 2-5 µ"
Immersion Tin (ImSn)	Sn:8-12 µ"	
Immersion Silver (ImAg)	Ag: 4-12 µ"	
Organic Solderability Preservative (OSP)	0.2-0.6 µm	
Electroless Nickel, Electroless Palladium, Immersion Gold (ENEPIG)	Ni: 118 – 236 µ"	Pa: 2-5 µ" Au: 2-5 µ"

Combination Finishes	Suggested Parameters	
HASL & Selective Electrolytic Ni/Au (HASL for solder pads with Ni/Au on contact pads)	Ni:118 – 236 µ"	Hard Au 35-50 µ"
Selective Electrolytic Ni and Soft Au (Thin Au for soldering, thick for wire bonding)	Ni:118 – 236 µ"	Soft Au: 3-8 µ" & 35-50 µ"
Selective Electrolytic Ni and Hard Au (Thin Au for soldering, thick for contact pads)	Ni:118 – 236 µ"	Hard Au: 3-8 µ" & 35-50 µ"
Selective Electrolytic Ni/Au and OSP Wire Bond or Contact Pads Solder Pads	Ni:118 – 236 µ" OSP: 0.2-0.5 µm	Soft or Hard Au 35-50µ"

Remark: Mixed or other Finishes need to be confirmed by process engineers.

7. Electrical Test

Typical electrical test parameters are:

- Test Voltage 250 Volts
- Continuity 20 Ohms
- Isolation Resistance 20 Meg-Ohms

7.1 Netlist Testing

Sunshine offers a wide range of electrical test equipment and capabilities. Most bare board testing is done on universal grid testers with test fixtures built in-house. For small lots or extremely fine pitch configurations, flying probe testers are used.

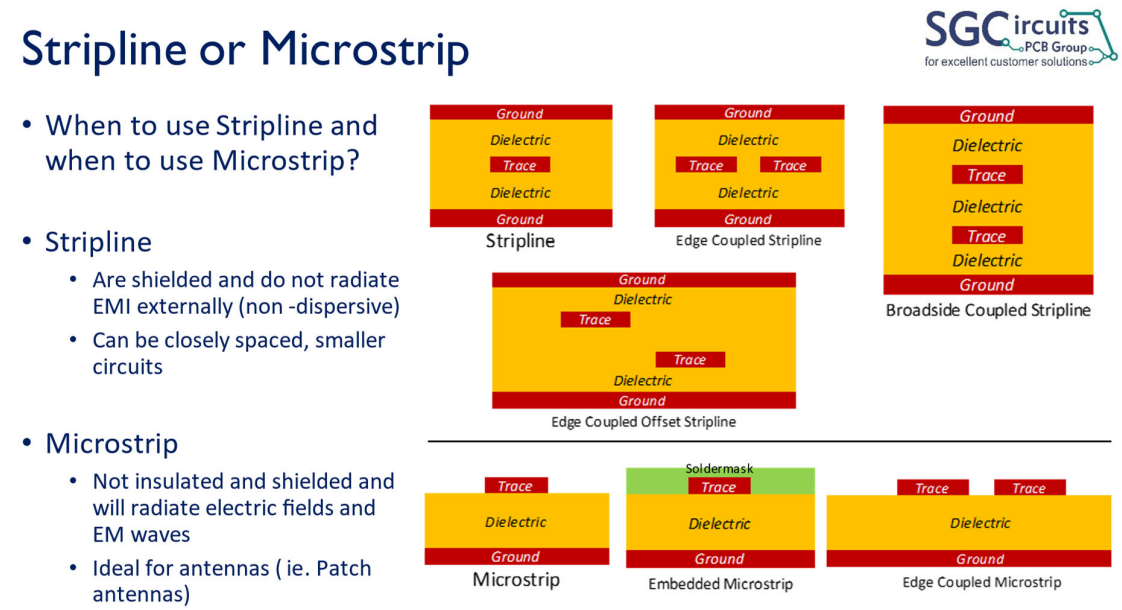
7.2 HIPOT Testing

HIPOT testing is conducted at inner layer process as wells on finished raw PCB's to insure isolation between all power / ground planes. Testing may be conducted with respect to current leakage or mΩ resistance between biased layers. With the trend toward decreasing thickness of dielectric layers it is necessary to re-think the traditional 500V HIPOT test. Boards designed with 0.002" (or less) dielectrics and nominal spacing between drilled vias and planes <0.01" may not be able to withstand a 500V bias and meet required current leakage or mΩ resistance standards. Consideration needs to be given to the actual working voltage of the board under test and the maximum expected transient voltage when deciding how best to design a HIPOT rest for a given PCB.

8. Controlled Impedance

8.1 Impedance Basics

Controlled impedance lines may be designed in many configurations. The most common are microstrip (surface) and stripline (internal). Variations of these basic forms include microstrip with and without solder mask, embedded microstrip, differential microstrip, edge coupled microstrip, edge coupled differential stripline, broadside coupled stripline, and edge-coupled offset stripline.



The variables of controlled impedance structures include the following:
1. Thickness of the copper signal trace
2. Width of the copper signal trace (Width of top and bottom of trapezoidal shape)
3. Thickness of the dielectric material between the trace and the reference plane
4. Pitch of differential pairs (spacing between parallel traces)
5. Dielectric constant (Er or Dk) of the materials around the impedance trace
6. Horizontal distance to ground guards, if any

We recommend designers specify on the drawing which line widths on which layer are controlled impedance, type of impedance (singled ended or differential), reference layers, required impedance value, and tolerance. For differential impedance, the target spacing also needs to be stated.
Example: 50 Ω singled-ended impedance +/-10%, on 0.004" lines on L3 referencing L4.

If more than one impedance value is required on a given layer and/or there are various controlled impedance structures within the same PCB, it is beneficial to provide an Impedance Table on the master drawing with all the relevant information, see example table below.

If 0.005" lines are to be 50Ω single-ended and other 0.005" lines on the same layer are to be 100Ω differential pairs, then it is best to set the differential pair lines at a slightly different width (i.e. 0.0051”) so CAM operators can differentiate between them, and make the necessary adjustments to the final line width to the correct traces.

Example Table (suggested to be added to master drawing):

Controlled Impedance Requirements

Layer	Lines	Pitch	Ref. Layer	Impedance(Ω)	Tolerance(+/-%)
Top	0.007"	N/A	2	50 SE	10
3	0.005"	N/A	2&4	50 SE	10
3	0.0051"	0.015"	2&4	100 Diff	10
6	0.005"	N/A	5&7	50 SE	10
6	0.0051"	0.015"	5&7	100 Diff	10
Bottom	0.007"	N/A	7	50 SE	10

For most applications, our understanding is the final impedance value will take precedence over original line widths in the data. We will make adjustment in the line widths and dielectric thicknesses to come as close as possible to target impedance values. We request the customer to review our stackup and impedance modeling during the EQ stage. If for any reason the line widths in the original data take precedence and must not be changed, then this must be made clear in the drawing notes.

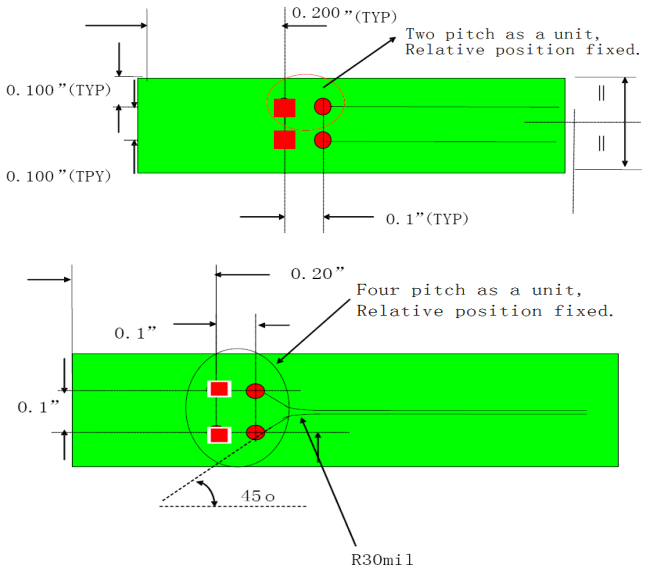
While it is possible to achieve impedance tolerances of +/- 5%, the manufacturing tolerances in the dielectrics, etched trace widths/spacing, and variations in the dielectric constant makes this very difficult, esp. for 50 ohms or below traces. Tight impedance tolerances may require several lots to finetune the values and may result in poor yields, therefore there will be a cost penalty for anything less than the standard +/- 10% impedance tolerance.

Parameter	Standard	Advanced
Impedance Tolerance ≥ 50 ohms	±10%	±5%
Impedance Tolerance ≤ 50 ohm	±5 ohm	±2.5ohms

8.2 Impedance Measurements and Coupons

Sunshine uses time domain reflectometry (TDR) for testing impedance on PCB's. Measurements are performed on the coupons in the rails of Sunshine working panels which represent the impedance traces inside the PCB. The coupon design incorporates the same geometry of the PCB with respect to dielectric thickness, copper weights, line widths, configuration, and are controlled in the same way as the traces inside the PCB. For most production orders, the TDR used for measurement of impedance coupons is the **Polar CITS880s**. Impedance measurement reports are provided with all controlled impedance orders and are included with the QA Report. The coupons are normally not shipped to customer but are available upon request. Original files from the Polar tester are also available upon request.

The design of the impedance coupons follows specifications from Polar. There are requirements regareding the length of coupon traces and distance between test holes/pins. Test hole diameter are 1.0-1.2 mm, and pitch to pitch distance are 0.1".



8.3 How to read Stackup and Impedance Diagrams from Sunshine

Sunshine FAE regularly provides stackup and impedance diagrams to customers, and sometimes we get questions about how to read or use these diagrams. Here is a brief explanation of these diagrams and the information they contain. See example of 12L HDI board below.

The top of the page provides identifying information such as the Job Name (or Sunshine P/N), Customer Code, and Customer Part Name and Revision. The “Customer Required Finished Thickness” is the overall thickness specification, and below that is shown our calculated thickness. Please note this “Estimated Finished Thickness” is the expected thickness after lamination measured over raw

foil prior to plating. After copper plating and soldermask are added, the overall thickness will usually gain 4 to 6 mils over this value.

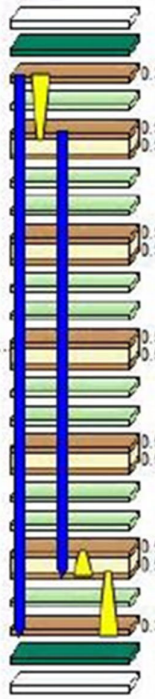
Job Name: **QCGU00197A0**
Customer: **U00**

Customer Required Finished Thickness: **62.00 (± 6.20) mils (Over mask on plated copper)**
Estimated Finished Thickness: **56.44 mils (Over raw foil)**

Part Name:

Revision:

Stackup Notes: Preliminary Stackup, subject upon receipt and review of data

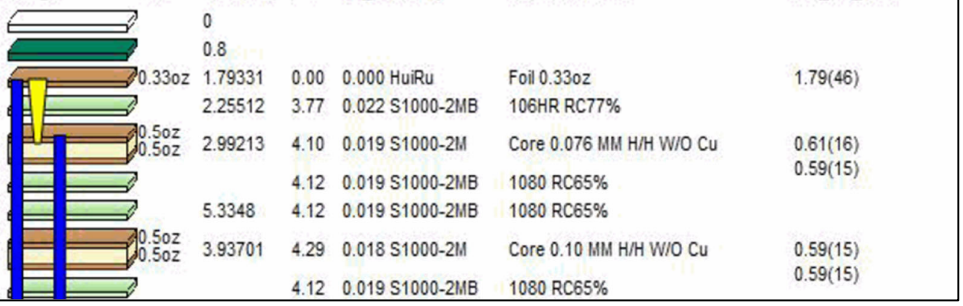


Lyr	LayType	CU %	SM_DF	Foil	Thk (Mil)	Er	DF_	Family	Generic Name	Fin_Cu_Thk
CS			0.000		0					
CM			0.025		0.8					
L1	Sig	50		0.33oz	1.79331	0.00	0.000	HuiRu	Foil 0.33oz	1.79(46)
					2.25512	3.77	0.022	S1000-2MB	106HR RC77%	
L2	PG	76		0.5oz	2.99213	4.10	0.019	S1000-2M	Core 0.076 MM H/H W/O Cu	0.61(16)
L3	Sig	28		0.5oz		4.12	0.019	S1000-2MB	1080 RC65%	0.59(15)
					5.3348	4.12	0.019	S1000-2MB	1080 RC65%	
L4	PG	76		0.5oz	3.93701	4.29	0.018	S1000-2M	Core 0.10 MM H/H W/O Cu	0.59(15)
L5	Sig	28		0.5oz		4.12	0.019	S1000-2MB	1080 RC65%	0.59(15)
					5.3348	4.12	0.019	S1000-2MB	1080 RC65%	
L6	PG	76		0.5oz	9.84252	4.29	0.018	S1000-2M	Core 0.25 MM H/H W/O Cu	0.59(15)
L7	PG	76		0.5oz		4.12	0.019	S1000-2MB	1080 RC65%	0.59(15)
					5.3348	4.12	0.019	S1000-2MB	1080 RC65%	
L8	Sig	28		0.5oz	3.93701	4.29	0.018	S1000-2M	Core 0.10 MM H/H W/O Cu	0.59(15)
L9	PG	76		0.5oz		4.12	0.019	S1000-2MB	1080 RC65%	0.59(15)
					5.3348	4.12	0.019	S1000-2MB	1080 RC65%	
L10	Sig	28		0.5oz	2.99213	4.10	0.019	S1000-2M	Core 0.076 MM H/H W/O Cu	0.59(15)
L11	PG	76		0.5oz		3.77	0.022	S1000-2MB	106HR RC77%	0.61(16)
					2.25512					
L12	Sig	50		0.33oz	1.79331	0.00	0.000	HuiRu	Foil 0.33oz	1.79(46)
SM			0.025		0.8					
SS			0.000		0					

Impedance Table

Layer	Required Impedance (Ohms)	Tolerance (Ohms)	Impedance Type	Upper Ref	Lower Ref	Customer L/W mils	Customer Space mils	Finished L/W mils	Finished Space mils	CoPlanar Space mils	Calculated Impedance (Ohms)	
L1	50.0	±5.0	se_coated_microstrip	None	L2	3.45	---	3.45	---	---	49.50	
L1	90.0	±9.0	diff_coated_microstrip	None	L2	2.99	4.30	2.99	4.30	---	89.61	
L1	100.0	±10.0	diff_coated_microstrip	None	L2	3.00	9.00	3.00	9.00	---	99.45	
L3	50.0	±5.0	se_stripline	L2	L4	3.25	---	3.25	---	---	49.35	
L3	100.0	±10.0	diff_stripline	L2	L4	3.00	7.00	3.00	7.00	---	99.04	
L5	50.0	±5.0	se_stripline	L4	L6	3.80	---	3.80	---	---	49.73	
L5	100.0	±10.0	diff_stripline	L4	L6	3.00	4.80	3.00	4.80	---	99.86	
L5	90.0	±9.0	diff_stripline	L4	L6	3.85	4.65	3.85	4.65	---	89.58	
L8	50.0	±5.0	se_stripline	L7	L9	3.80	---	3.80	---	---	49.73	
L10	50.0	±5.0	se_stripline	L9	L11	3.25	---	3.25	---	---	49.35	
L10	100.0	±10.0	diff_stripline	L9	L11	3.00	7.00	3.00	7.00	---	99.04	
L10	90.0	±9.0	diff_stripline	L9	L11	3.25	4.25	3.25	4.25	---	90.00	
L12	50.0	±5.0	se_coated_microstrip	L11	None	3.45	---	3.45	---	---	49.50	
L12	90.0	±9.0	diff_coated_microstrip	L11	None	2.99	4.30	2.99	4.30	---	89.61	
L12	100.0	±10.0	diff_coated_microstrip	L11	None	3.00	9.00	3.00	9.00	---	99.45	

Now we will go over the stack-up or construction diagram. Each column has a header but some of their meaning may not be obvious. From left to right:

Lyr	LayType	CU %	SM_DF	Image	Foil	Thk (Mil)	Er	DF_	Family	Generic Name	Fin_Cu_Thk
CS			0.000			0					
CM			0.025			0.8					
L1	Sig	50			0.33oz	1.79331	0.00	0.000	HuiRu	Foil 0.33oz	1.79(46)
						2.25512	3.77	0.022	S1000-2MB	106HR RC77%	
L2					0.5oz						
L3	PG	76			0.5oz	2.99213	4.10	0.019	S1000-2M	Core 0.076 MM H/H W/O Cu	0.61(16)
	Sig	28									0.59(15)
							4.12	0.019	S1000-2MB	1080 RC65%	
						5.3348	4.12	0.019	S1000-2MB	1080 RC65%	
L4					0.5oz						
L5	PG	76			0.5oz	3.93701	4.29	0.018	S1000-2M	Core 0.10 MM H/H W/O Cu	0.59(15)
	Sig	28									0.59(15)
							4.12	0.019	S1000-2MB	1080 RC65%	

1. **Lyr** is the sequence number for the copper layer (ie. L1= layer 1 and so on).
2. **LayType** is the type of copper pattern (Sig= Signal, PG= Power/Ground).
3. **CU%** is the percent copper retained after etch. The value is provided by the CAD system based on the actual copper pattern of each layer in the files. If no data is received, we assume 28% for internal signal and 76% for internal plane layers.
4. **SM_Df** is the Df value or loss tangent of the soldermask.
5. **Image** is a simplified drawing with different colors for foil (brown), prepreg (green), and core (yellow). Vias are shown with mechanically drilled through-holes and blind vias in blue, and microvias in yellow.
6. **Thk(Mil)** is the expected thickness of the dielectric after pressing (with exception of the outer cu thickness). Core thicknesses will be in accordance with vendor standard cores built to tolerances per IPC-4101. The prepreg thicknesses are estimates based on the type of prepreg used and the **CU%** of the layers facing that dielectric. Sometimes symmetric prepreg layers that look the same will have different press-out thickness due to differences in the CU% of the adjacent copper layers.
7. **Er** is the Dk or dielectric constant of the material in that layer. Dk's vary slightly depending on the resin to glass ratio.
8. **Df** is the loss tangent or permittivity of the material. Df's also vary slightly based on the resin content of the material.
9. **Family** is the material type selected for this part number. For example, the example is using S1000-2M material, and the suffix "B" denotes bonding ply which is prepreg of S1000-2M.
10. **Generic Name** provides details for material ordering. For cores, the example L2/L3 is .076 mm H/H w/o Cu which means .076mm core (measured without cu) with half ounce foil on both sides (H/H is read half over half). For prepregs, the example between L3/L4 is 2 plies of 1080 glass with 65% resin content (HR = high resin content).
11. **Foil_Cu_Thk** at the far right represents the estimated finished copper thickness after plating and processing. The values are expressed in mils and micron (um).

One common question we get is why do 2 prepreg openings that appear to be identical are shown to have different thicknesses? This is due to different copper retained after etch (see CU% column). Different amount of copper remaining after etch will result in different amount of resin required to fill the gap, resulting in slightly different thickness of the prepregs after press.

Finally we have the impedance table. Here we see the details of the impedance requirements, if any are present in the design. The left six columns state the customer requirements: layer, target value, tolerance, impedance model, and upper/lower reference plane layers. Many designers ask: which line width should I use for my layout?

Impedance Table												
Layer	Required Impedance (Ohms)	Tolerance (Ohms)	Impedance Type	Upper Ref	Lower Ref	Customer L/W mils	Customer Space mils	Finished L/W mils	Finished Space mils	CoPlanar Space mils	Calculated Impedance (Ohms)	
L1	50.0	±5.0	se_coated_microstrip	None	L2	3.45	---	3.45	---	---	49.50	
L1	90.0	±9.0	diff_coated_microstrip	None	L2	2.99	4.30	2.99	4.30	---	89.61	
L1	100.0	±10.0	diff_coated_microstrip	None	L2	3.00	9.00	3.00	9.00	---	99.45	
L3	50.0	±5.0	se_stripline	L2	L4	3.25	---	3.25	---	---	49.35	
L3	100.0	±10.0	diff_stripline	L2	L4	3.00	7.00	3.00	7.00	---	99.04	
L5	50.0	±5.0	se_stripline	L4	L6	3.80	---	3.80	---	---	49.73	
L5	100.0	±10.0	diff_stripline	L4	L6	3.00	4.80	3.00	4.80	---	99.86	
L5	90.0	±9.0	diff_stripline	L4	L6	3.85	4.65	3.85	4.65	---	89.58	
L8	50.0	±5.0	se_stripline	L7	L9	3.80	---	3.80	---	---	49.73	
L10	50.0	±5.0	se_stripline	L9	L11	3.25	---	3.25	---	---	49.35	

If this is a board that has already been laid out, then the “Customer L/W” will be the actual line width found in the design. When we model the impedance, we do our best to use the same line width as in the design files; however, dielectric constraints may require us to adjust the line width slightly to meet the target impedance. The “Finished L/W” is our suggested line width to be used in production (+/- manufacturing tolerances).

If this is for a board that has not been laid out yet, the PCB designer should use the “Finished L/W” for their design.

9. Array Panel Guidelines

Many customers require their boards to be panelized with suitable rails so the product can be run down an automated assembly line. It is best that an assembly array drawing or guidelines are supplied at the time of quoting. Please check with your contract manufacturer (CM) regarding their array preferences. However, we will cover a few basics on array panels.

There is basic information required to design the assembly array:

1. Depanelization method:
    a. V-score
    b. Tab with break holes (Rout and Retain)
    c. Solid tabs with V-score
    d. Solid tabs – no break holes (To be routed out by the CM after assembly)
2. Minimum or maximum array panel size (this can vary by CM or equipment):
    a. Typical minimum is 5.000” x 4.250” including the rails.
    b. Typical maximums:
        i. Board thickness ≤ 0.031” – ~11.00” x 9.00” including the rails.
        ii. Board thickness > 0.031” – ~19.00” x 14.00” including the rails.

3. Array requirements.
    a. Fiducials:
        i. Minimum pad size – 1.6mm is suggested minimum size
        ii. Minimum number of fiducials per side – We default to 3 per side
        iii. Minimum distance from board or panel edge – We default to center of rail
    b. Tooling holes:
        i. Minimum size – our typical minimum is 1mm to 3.2mm based on the rail size.
        ii. We prefer a minimum of 3 tooling holes towards the corners of the array panel.
    c. Constraints and other notes:
        i. Overhanging components must be considered
        ii. Keep out areas for connectors or other areas that require special attention should be noted
        iii. Minimum of 2mm spacing is required between boards for double V-cutting
        iv. Board orientation - can boards be rotated 180° for better material usage?
        v. If board is thin or long between assembly rails, warpage may be an issue.

10. Production Panel Information

One of the largest cost factors in PCB manufacturing is the base material cost. Here is some information to help optimize your design for best material use practices.

Sunshine purchases laminates in full sheets from the material supplier and cuts the sheets into working panels for fabrication. Sheet sizes include 43”x49, 41”x49”, and 37”x49”. Below is a list of our preferred working panel sizes for best material usage.

Other sizes are available; please contact us for more information.

Sunshine Preferred Sizes
24x21 inch (610 x 533 mm)
24x20 inch (610 x 508 mm)
24x18 inch (610 x 457 mm)
24x14 inch (610 x 356 mm)
24x13 inch (610 x 330 mm)
24x12 inch (610 x 305 mm)
16x21 inch (406 x 533 mm)
16x20 inch (406 x 508 mm)
16x18 inch (406 x 457 mm)
24x27 inch (621 x 692 mm)
24x28 inch (621 x 726 mm)

Allow minimum 0.6” border for tooling and coupons and minimum .08” (2mm) between arrays.
Remark： The thinnest FR4 core thickness for our standard process is .002” (0.05mm).

While we appreciate customers taking into consideration our panel sizes and material utilization rates, we are often unable to get customers to change their PCB dimensions or assembly panel sizes. Therefore, Sunshine maintains a large number of panel sizes and we take steps to maintain >70% material utilization rates in most cases. If we come across a PCB design with very low utilization rates, then we will do our best to notify the customer of this issue and resulting cost adder.

11. Contact Us

All information in this document are provided as a guideline to assist Sunshine customers in developing PCB designs in accordance with DFM standards and manufacturing capabilities. If any questions regarding this document, please reach out to our team.

Sunshine USA Engineering general email: US_FAE@sunshinepcb.com

Al Silveira, Senior DFM Engineer
Mobile 360-904-5117
alsilveira@sunshinepcb.com

Alfredo Perez, Sr. Field Application Engineer
Mobile 331-385-1457
alfredoperez@sunshinepcb.com

Jimmy Fang, VP of Business Development
Mobile 626-422-4296
jimmyfang@sunshinepcb.com