Sunshine Global Circuits

ATE Technology

Jan. 2026

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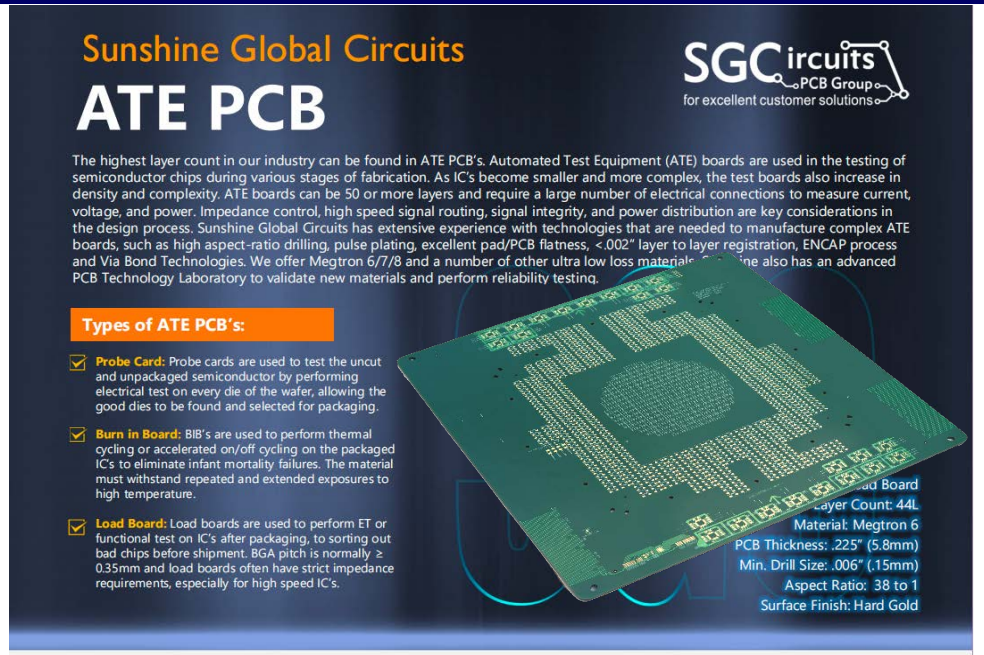
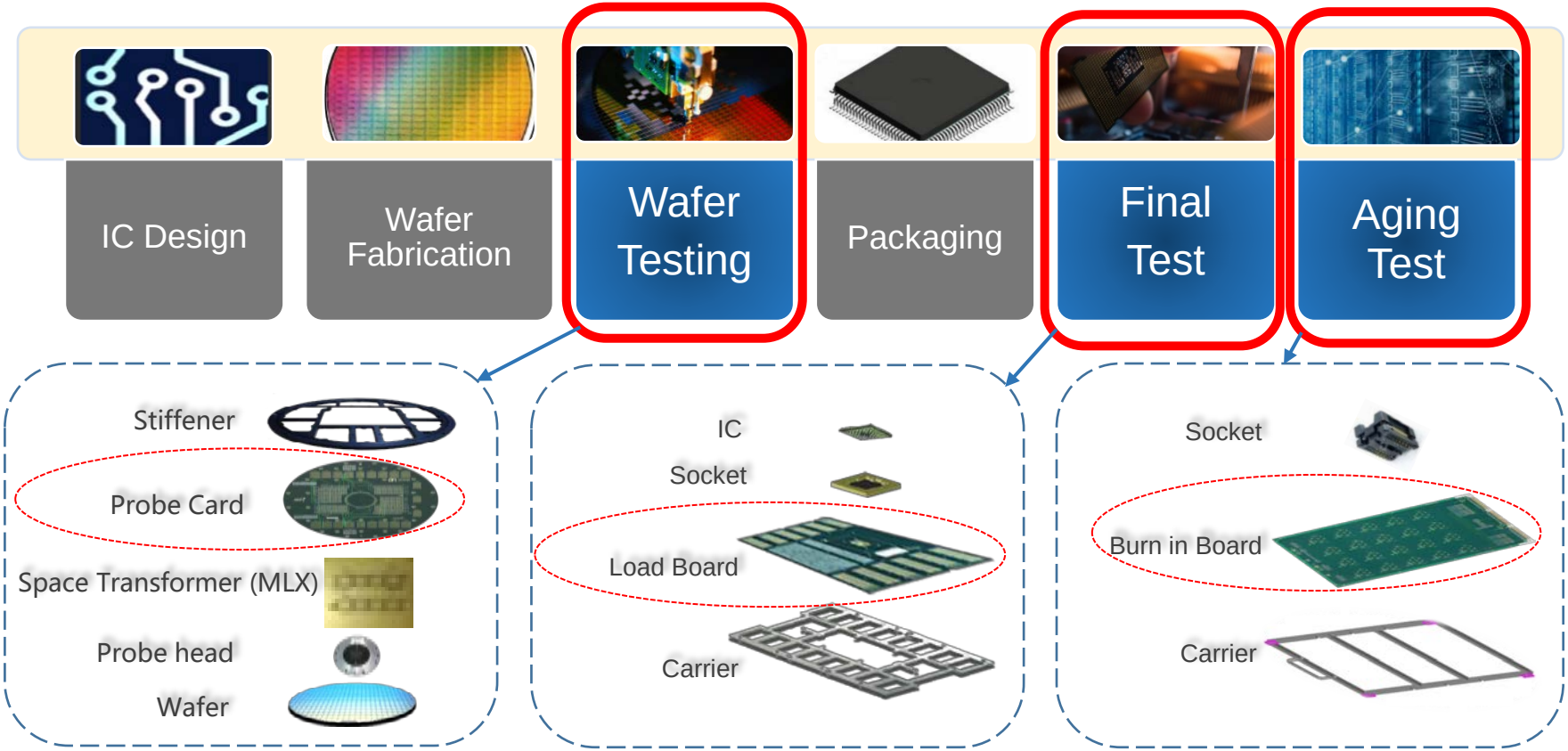
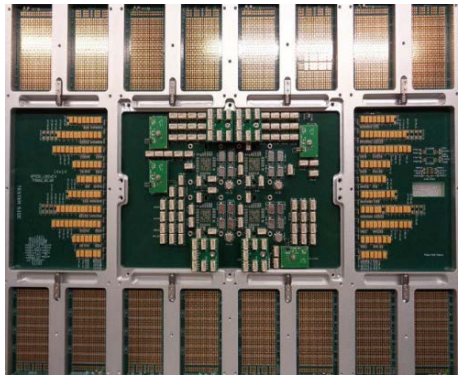


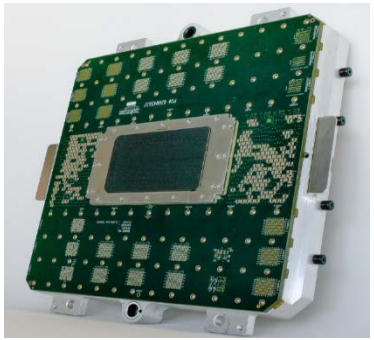
Introduction to ATE PCB's

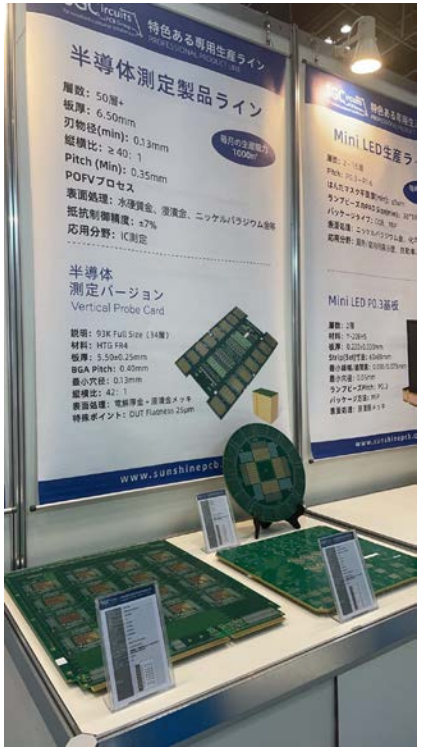


Introduction to ATE PCB's

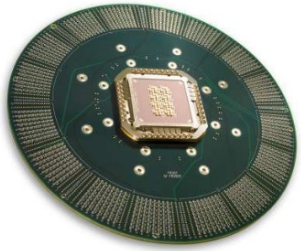
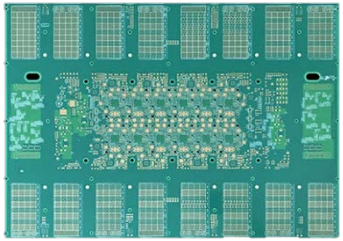
The Load Board or Probe Card acts as the interface between Automated Test Equipment (ATE) and the Device Under Test (DUT).







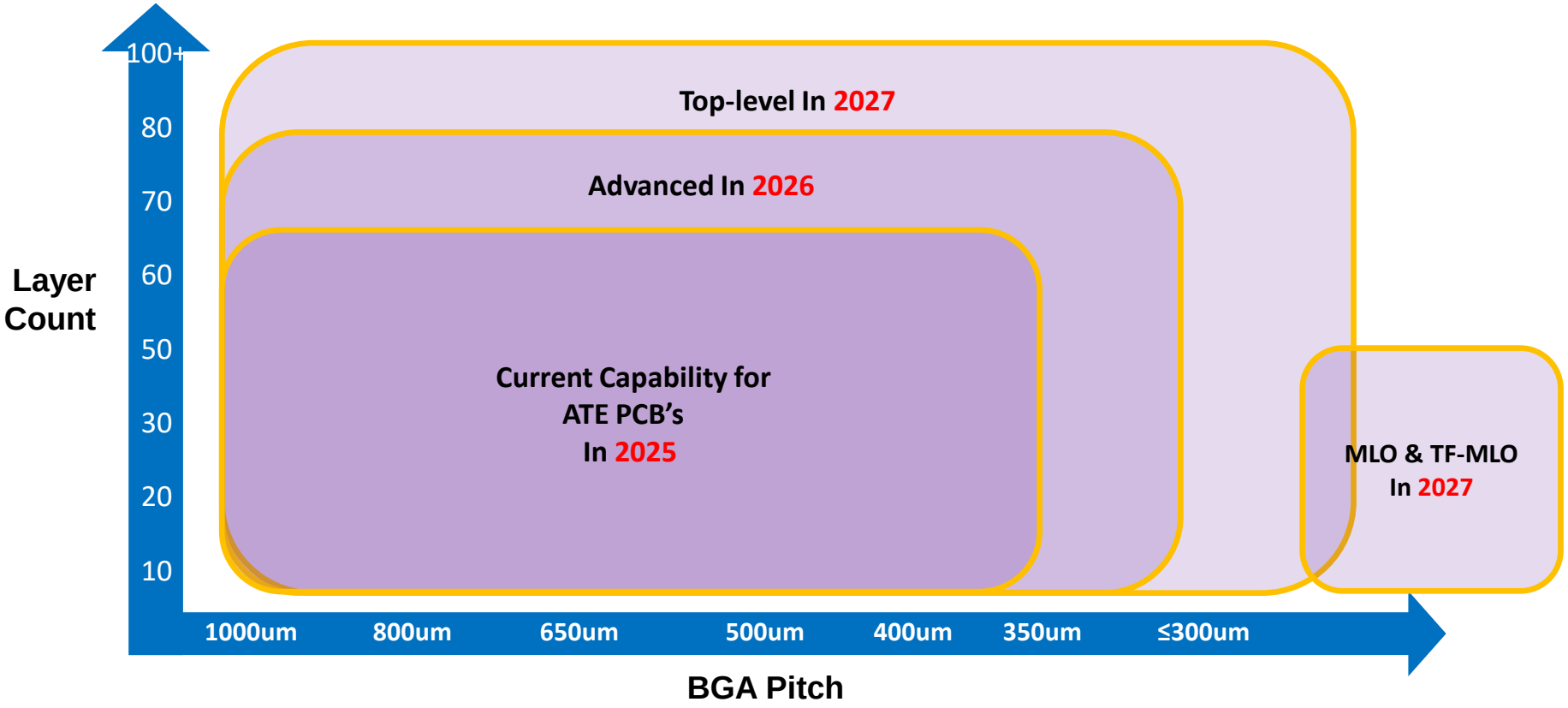
ATE Board Types

Type	Description	Example
Probe Card	Probe cards are used to test the uncut and unpackaged semiconductor by performing electrical test on every die of the wafer, allowing the good dies to be picked out. Normally, the BGA pitch of probe cards is no less than 0.3mm. If the pitch is less than 0.3mm, the probe card will be connected with probe head through an interposer and MLO, which calls for tight requirement for density, impedance and flatness control.	
Load Board	Load boards are used to perform the electrical test or functional test on each IC after packaging, to sorting out bad IC's before shipment. The BGA pitch is normally no less than 0.35mm and Load boards often have strict impedance requirements, especially for high speed or high frequency IC's.	
Burn in Board	BIB's are used to perform accelerated aging or "infant mortality" testing on the packaged IC's to confirm the reliability of the IC's. The BGA pitch is normally no less than 0.35mm. The PCB material is normally polyimide or BT to ensure resistance to high temperature for repeated and extended periods of time.	

Technical Features of ATE Boards

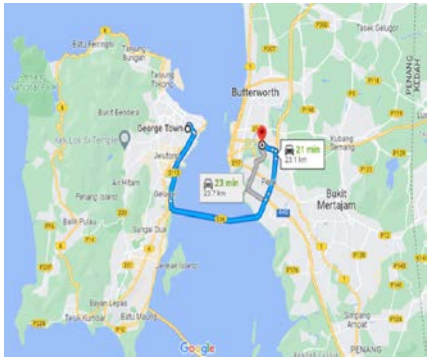
No.	Item	Description
1	Alignment & High Aspect Ratio	BGA pitch of load board & VPC is usually within 0.3 to 0.5 mm. Parallel testing channels: 4 sites, 8 sites, to 16 sites. 30 ~ 70 layers or higher, drill to copper is generally below 4mil. PCB technology challenges: layer to layer alignment for 30+ layers, drilling accuracy, high aspect ratio copper plating and resin plugging process.
2	Testing Interface for Super High Density	BGA pitch of high end vertical probe card is usually 85~200 um, even to 40~55 um which is out of PCB process capability, it's necessary to apply such space transformer as MLO/MLC as the transfer interface. IC substrate or wafer backend technology could be used as well.
3	Ultra Flatness	Vertical probe card and high-end ATE PCBs have high requirement for the flatness of DUT area, and the bow and twist shall be kept within 0.1%~0.2%. The range of the pad height at BGA area shall be kept within 50 um (2mil), high end applications requires this to be within 25~28 um (1mil).
4	Cosmetic Quality	The DUT area is interconnected through the probe, requiring pretty high quality of the pad surface without dents or damage, and no scratches or roughness issues on the hard gold surface.
5	Signal Integrity	The SI requirements call out +/- 5% impedance tolerance and stubs below 6 mil, which pushes the plating, etching uniformity, and back drill process capability.

ATE Product Positioning



Locations - Manufacturing Facilities

In Progress

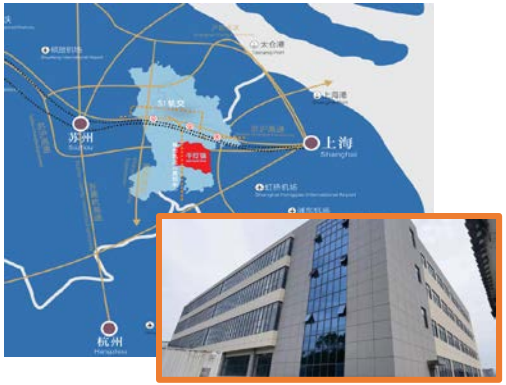


Dedicated ATE production line will be set up in Malaysia Penang plant by Q3 2026.

In Operation

Shenzhen plant is the current base for ATE products and new product development. The ATE line supports prototypes and small volume production.

In Progress

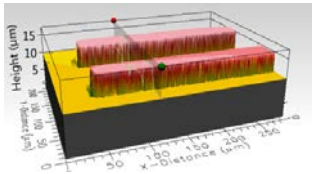


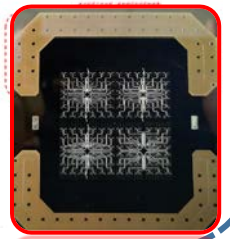
Suzhou ATE plant is under construction and is expected to be operational in Q4 2026.

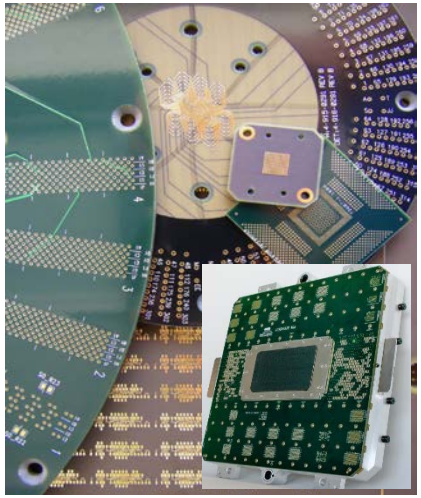
Technical Requirements

SGCircuits PCB Group
for excellent customer solutions

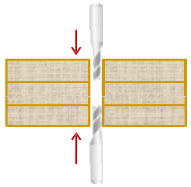
1. Fine line/spacing

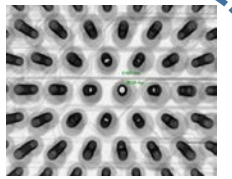
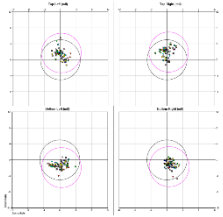



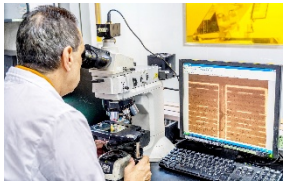
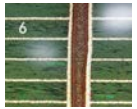
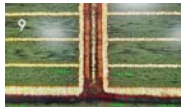


2. Alignment/Registration

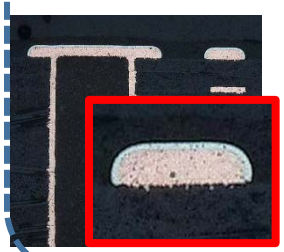
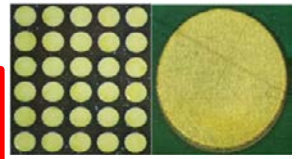


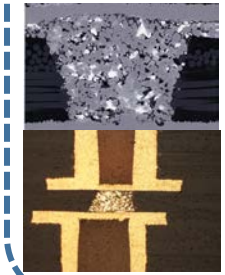
3. Pulse plating

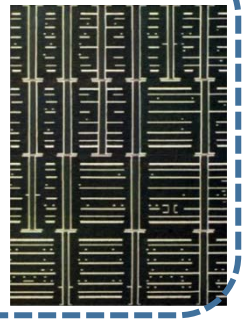




4. Pad flatness

5. Via bond

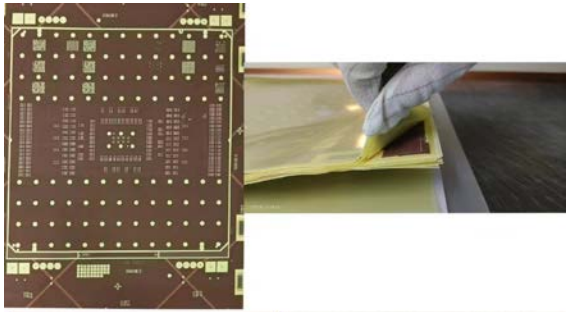


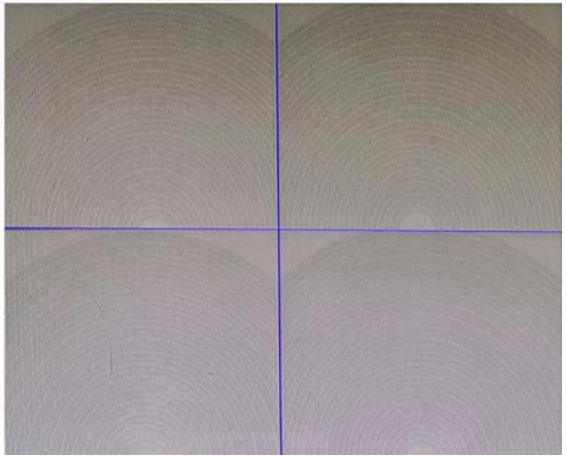


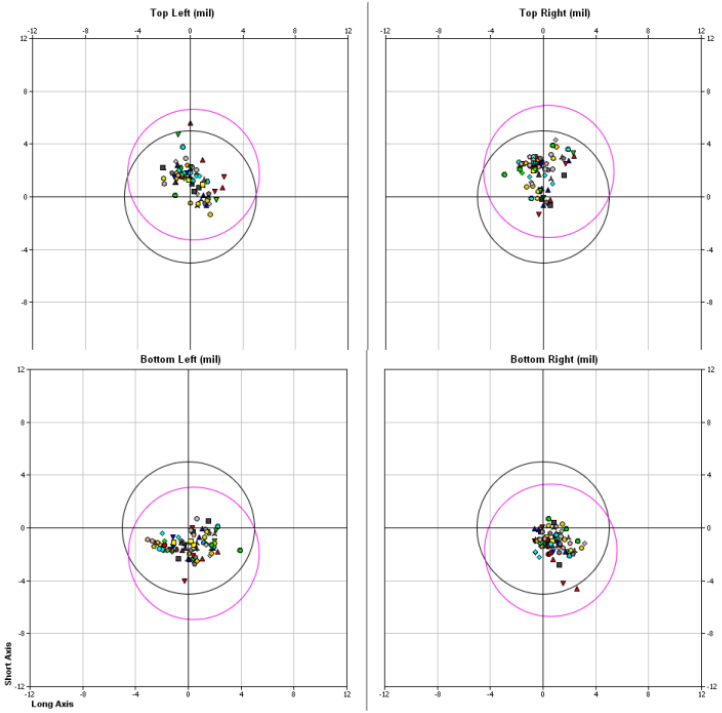
Key Technologies

Excellent Multilayer Layer to Layer Alignment

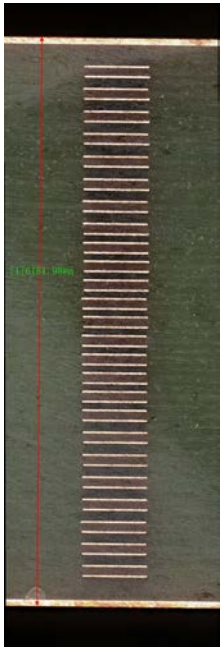
Less than +/- 2.0 mil in DUT area



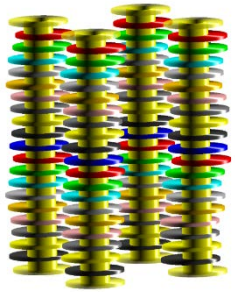


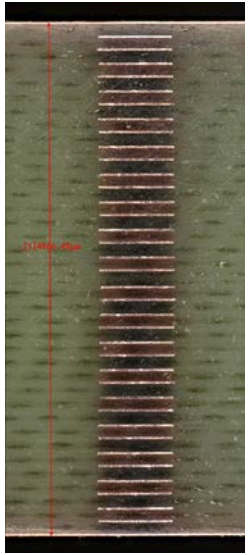


layer to layer Position Analysis



Microsection

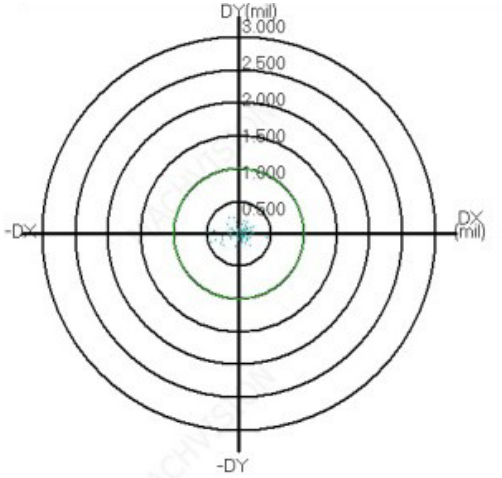




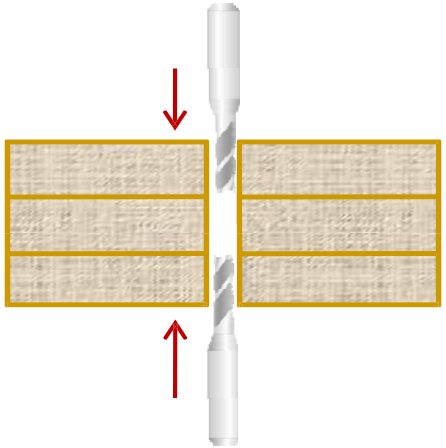
Key Technologies

High Density and High Aspect Ratio Drilling

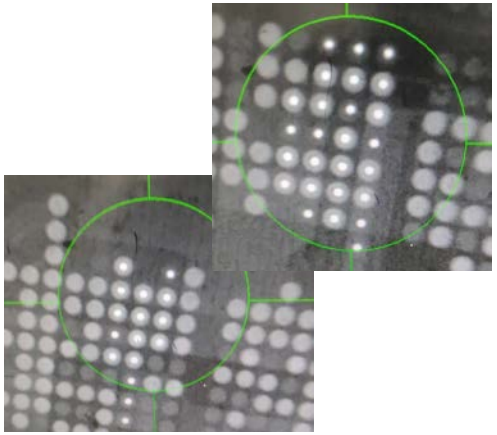
1. Excellent Drilling Positional Accuracy, Cpk ≥ 2.0 (±1mil)
2. Excellent Flip Drill Alignment: ≤ 25 μm



Positional accuracy



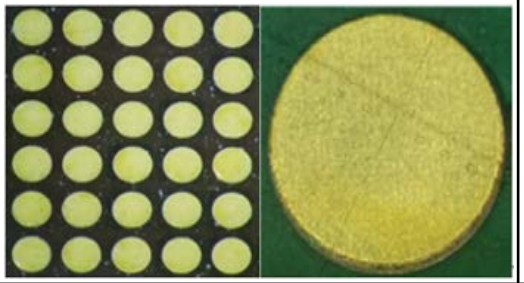
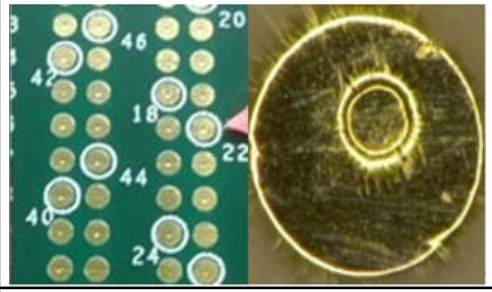
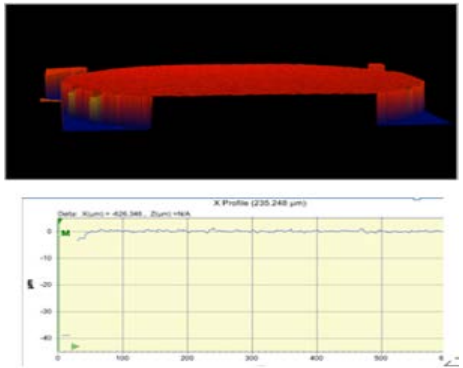
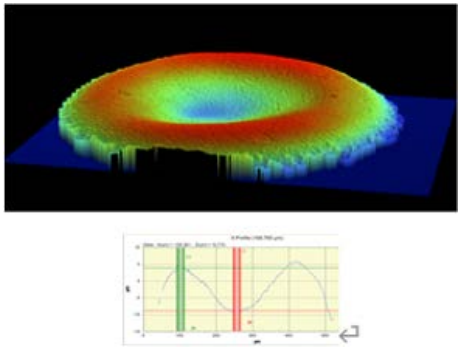
Flip-drill diagram



Micro section after flip-drill

Key Technologies

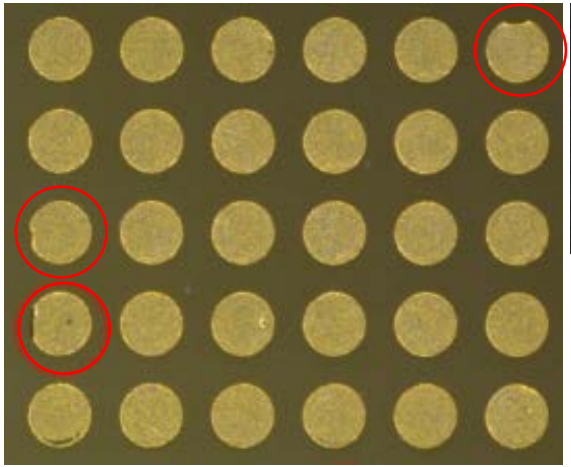
Excellent DUT Pad Flatness

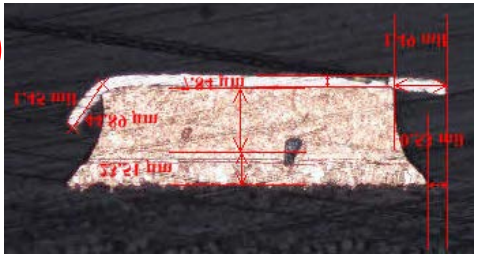
Item	ATE Pads		Normal Product Pads	
	Picture	Result	Picture	Result
Appearance		No dimple		With Dimple
Roughness (3D profilometer)		No dimple		With Dimple < 15um

Key Technologies

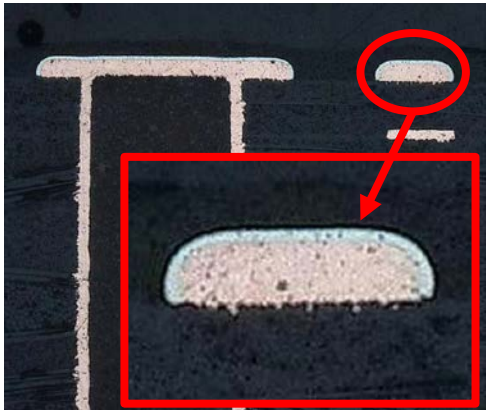
ENCAP Technology

- Encap process is a special process for electrolytic Ni/Au plating on outerlayer pads
- Standard process results in large overhang of Ni/Au which may become dislodged, causing shorts and damaged pads
- Encap process eliminates overhang of Ni/Au on contact pads
- Generally, the Encap process is applied to products with BGA pitch ≤ 0.5mm





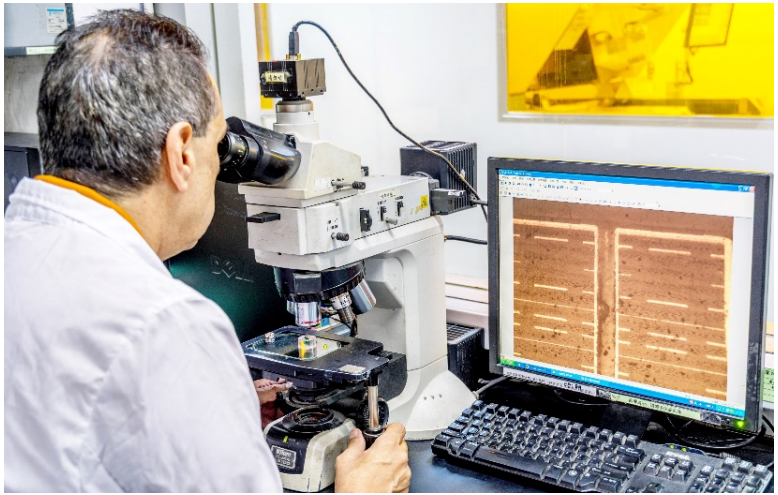
Microsection with overhang



Microsection after Encap Process

Key Technologies

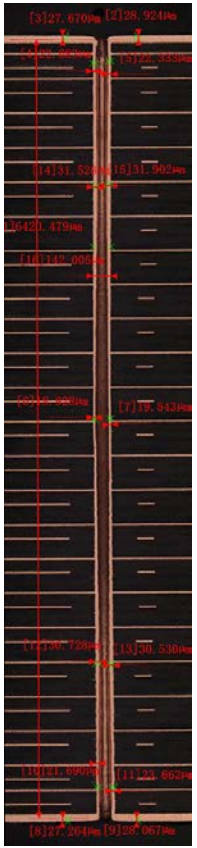
Pulse Plating for High Aspect Ratio (>30:1)



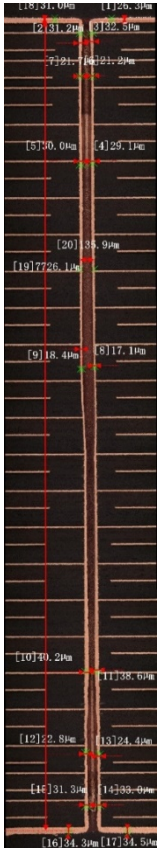
Reverse pulse plating enables the plating of very high aspect ratio holes using periodic pulses of opposite polarity, resulting in hole walls with excellent copper uniformity.

Aspect Ratio 42:1 (TP:＞80%)

Aspect Ratio 50:1



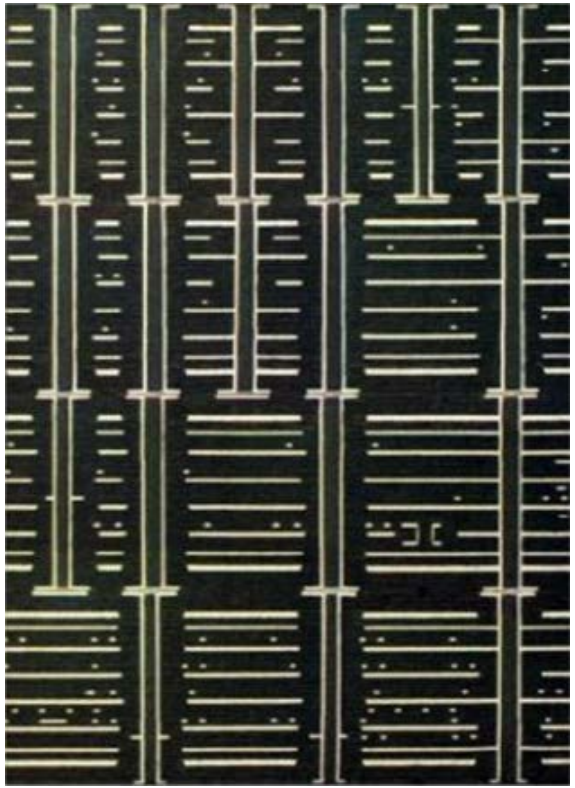
Aspect Ratio 60:1



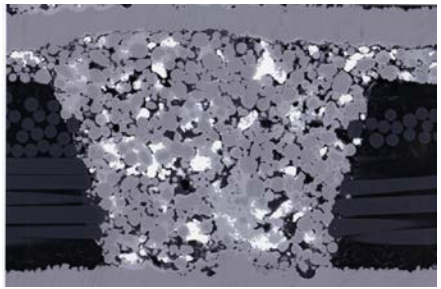
Key Technologies

Z-Axis Interconnects – Via Bond

- Cu/Sn paste undergoes sintering during lamination process, creating a conductive bond that is strong and conductive
- Enables formation of any layer interconnects and alternatives to stacked microvias or blind/buried vias
- Enables connecting multiple subs to form very high layer count PCB's
- Reduces lam cycles, leadtime, & costs
- Very high layer count (> 70 layers)
- Very high aspect ratio (> 46:1)
- Very high board thickness (> 0.315")



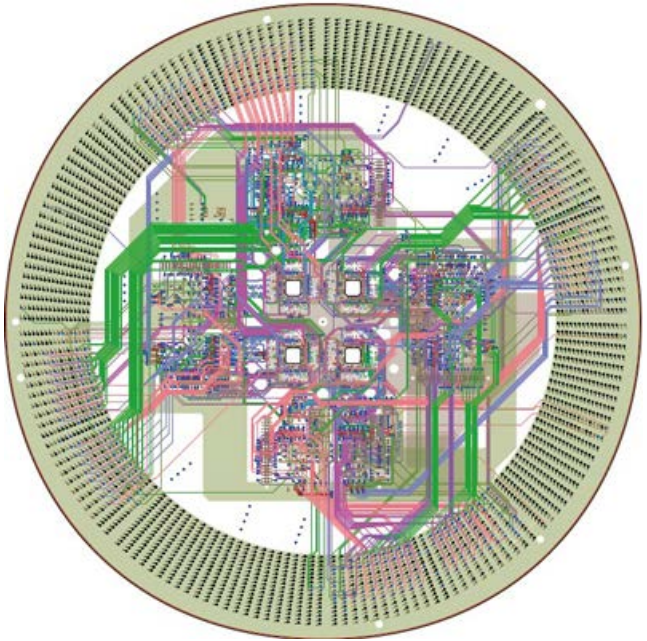
Microsection of via



SEM picture of sintered via

Key Technologies

Ultra Flatness



Maximum Bow/Twist: 0.15% (.0015”/inch)

Panel Flatness: ≤200 um

DUT Flatness: ≤50 um

Standard

Vs

Ultra Flatness

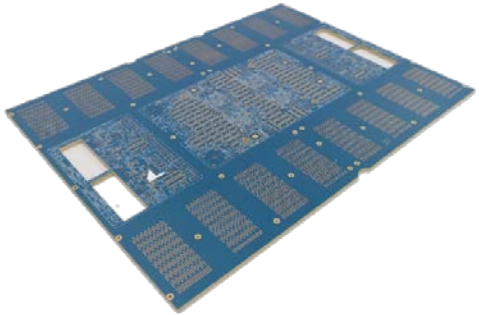
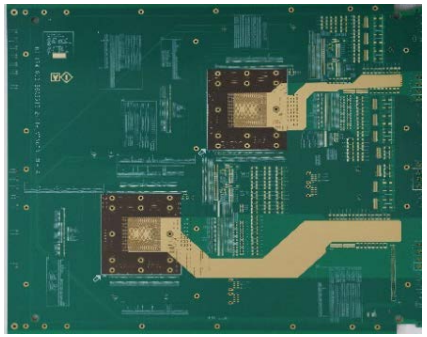
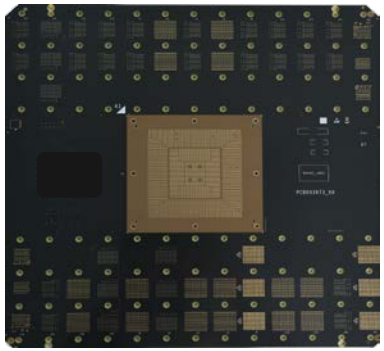
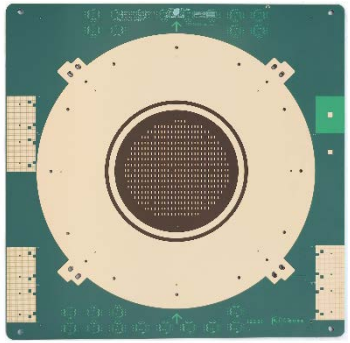
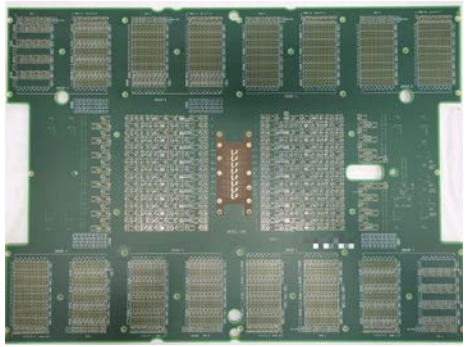
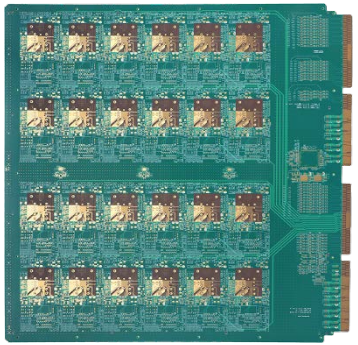
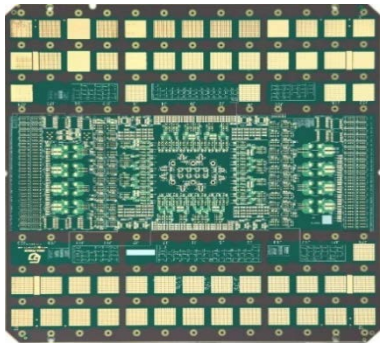
Capabilities

ATE PCB Technology Roadmap

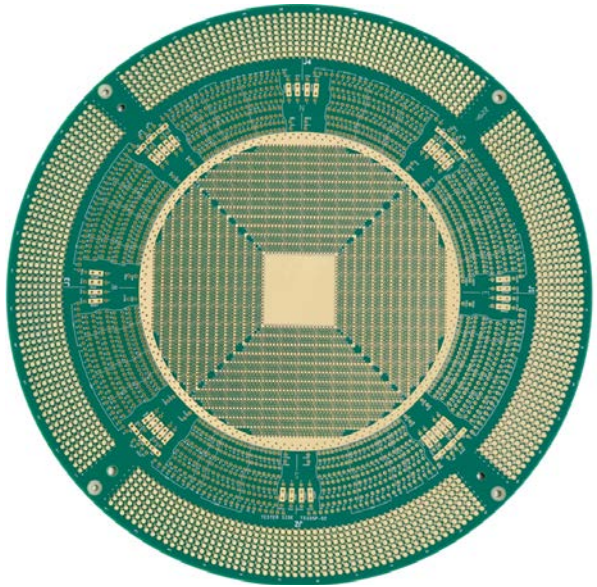
Technology	Characteristic	2025	2026	2027
Board size	Maximum Panel Thickness (mm)	6.5	8.0	10
	Maximum Panel size (inch)	24*28	26*30	26*34
	Finished board size(mm)	571*676	621*726	621*821
	Maximum Layer Count	70	80	100
Registration	Minimum Drill to Copper (mil)	3.1	3.1	2.6
Hole size	Minimum Drill Size (mil)	5	4	4
	Minimum BGA Pitch (mm)	0.35	0.35	0.3
	Hole Size Tolerance (mil)	±2.0 PTH ±1.0 NPTH	±1.5 PTH ±1.0 NPTH	±1.5 PTH ±1.0 NPTH
	Hole Position Tolerance (mil)	±1.0	±1.0	±1.0
	Minimum Stub Length (mil)	6～12	4～8	2～6
Laser via	Via Size (mil)	4~6	3~8	2~10
	build-up	3	5	7
Cu Plating	Maximum Aspect Ratio	42:1	46:1	50:1
Resin Fill	Maximum Aspect Ratio	42:1	46:1	50:1
Surface treatment	ENIG(μm)	Au:0.05~0.07 Ni:3~8	Au:0.05~1.0 Ni:3~8	Au:0.05~1.5 Ni:3~8
	Flash Gold+Hard Gold(μm)	Au:0.05~1.27 Ni:≥3	Au:0.05~1.27 Ni:≥3	Au:0.05~1.27 Ni:≥3
Impedance	Impedance Tolerance (IL)	±5%	±5%	±5%
	Impedance Tolerance (OL)	±10%	±8%	±7%
Flatness	Bow & Twist (%)	0.2%	0.15%	0.1%
	POFV Flatness (mil)	No dimple	No dimple	No dimple
	Range of Flatness at DUT area (μm)	50	40	25
	overall Flatness (μm)	200	150	100

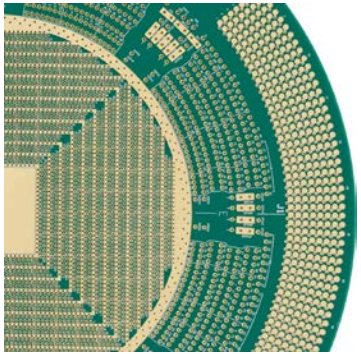
Product Showcase

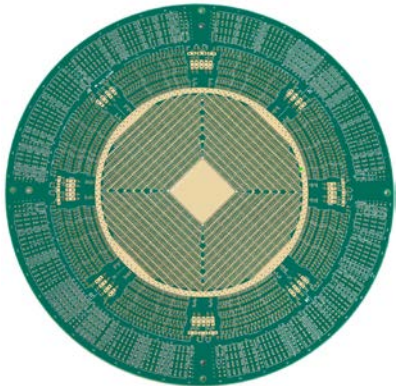
In 2024, Sunshine ATE team successfully shipped 70 Layer PCB, Vertical Probe Cards with DUT flatness ≤50um, Load boards with 0.35mm pitch, and Oversized Burn-in Boards. These technical achievements prove our capabilities are world-class.

Product Showcase



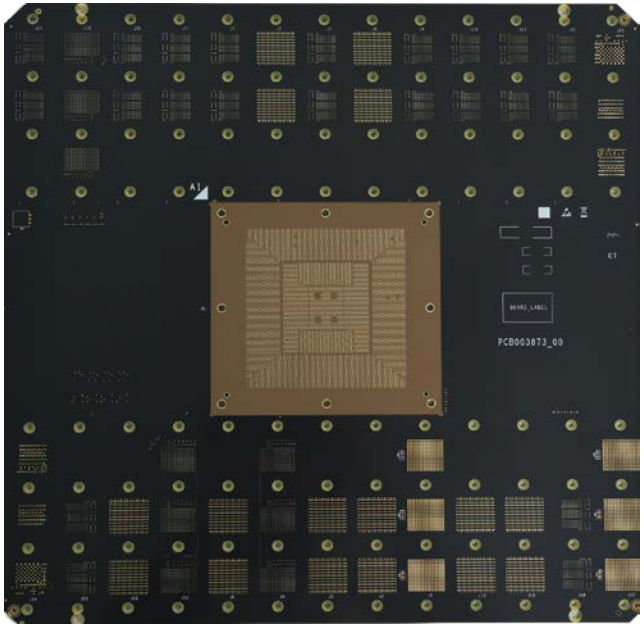


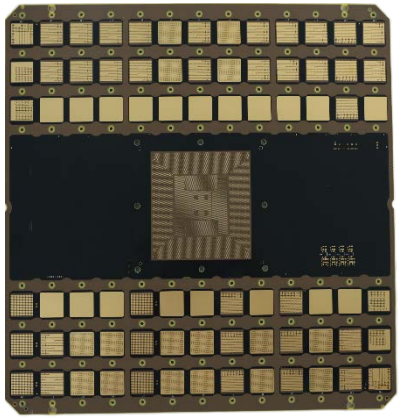


ATE Probe Card

- 52 layers
- HTG FR4
- Via-in-Pad (VIPPO)
- Pitch 0.65mm
- Board Thickness = 0.25”(6.35mm)
- Min. hole size = .010” (0.2mm), Via in Pad
- Aspect Ratio = 32:1
- Drill to Copper = 6.5mil
- Minimum L/S = 0.004”/.003”
- Flash Gold + Selective Hard Gold
- Flatness = ±0.1mm

Product Showcase

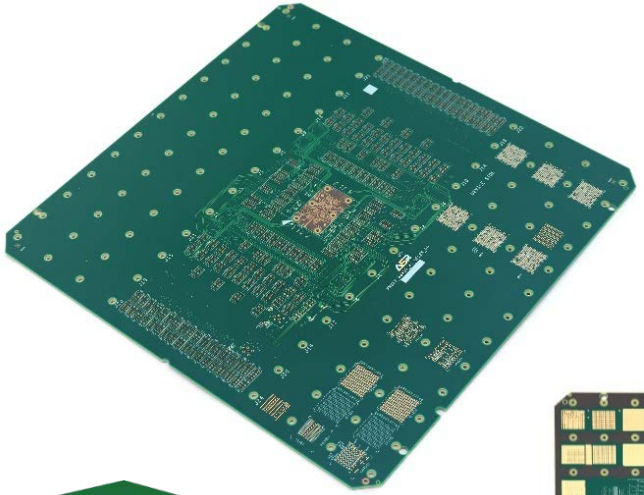


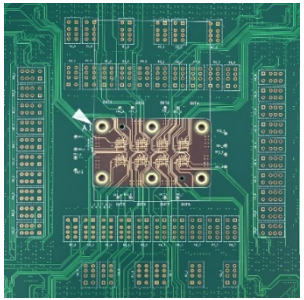


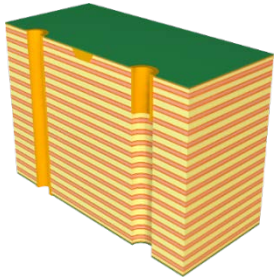
ATE Load Board (TUF)

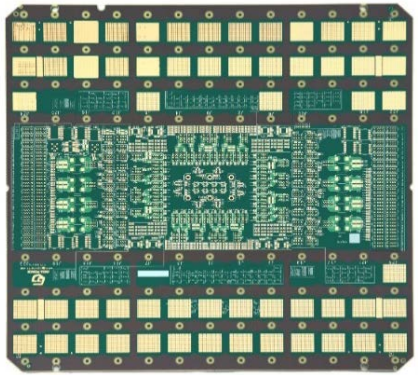
- 18 Layers
- HTG FR4
- Pitch 1.0mm
- Size = 15.87“x15.9” (403 x403mm)
- Board Thickness = .208” (5.3mm)
- Drill/Pad = .010”/.020” (.25 /.5mm)
- Aspect Ratio = 21:1
- Minimum L/S = .005”/.005”
- Flash Gold + Selective Hard Gold
- Via Pad Flatness=0

Product Showcase





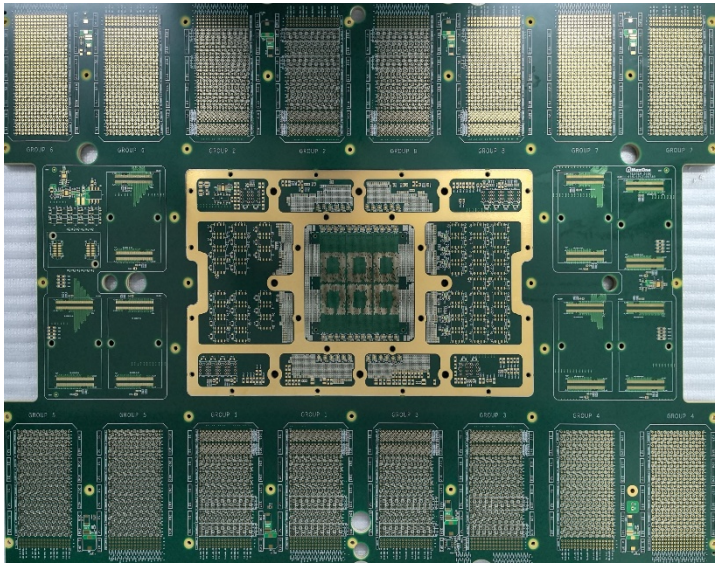


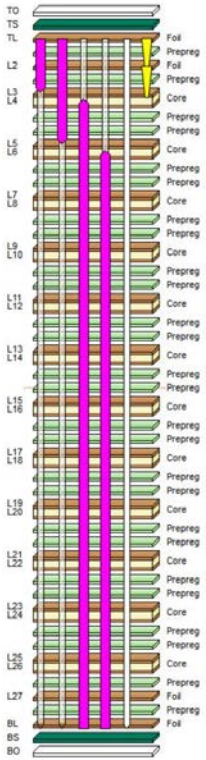


ATE Load Board (TUF)

- 38 Layers
- HTG FR4
- Via-in-Pad (VIPPO)
- Pitch 0.4mm
- Size = 15.87“x15.9” (403 x403mm)
- Board Thickness = .200” (5.08mm)
- Drill/Pad = .005”/.012” (.13 /.3mm)
- Aspect Ratio = 39:1
- Minimum L/S = .0025”/.004”
- Flash Gold + Selective Hard Gold
- Back drilling
- Ultra Flat planarization 75um

Product Showcase

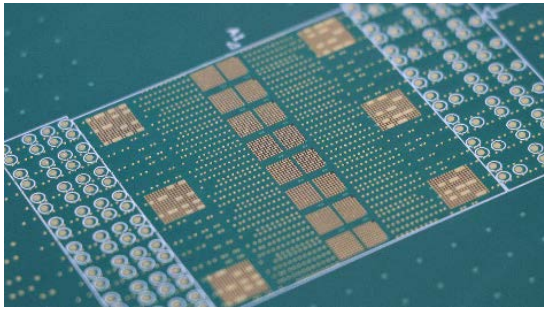


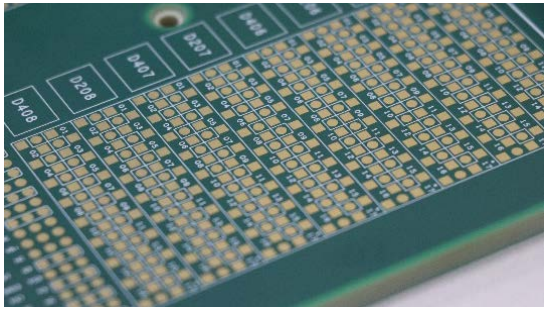


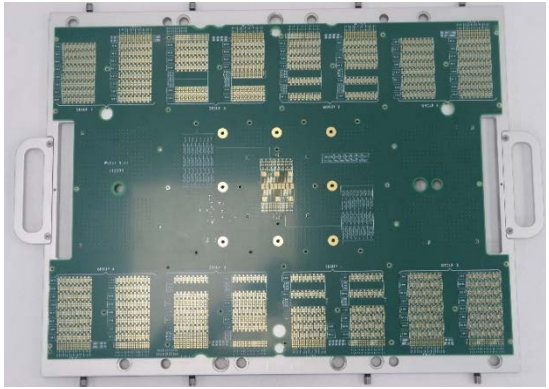
ATE Load Board (V93K full size)

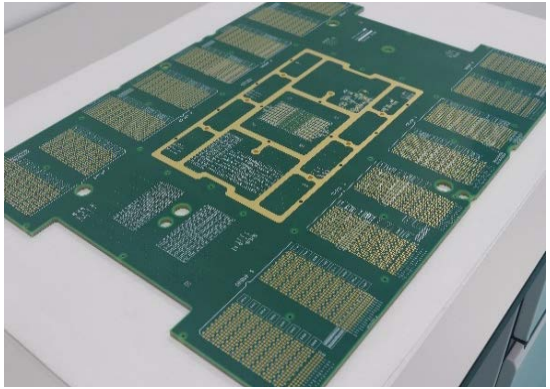
- 28 Layers
- Megtron 6 + HTG FR4
- Pitch 0.35mm
- 2-Step Stacked Laser Via
- Size = 22.9“x16.9” (581x429mm)
- Board Thickness = 0.173” (4.4mm)
- Min. Laser hole size = .004”/0.10mm
- Min. CNC hole size = .005”/0.13mm
- Aspect Ratio = 34:1
- Min. inner hole to trace = 2.8mil
- Minimum L/S = .002”/.004”
- Flash Gold + Selective Hard Gold
- Back drilling
- Warpage 0.15%

Product Showcase





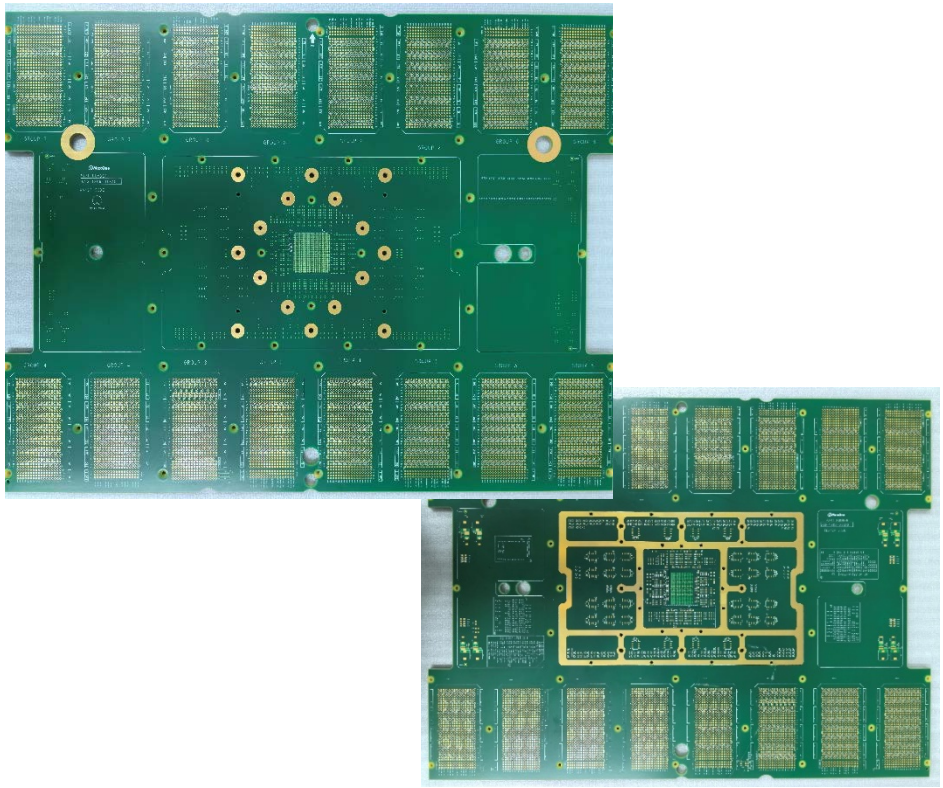




ATE Vertical Probe Card (V93K full size)

- 40 Layers
- HTG FR4
- Pitch 0.4mm
- Via-in-Pad (POFV)
- Size = 22.9“x16.9” (581x429mm)
- Board Thickness = 0.216” (5.5mm)
- Min. hole size = .005”/0.13mm
- Aspect Ratio = 42:1
- Min. inner hole to trace = 3.8mil
- Minimum L/S = .003”/.0065”
- Flash Gold + Selective Hard Gold
- Back drilling
- Warpage 0.15%
- Ultra Flat planarization 50um

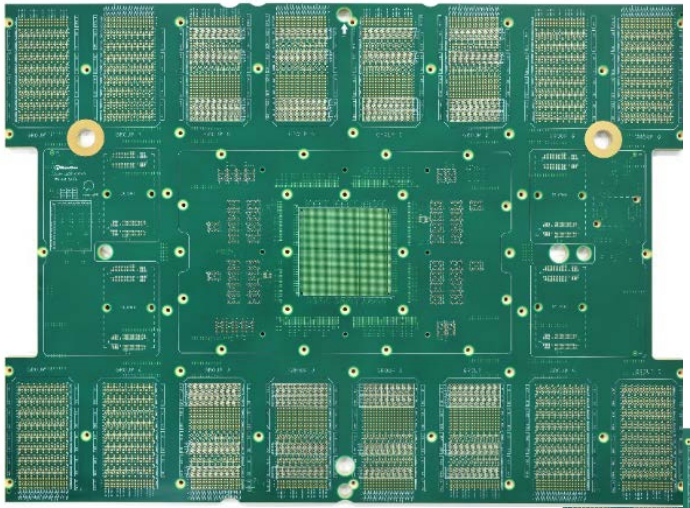
Product Showcase

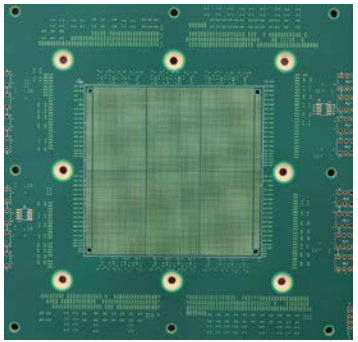


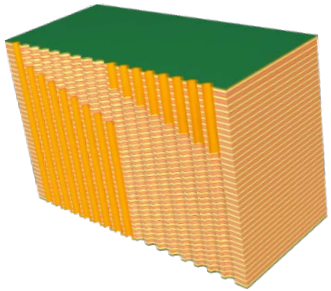
ATE Vertical Probe Card (V93K full size)

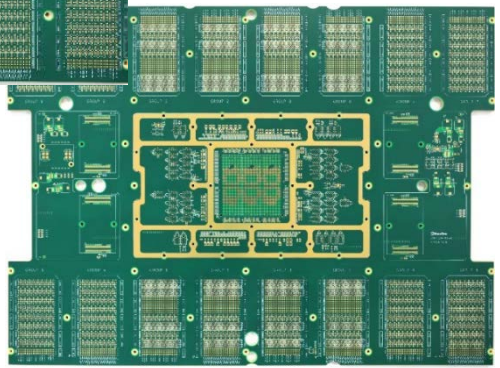
- 56 Layers
- Megtron 6 + HTG FR4
- Via-in-Pad (POFV)
- Pitch 0. 5mm
- Size = 22.9“x16.9” (581x429mm)
- Board Thickness = 0.250” (6.0mm)
- Drill size = .006”(.15 mm)
- Aspect Ratio = 40:1
- Min. inner hole to trace = 5mil
- Minimum L/S = .004”/.008”
- Flash Gold + Selective Hard Gold
- Back drilling
- Warpage 0.15%
- Ultra Flat planarization 50um

Product Showcase





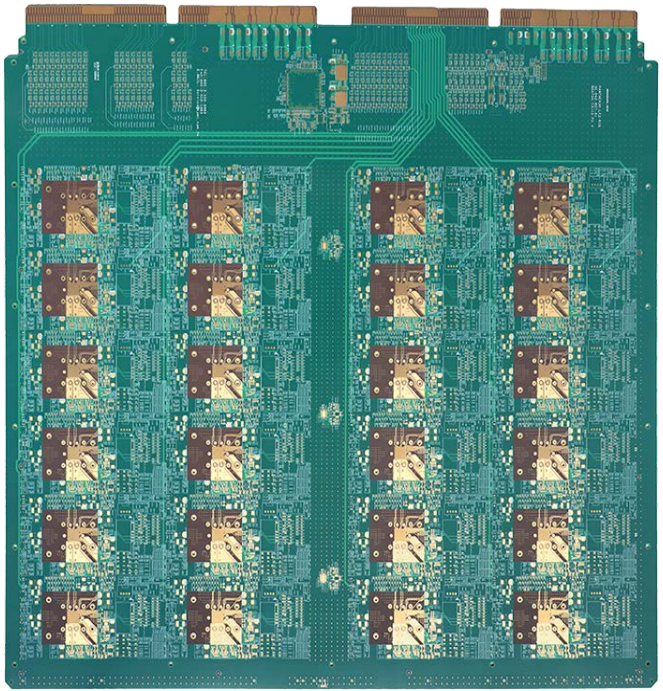


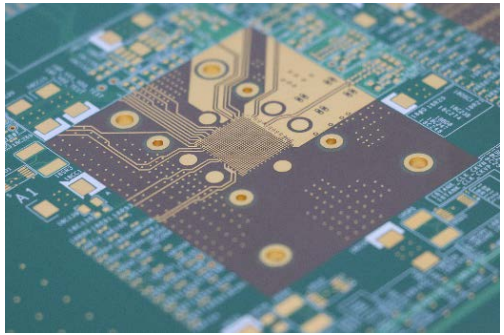


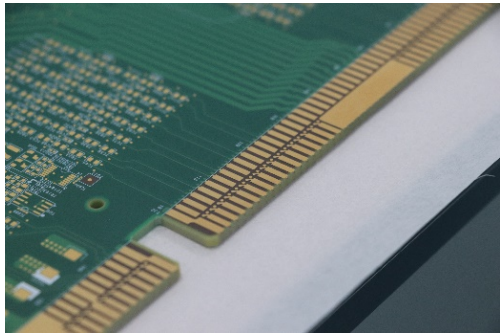
ATE Vertical Probe Card (V93K full size)

- 70 Layers
- Megtron 6
- Via-in-Pad (POFV)
- Pitch 0. 65mm
- Size = 22.9“x16.9” (581x429mm)
- Board Thickness = 0.250” (6.6mm)
- Drill size = .008”(.2 mm)
- Aspect Ratio = 33:1
- Min. inner hole to trace = 6mil
- Minimum L/S = .004”/.008”
- Flash Gold + Selective Hard Gold
- Back drilling
- Warpage 0.15%
- Ultra Flat planarization 75um

Product Showcase



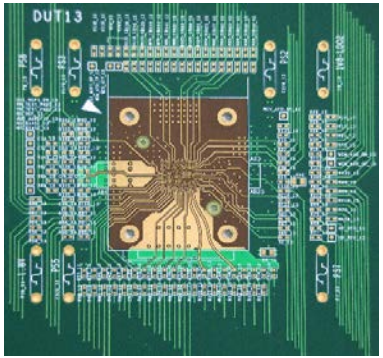




Large Burn-In Board (BIB)

- 20 Layers
- Polyimide
- Pitch 0.40mm
- Size = 24.1”x22.25” (612x565mm)
- Thickness = .087”(2.225mm)
- Min. hole size. = .005” (0.13mm)
- Min. inner hole to trace = 3.8mil
- Minimum Trace = .002”
- Flash Gold + Selective Hard Gold
- Gold Fingers

Product Showcase



Burn-In Board (BIB)

- 14 Layers
- Polyimide
- Pitch 0.35mm
- Size = 22.44”x17.72” (570x450mm)
- Thickness = .079”(2.0mm)
- Min. hole size. = .005” (0.13mm)
- Min. inner hole to trace = 3.0mil
- Minimum Trace = .002”
- Flash Gold + Selective Hard Gold
- Gold Fingers

Cycle Times (estimated)

Process	Description	Cycle Time (CD)	Lead Time (CDs)
General	One cycle lamination, no via fill	7.0	13 ~ 15
Via Fill + POFV	Drill size ≤ 0.15mm, Aspect ratio ≥ 15:1.	+3.0	
DUT via in pad	No dimple	+1.0	
Special Process	Back drill	+0.5	
	High registration accuracy / DUT pitch ≤ 0.5mm	+1.0	
	Encap process	+1.5	
	Via bond process	+3.0	
	Ultra Flat planarization, DUT≤75um	+2.0	
Sequential Lam	Additional lamination cycle = add 3 days per cycle	+3.0	
Order Quantity	Order quantity ≥ 5 = add 2 days	+2.0	
Panel size	Panel size greater than 24″ x 28″ = add 2 days	+2.0	
Expedite (Quick Turn)	For QT, delivery time within 7 days will be reduced by 1 day, and delivery time beyond 7 days will be reduced by 2 days	-1~2	

Thank You.

SALES SUBSIDIARIES:

Sunshine PCB (HK) Co., Limited
Room 706A, Harbour Crystal Centre
100 Granville Road, Tsim Sha Tsui
Kowloon, Hong Kong

Sunshine Circuits USA, LLC
3400 Silverstone Drive, Suite 139
Plano, Texas, USA 75023
Tel. +1 972 867 8886
Fax +1 972 867 8002

Sunshine PCB GmbH
Wildparkstraße 7 D-09247
Chemnitz, Germany
Tel. +49 3722 59967 12

MANUFACTURING LOCATIONS:

Sunshine Global Circuits Co., Ltd.
Bldg B, #32 Nanhuan Road, Shangxing #2 Industrial Zone
Xinqiao, BaoAn, Shenzhen, Guangdong, China 518125
Tel. +86 755 2724 3597
Fax +86 755 2724 3609

Jiujiang Sunshine Circuits Technology Co., Ltd.
GangCheng Rd, ChengXiGang Economic Development Zone,
Jiujiang City, Jiangxi, China 332000
Tel. +86 792 238 5678
Fax +86 792 2385668

Sunshine PCB GmbH
Walter-Freitag -Straße 17 D-42899
Remscheid, Germany
Tel. +49 2191 9573 0

Sunshine PCB (Penang) Sdn. Bhd.
2541 & 2542 Lorong Jelawat 6, Seberang Jaya, 13700 Perai,
Penang, Malaysia
Tel. +60 4 399 0791