SemiQon™

Scaling quantum systems with SemiQon Cryo-CMOS: World's first fully optimized transistor for cryogenic conditions

SemiQon's ultra-low dissipation cryo-CMOS technology integrates qubit control directly with the cryostat. It reduces the need for costly room temperature control electronics infrastructure in quantum computers and makes them less complex and more efficient to operate.

KEY BENEFITS OF OUR SOLUTION TO QUANTUM SYSTEM INTEGRATORS

- 1,000× lower power consumption than traditional control electronics
- 30% infrastructure cost reduction for quantum hardware manufacturers
- In-house manufacturing and packaging: rapid iteration in a semiconductor pilot line foundry as well as expertise in cryogenic packaging

GET IN TOUCH

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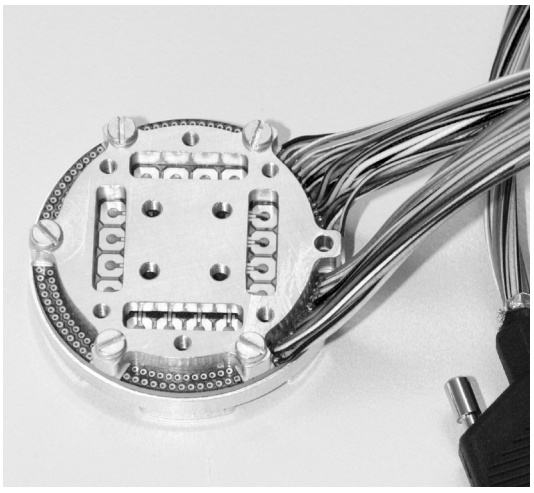
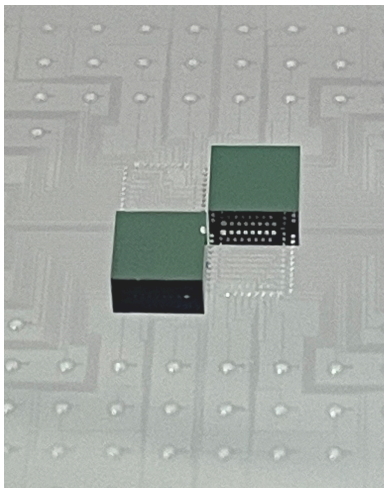
Real, scalable, cryogenic-ready quantum hardware — available now.



PACKAGED CHIP



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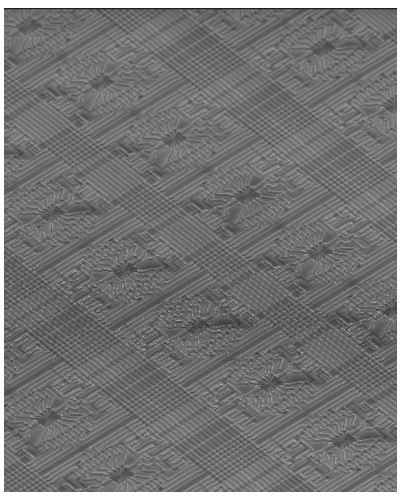


MICROGRAPH OF CMOS DEVICE

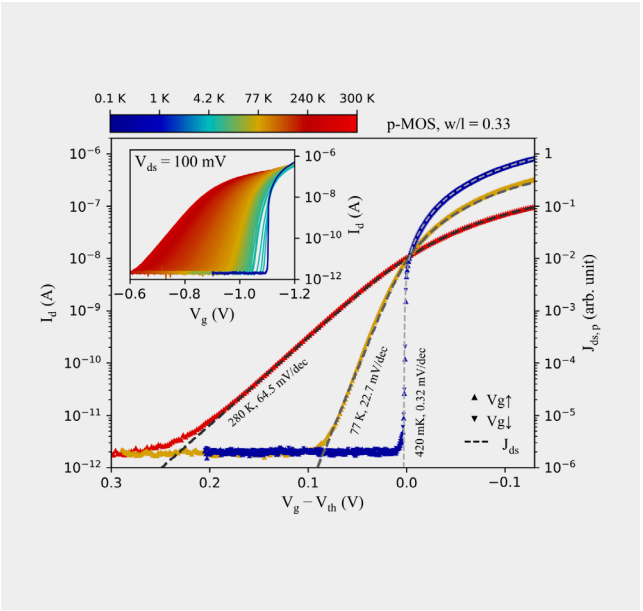
BREAKING THE BOTTLENECKS IN QUANTUM HARDWARE

Quantum computers are expanding, but to be commercially viable, they must become smaller, more efficient, and cost-effective. Control electronics remains the biggest roadblock to scaling quantum systems.

SEMIQON'S CRYO-CMOS TRANSISTORS SOLVE FOUR CRITICAL CHALLENGES

- Input/output limitations: Room-temperature electronics add cost and complexity to quantum processor interfacing
- Power-intensive control electronics limit scalability
- No design kits for cryogenic silicon ICs exist yet
- No practical solution for qubit control using cryogenic silicon ICs exists yet

SemiQon is breaking these barriers with the world's first cryo-CMOS transistors, paving the way for scalable, affordable and sustainable quantum computing.



TECHNICAL SPECIFICATIONS

Technology	Min. subthreshold swing (mV/dec)	Subthreshold gain increase (RT/cryo)	ION increase (cryo/RT)	ΔVth (mV)	Source
SemiQon	0.32	203 x	10 x	Tunable	N. Yurttagül et al. https://arxiv.org/abs/2410.01077 (2024)
14nm FinFET	15	5 x	6 x	80	A. Chabane et al., ESSCIRC 2021 – IEEE 47th European Solid State Circuits Conference (ESSCIRC), Grenoble, France, 2021, pp. 67-70. 10.1109/ESSCIRC53450.2021.9567802
28nm bulk CMOS	20	4 x	—	160	A. Beckers, et al., 47th European Solid-State Device Research Conference (ESSDERC), 2017. 10.1109/ESSDERC.2017.8066592
28nm FDSOI	5	14 x	7 x	Tunable	B. C. Paz et al., 2020 IEEE Symposium on VLSI Technology, Honolulu, HI, USA, 2020, pp. 1–2. 10.1109/VLSITechnology18217.2020.9265034
40nm bulk CMOS	28	3 x	3.5 x	120	R. M. Incandela et al., IEEE J. Electron Devices Soc., vol. 6, 2018. 10.1109/JEDS.2018.2821763
160nm bulk CMOS	23	4 x	3 x	150	R. M. Incandela et al., IEEE J. Electron Devices Soc., vol. 6, 2018. 10.1109/JEDS.2018.2821763
22nm FDX	14	5 x	6 x	Tunable	O. Seidel et al., Fermi laboratory report for DoE, OSTI ID: 2217187. https://www.osti.gov/servlets/purl/2217187/ (2023)

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