Endiya

DEMO Insights Report

India Semiconductor Ecosystem:

From Policy to Execution

Published by Endiya Partners
February 2026

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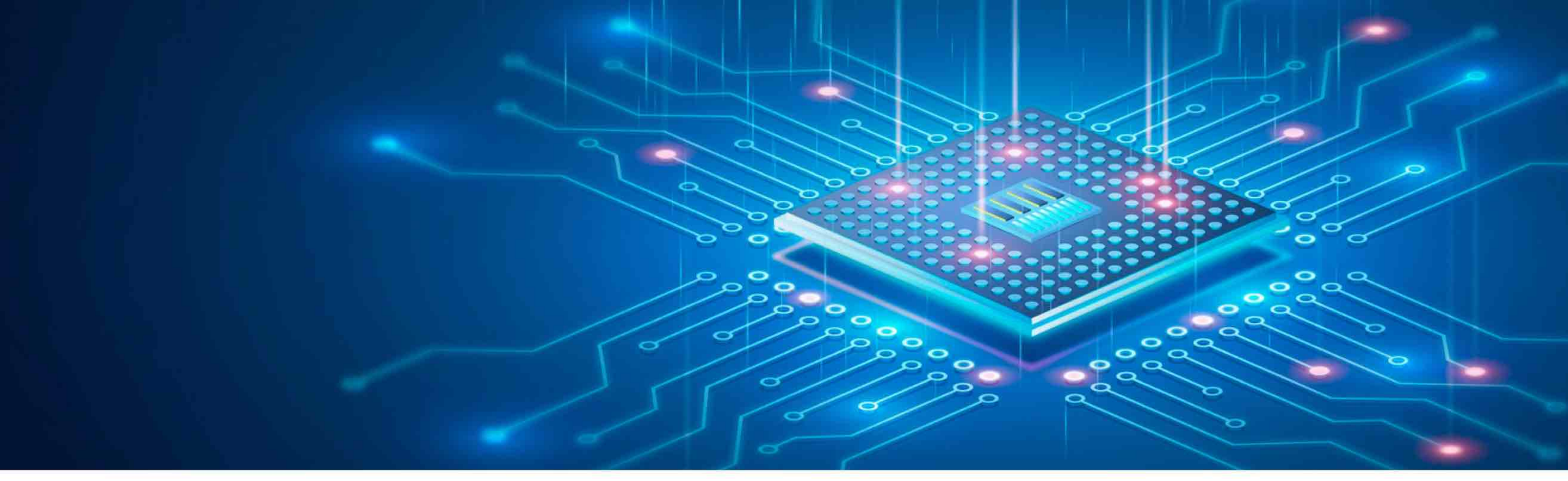
EXECUTIVE BRIEF

India Semiconductor Ecosystem



India's semiconductor journey has reached an inflection point. The announcement of India Semiconductor Mission 2.0 in the Union Budget 2026-27 signals a strategic shift: from building fabs to developing the capabilities that determine competitiveness across equipment, materials, intellectual property, and specialized talent.

The Foundation: ISM 1.0 Delivers Infrastructure

Since December 2021, India has mobilized Rs 1.6 lakh crore (~$18 billion) in private investment through the Semiconductor Mission's Rs 76,000 crore (~$8.4 billion) incentive outlay. Ten approved projects now span fabrication, assembly and testing, and compound semiconductors across six states.

The tangible progress: Tata Electronics' Dholera fab, India's first commercial-scale silicon foundry is targeting first production in Q4 2026. Micron's Sanand facility is expected to commence commercial production in February 2026.

The Strategic Pivot: ISM 2.0 Addresses Missing Pieces

ISM 2.0's Rs 1,000 crore (~$111 million) allocation for FY 2026-27 tackles systemic gaps that fabrication alone can't solve. Over 90% of semiconductor equipment, chemicals, and materials are currently imported. Critical design IP in analog, RF, and compute domains remains absent. A projected talent deficit of 10,000-13,000 manufacturing professionals looms by 2027.

Union Minister Ashwini Vaishnaw has been explicit: design companies and startups are the "topmost priority" of ISM 2.0. This reflects operational reality that fabs require indigenous IP, equipment maintenance capabilities, and process expertise to achieve competitive yields.

ISM 2.0 is also an implicit course correction. The manufacturing-first strategy assumed global supply chains would localize organically; they have not. Equipment vendors and materials suppliers require demand certainty that ISM 1.0 did not fully address.

The Opportunity Redefined

India's domestic semiconductor market is expected to double from $52 billion in 2024 to $103 billion by 2030 driven by AI infrastructure, electric mobility, defense modernization, and connectivity needs. The AI infrastructure build-out plan is unprecedented: data center capacity is expected to explode from ~1.5GW to 9 GW by 2030. The IndiaAI Mission has deployed 38,000 GPUs against an original 10,000 target .

This is not abstract market growth. Geopolitical supply chain restructuring, driven by CHIPS Act constraints on China, creates a specific window for India's mature node capacity. The AI build-out requires exactly the analog, power, and memory chips that India's first fabs will produce.

The venture opportunity is shifting from application-specific chip companies to horizontal ecosystem infrastructure: design automation, manufacturing intelligence, specialized IP, and productivity software serving multiple segments.

Endiya's Conviction

Our semiconductor portfolio reflects a focused thesis: Horizontal productivity infrastructure offers better risk-adjusted returns at an early stage than fabless chip design.

Maieutic Semiconductors addresses analog and mixed-signal IC design productivity through AI-enabled automation, directly aligned with ISM 2.0's priorities. ThirdAI Automation provides manufacturing intelligence and RCA for fabs, positioned to serve India's ten approved facilities as they scale from construction to operations.

This thesis predates ISM 2.0, but the policy evolution validates it. As India moves from "will we build fabs?" to "can we operate them competitively?", the ecosystem needs design tools, manufacturing AI, and productivity software more urgently than another application-specific chip startup competing for limited foundry allocation.

Execution discipline, not policy announcements, will determine outcomes. The next 18 months will reveal whether India can convert infrastructure momentum into operational credibility.

KEY MILESTONES

Phase 1 - ISM 1.0

Focus: Building physical infrastructure

Key Allocation: ₹76K crore (~$8.4B) incentive framework (up to 50% fiscal support).

2021-2022
Launch of ISM 1.0.

2022-2023
10 projects approved, mobilizing ₹1.6 lakh crore (~$17.8B) private investment across 6 states

2024-2025
Construction milestones (e.g., Tata Dholera fab underway; CG Power-Renesas G1 pilot operational Aug 2025).

Transition Phase

2025-2026
Shift from "building presence" to "deepening capabilities.
Union Budget 2026-27 launches ISM 2.0 with ₹1,000 crore (~$111M) allocation for FY 2026-27.

Phase 2 - ISM 2.0

Focus: Deeper capabilities

Key Allocation: ₹1K crore for targeted interventions; complements schemes (₹40K crore)

2026-Q1
Design companies/startups prioritized; indigenous IP development ramps up (analog/RF/compute).

2026-Q2 & Q3
Equipment/materials localization pilots (>90% currently imported); talent programs address 10k–13k manufacturing deficit.

2026-Q4
Tata Dholera first production; yield/quality benchmarks; customer adoption starts.

2027 onwards
Full-stack IP readiness; progress toward 3nm/2nm by 2035; reduced supply chain vulnerability; Series B funding for DLI startups.

ISM 2.0:

WHAT CHANGED AND WHY IT MATTERS

ISM 1.0: Building Physical Infrastructure

The India Semiconductor Mission launched in December 2021 with Rs 76,000 crore (~$8.4 billion) in incentives offering up to 50% fiscal support for fabrication, assembly, testing, and design projects. The results: ten approved projects mobilizing Rs 1.6 lakh crore (~$18 billion) in private investment.

Key ISM 1.0 Approvals:

Silicon Fabrication

- Tata Electronics-PSMC (Taiwan): Rs 91,000 crore (~$10.1B), 50,000 wafers per month capacity, Dholera Gujarat, 28nm-110nm nodes, first production Q4 2026

Compound Semiconductors (SiC/GaN)

- SiCSem-Clas-SiC (UK partnership): Rs 2,067 crore (~$230M), commercial SiC fab, Bhubaneswar Odisha, for EVs and power electronics, operational target 2027-28
- RIR Power Electronics: Rs 618 crore (~$69M), SiC MOSFETs and diodes (3.3kV-20kV), Bhubaneswar

OSAT (Assembly, Testing, Packaging)

- CG Power-Renesas-Stars Microelectronics: Rs 7,600 crore (~$44M), Sanand Gujarat. G1 pilot operational since August 2025 (0.5M units/day), commercial production 2026, G2 under construction (14.5M units/day)
- Tata OSAT: Rs 27,000 crore (~$3B), Morigaon Assam, under construction, commissioning target April 2026, 48 million chips per day capacity
- Micron Technology: $2.5 billion (Rs 22,516 crore), Sanand Gujarat, advanced testing and packaging, commercial production expected to commence in February 2026, 14 million units per week capacity

Display Fabs

- HCL-Foxconn: Display driver chips, Rs 3,706 crore (~$412M), Jewar UP, 20,000 wafers per month capacity. Production target 2027

Design Ecosystem The Design Linked Incentive (DLI) scheme sanctioned 23 chip design projects with Rs 803 crore (~$89M) outlay. Today, 278 academic institutions and 72 startups have access to industry-grade Electronic Design Automation tools. Six companies completed prototype tape-outs at international foundries. Twenty chip designs from 17 institutions were fabricated at SCL Mohali.

ISM 2.0: Building Capabilities That Matter

The Union Budget 2026-27 announcement of ISM 2.0 with Rs 1,000 crore (~$111 million) for FY 2026-27 reflects policy maturation. Four pillars define the focus:

Equipment and Materials Production Currently, over 90% of semiconductor manufacturing equipment, specialty chemicals, gases, and materials are imported. ISM 2.0 prioritizes domestic production of manufacturing equipment, metrology tools, specialty chemicals (photoresists, etchants), high-purity materials, and testing equipment. This addresses supply chain vulnerability and creates localization opportunities.

Full-Stack Indian IP Development Despite employing 150,000+ design engineers (20% of global workforce), India lacks indigenous IP in critical areas: analog and mixed-signal IP (converters, PLLs, power management), RF and wireless IP (5G/6G, connectivity), and compute IP (processors, accelerators, memory controllers).
Minister Vaishnaw's emphasis on design companies as ISM 2.0's "topmost priority" aims to create companies that can "design a product, take it to market, become the next Qualcomm from India." Strong rhetoric, but the real test is commercial validation.

Supply Chain Resilience Strengthening both domestic and global semiconductor supply chains through diversified sourcing, expanded domestic ATMP infrastructure, testing and validation facilities, and certification frameworks for Indian-designed chips.

Industry-Led R&D and Training Centers Targeted funding for industry-led research centers advancing toward 3nm and 2nm nodes by 2035, specialized training for manufacturing professionals, and collaboration platforms between academia, startups, and industry.

Why This Matters

ISM 2.0 acknowledges that fabs need more than construction budgets. They need equipment, materials, process know-how, specialized talent, and domestic IP to operate competitively. The shift from Rs 76,000 crore for fabrication (ISM 1.0) to Rs 1,000 crore for capabilities (ISM 2.0) signals focused intervention rather than broad subsidies.

Investor Implication

ISM 2.0's focus creates opportunities with better venture economics: design automation and productivity tools (shorter development cycles, multiple customers, recurring revenue), manufacturing intelligence and yield optimization (software-driven, horizontal deployment), specialized IP with licensing models (lower capital than full chip development), and equipment and materials localization (addressable with patient capital).

The policy evolution mirrors the ecosystem maturation required: from announcing projects to executing reliably, from importing solutions to building indigenous capability, from policy momentum to commercial credibility.

ISM 1.0 (Dec 2021–2025)		ISM 2.0 (2026+)
Building physical infrastructure (fabs, OSAT, compound semi, display, basic design).	Primary Focus	Deepening capabilities (equipment/materials, full-stack IP, supply chain resilience, R&D/training).
₹76,000 crore (~$8.4B) incentive framework; mobilized ₹1.6 lakh crore (~$17.8B) private investment.	Allocation	₹1,000 crore (~$111M) for FY 2026-27; targeted + complements broader schemes (e.g., ₹40,000 crore for components).
Attracting large-scale manufacturing projects (10 approved across 6 states).	Top Priority	Design companies/startups; indigenous IP (analog/RF/compute); "topmost priority" per Minister Vaishnaw.
Project approvals, investment mobilization, construction milestones (e.g., Tata Dholera Q4 2026 production); 23 DLI projects.	Success Metric	Commercial viability: Localization (>90% import reduction), yield/quality, talent retention, 3nm/2nm readiness by 2035.

Based on Union Budget 2026-27 and PIB releases

ECOSYSTEM SNAPSHOT

Fabrication & OSAT Infrastructure

Segment	Company/ Partnership	Investment	Scope	Location	Status	Timeline
Silicon Fab	Tata Electronics-PSMC	Rs 91,000 Cr (~$10.1B)	50,000 wafers/month, 28nm-110nm	Dholera, Gujarat	Construction underway	First commercialisation Q4 2026*
Compound Semi	SiCSem-Clas-SiC (UK)	Rs 2,067 Cr (~$230M)	60,000 SiC wafers / yr with packaging for 96 million units	Bhubaneswar, Odisha	Groundbreaking Nov 2025	2027-28
Compound Semi	RIR Power Electronics	Rs 618 Cr (~$69M)		Bhubaneswar, Odisha	Under development	TBD
OSAT	CG Power-Renesas-Stars	Rs 7,600 Cr (~$844M)	G1: 0.5M units/day	Sanand, Gujarat	G1 operational Aug 2025, G2 under construction	Commercial 2026
OSAT	Tata OSAT	Rs 27,000 Cr (~$3.1B)	48 million chips per day capacity	Morigaon, Assam	Under construction	April 2026
OSAT	Micron Technology	$2.5B (Rs 22,516 Cr)	14 million units per week capacity	Sanand, Gujarat	Operational	Feb 2026
Display	HCL-Foxconn	Rs 3,706 Cr (~$430M)	20K wafers/month, 36M chips/month	Jewar, UP	Under development	2027

Global Players & Design Centers

India has emerged as a critical node in global semiconductor design, with 95+ Global Capability Centers employing 150,000+ design engineers (~20% of global design workforce).

Company	Investment/ Milestone	Focus	Significance
AMD	Expanding Presence. $400M (2023-2028)	India as largest AMD design center	Major GCC investment
Qualcomm	2nm chip tape-out (Feb 2026)	Advanced node co-development	India is 2nd largest design base
Intel	Expanding presence	AI chips, data center, IoT	Design and engineering R&D
ARM	Bengaluru center opened	Processor architecture, IP	Chip design capabilities
Texas Instruments	Bengaluru R&D (Feb 2026)	Analog, embedded processing	Product development
NVIDIA	Active presence	GPUs, AI computing	AI semiconductor development
Broadcom	Strong R&D team	5G, Wi-Fi, optical, IoT	Connectivity solutions

Funded Indian Startups (>$3M raised, 2023-2026)

Company	Funding	Focus	Stage	Key Milestone
Netrasemi	Rs 107 Cr (~$12.5M) Series A (Jul 2025)	Edge AI vision SoCs	Pre-commercial	Two SoCs in tape-out
Mindgrove	$8M Series A (Dec 2024)	Secure IoT SoCs (RISC-V)	Early revenue	Secure IoT chip launched May 2024
Morphing Machines	~$7.1M total (Seed $2.76M, 2023 + Series A ~$4.32M, 2025)	Reconfigurable processor IP	Pre-silicon	REDEFINE architecture
Maieutic	$6M Seed (2025)	Analog IC design automation	Development	AI-assisted analog, mixed-signal, and RF design productivity platform
FermionIC	$6M reported (2024)	High-speed wireline/RF IP	Development	SERDES and RF IC dev
AGNIT	$4.87M total (incl. $3.5M seed, 2024)	GaN devices	Development	Defense/telecom validation underway
InCore	$3M Seed (May 2023)	RISC-V processor IP	Early revenue	SoC generator platform
ThirdAI	$3M Seed (Feb 2026, Endiya + Capria)	Fab manufacturing intelligence	Development	RCA platform for fabs
Saankhya Labs	$13M disclosed round (Mar 2019)	SDR and wireless chipsets	Revenue stage	DLI-approved; acquired by Tejas Networks

Total 2025 semiconductor startup funding: ~$50M (up from $28M in 2024, $5M in 2023)

DLI Scheme Progress

Twenty-three chip design projects sanctioned with Rs 803 crore (~$89M) outlay. 278 academic institutions and 72 startups now have EDA tool access. Six companies completed prototype tape-outs at international foundries. Twenty chip designs from 17 institutions were fabricated at SCL Mohali. Ten startups secured venture capital funding.

Applications span: Surveillance SoCs, smart energy meters, networking chips, motor control for EVs and drones, space-grade systems for ISRO, RF and wireless IP, secure hardware platforms.

Critical Ecosystem Gaps:

- **Analog and Mixed-Signal IP:** Limited indigenous capability in converters, PLLs, power management (essential for automotive, industrial, IoT applications).

- **Manufacturing Intelligence:** As fabs scale from pilot to volume, yield optimization and manufacturing AI become crucial. Few domestic solutions exist.

- **Equipment and Materials:** Over 90% imported. Localization opportunities in metrology, testing equipment, specialty chemicals, high-purity materials.

- **Business Talent:** Design engineers are abundant. Product managers, applications engineers, sales specialists who understand both technology and markets remain scarce.

THE CAPITAL REALITY

Funding Trajectory: Growth Within Constraints

Indian semiconductor startups raised approximately $50 million in 2025, up from $28 million in 2024 and $5 million in 2023. This 10x growth over three years shows increasing investor confidence, but remains modest relative to capital requirements and global comparables.

Recent Funding Rounds (2023-2025):

- **Netrasemi:** $12.5M Series A (July 2025)
- **Mindgrove:** $8M Series A (December 2024)
- **Morphing Machines:** ~$7.1M total (Seed 2023 + Series A 2025)
- **Maieutic:** $6M Seed (2025)
- **FermionIC:** $6M reported round (2024)
- **AGNIT:** $4.87M total (2021–2024)
- **InCore:** $3M Seed (May 2023)
- **ThirdAI:** $3M Seed (February 2026)

Active Investors:

Endiya Partners, Peak XV Partners (formerly Sequoia India), Zoho Corporation, Speciale Invest, Unicorn India Ventures, 3one4 Capital, Zephyr Peacock, Bessemer Venture Partners

Why Venture Capital Remains Limited

Government support and market opportunity haven't translated to proportional VC funding. Structural constraints persist.

Capital Intensity vs. Fund Economics

Fabless chip design requires $5-15M to first silicon, plus additional capital for scaling. Equipment and materials companies need $10-25M+ for commercial validation. VC funds typically deploy $2-5M at seed/Series A. The math doesn't work for most semiconductor plays.

Extended Timelines vs. Fund Horizons

Chip design takes 3-5 years minimum from concept to production. Customer qualification, especially for automotive, adds 18-36 months post-product. VC funds operate on 5-7 year investment periods with 10-year fund lives. Semiconductor timelines exceed typical return windows.

Technical Risk and Validation Challenges

First silicon failure rates are significant. Generalist VCs struggle to assess technical risk. Customer validation requires long qualification cycles. Exit comparables are limited. Steradian's acquisition by Renesas stands out precisely because it's rare.

Team and Talent Constraints

Senior semiconductor entrepreneurs are scarce in India. Experienced engineers prefer stable, high-paying roles at global chipmakers over startup risk. Business development and go-to-market expertise is rare. Multi-disciplinary teams combining design, manufacturing, and business capabilities are hard to assemble.

Market Access Barriers

Global customers have established supplier relationships. Indian startups face credibility challenges despite technical capability. The domestic market is price-sensitive. Global markets require extensive validation. OEMs need second-source guarantees that startups can't provide.

What Works: Capital-Efficient Segments

Funding patterns and investment experience point to segments with better venture economics:

Design Automation and Productivity Tools

Shorter development cycles (18-24 months vs. 3-4 years for chips). Horizontal platforms serving multiple customers without custom chip design. Recurring revenue potential through SaaS licensing. Lower capital requirements ($2-5M to launch vs. $10-15M to first silicon). Example: Maieutic's analog IC design automation.

Manufacturing Intelligence and Software

Software-driven solutions for fab operations, yield optimization, quality control. Deployable across multiple facilities (ten approved fabs/OSATs in India). Faster time-to-revenue than hardware. Scales without proportional capital increase. Example: ThirdAI's fab manufacturing intelligence.

Specialized IP with Licensing Models

IP blocks licensable to multiple chip companies. Lower capital than full chip development. Proven monetization through royalties and licensing fees. Requires strong technical differentiation and customer validation.

Application-Specific Chips (Highly Selective)

Viable when exceptional technical differentiation, strong customer pull pre-funding, hybrid founder teams (technical plus commercial), strategic co-investment from customers. The bar is high. Most VC-backed chip companies struggle with customer acquisition and follow-on funding.

Alternative Capital Sources

Comprehensive semiconductor ecosystem development requires capital beyond venture:

- **Strategic Corporate Investment:** Global semiconductor companies investing in Indian IP and design houses. Indian conglomerates (Tata, Murugappa, Zoho) backing ecosystem plays. Joint ventures with technology transfer (Tata-PSMC, CG-Renesas models).

- **Government and Development Finance:** DLI scheme providing non-dilutive development support. India Deep Tech Investment Alliance ($1 billion commitment from insurers, pension funds). State-level venture funds with longer horizons.

- **Patient Private Capital:** Family offices with 10+ year horizons. Sector-focused funds. Hybrid debt-equity structures for revenue-stage companies.

Endiya's Framework

We evaluate semiconductor opportunities against several criteria: Does the technology solve a real bottleneck with clear customer pain? Do founders combine technical depth with commercial thinking? Can capital needs be sequenced intelligently across milestones? Is there a focused beachhead market rather than "we'll sell to everyone"?

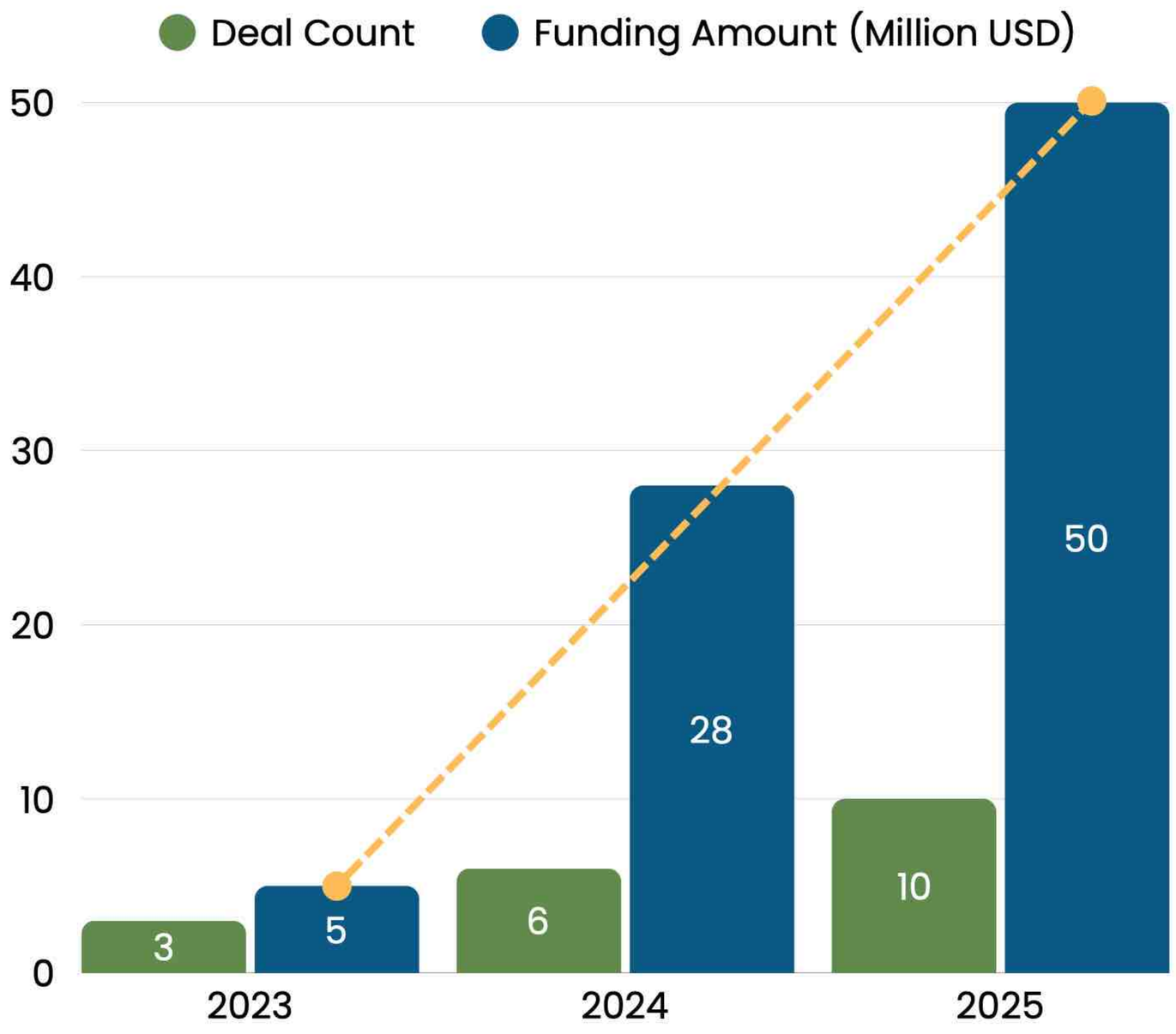
Current Portfolio:

- **Maieutic:** Analog IC design automation addressing productivity bottlenecks as India scales design activity and ISM 2.0 prioritizes indigenous analog IP

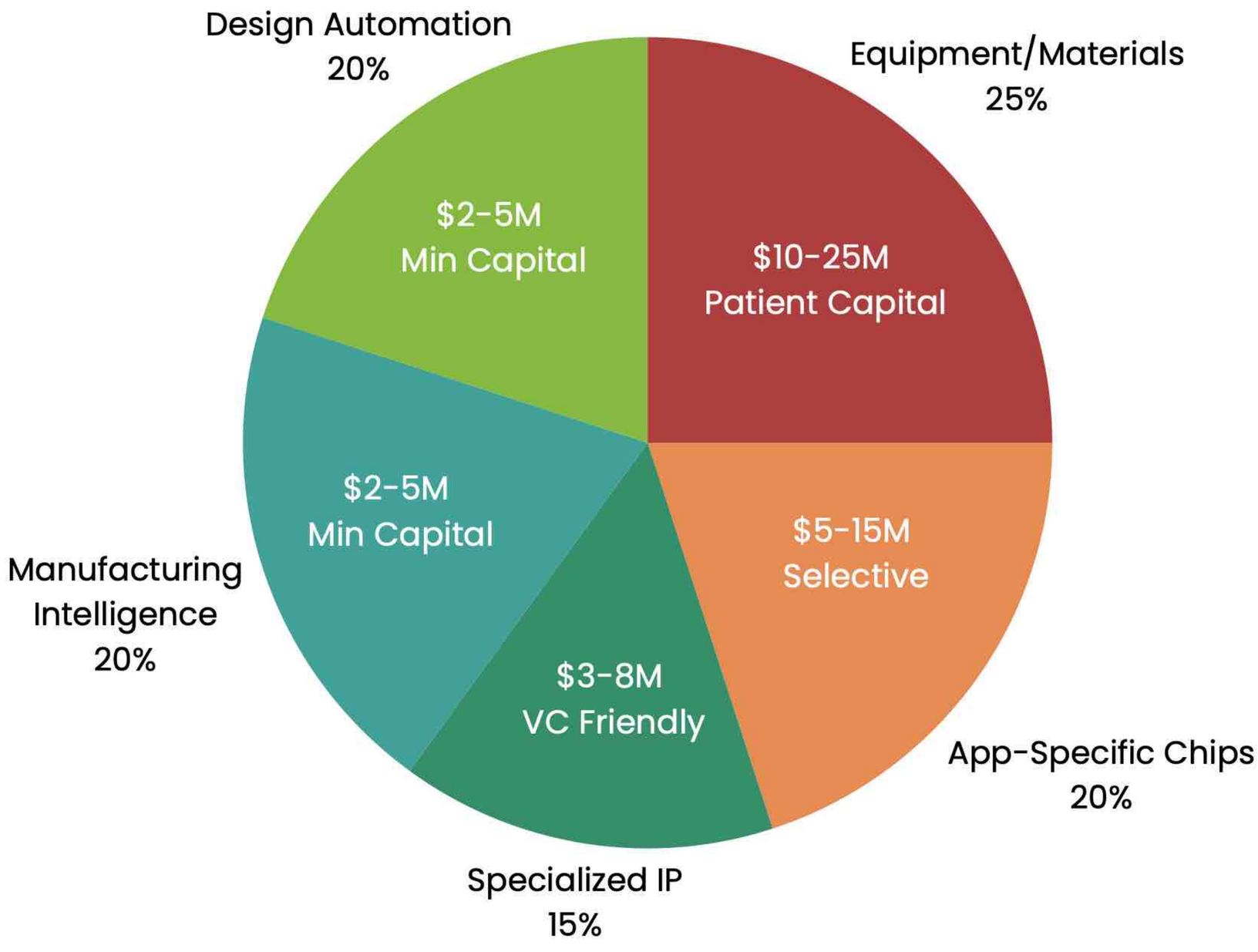
- **ThirdAI:** Fab manufacturing intelligence and yield optimization serving India's ten approved facilities as they transition from construction to operations

Our thesis: horizontal productivity infrastructure offers superior risk-adjusted returns at early stage compared to fabless chip design companies, while building defensible IP moats where India has structural design talent advantages.

Funding Growth



Capital Requirements by Segment



THE NEXT 18 MONTHS

WHAT TO WATCH

Critical Milestones (Q1 2026 through Q2 2027)

Q4 2026 Tata Fab First Production The most visible test of execution capability. Minister Vaishnaw has stated first chips from Dholera will arrive in December 2026. Success requires more than producing chips. Achieving target yields on 28nm/40nm nodes within 6-12 months of startup determines economic viability and customer confidence. Persistent yield issues or significant delays damage credibility for India's broader semiconductor ambitions.

2026-2027 Commercial Validation of DLI Startups Can the 23 DLI-supported startups transition from tape-out to commercial revenue? The gap between "chip designed" and "chip deployed in commercial product" is enormous. Watch for: 5-10 DLI companies achieving first customer revenue, venture-backed startups (Mindgrove, Netrasemi, InCore) securing Series B funding based on traction, reference design wins and anchor customer announcements, distinction between prototype validation versus volume production commitments.

2026 OSAT Facilities Scale to Volume CG Power Sanand scaling from pilot (0.5M units/day) to commercial targets (14.5M units/day with G2). Tata OSAT Assam becoming operational. Both demonstrating competitive quality, turnaround times, and pricing versus established regional hubs in Malaysia and Vietnam.

2027 Talent Retention Test Tata is sending hundreds of engineers to Taiwan for intensive training at PSMC facilities. Will trained professionals return and remain in India's semiconductor ecosystem? Or does this create brain drain to Taiwan, US, and Europe as individuals gain globally marketable experience? Retention rates determine whether India can sustain semiconductor operations long-term.

2026-2027 Customer Adoption Signals Policy support doesn't guarantee customer acceptance. Watch for: global OEMs (automotive, industrial, telecom) qualifying Indian fabs as approved sources, tier-1 suppliers adopting Indian-designed IP in production systems, multi-year supply agreements (not just pilot orders), Indian chips specified in commercial products globally.

What Success Looks Like:

Minimum Viable Success (by mid-2027): Tata fab operational and ramping yield toward targets. At least one OSAT facility at volume production with global customers. Three to five DLI startups with commercial revenue (even if modest). Semiconductor startup funding exceeding $100M annually. Twenty-five percent reduction in projected talent gap.

Strong Success (by mid-2027): Tata fab achieving over 70% of target yields on mature nodes. Multiple OSATs operational with capacity utilization above 50%. Ten-plus startups with commercial traction, two to three raising Series B rounds. Indian-designed chips in commercial products (consumer electronics, automotive). Equipment and materials localization projects underway with private sector participation.

Transformational Success (by mid-2027): India demonstrating advanced node (12nm/7nm) design capability at scale. Compound semiconductor production serving domestic EV and renewable markets with volume. One or more Indian semiconductor startups achieving unicorn valuation. Major global OEM committing to India as primary source for specific chip categories. ISM 2.0 equipment and materials ecosystem showing tangible commercial progress.

Risks to Outlook:

Execution: Infrastructure challenges (power, water reliability) delaying fab operations. Yield and quality issues damaging credibility. Talent shortages constraining scale despite training investments.

Market: Global semiconductor downcycle reducing demand and investment. Geopolitical tensions disrupting partnerships or market access. Customer reluctance to qualify new suppliers given established relationships.

Competitive: Vietnam and Malaysia offering better execution on OSAT and testing. China's rapid mature-node capacity expansion creates pricing pressure. Advanced node technology remains inaccessible despite policy support.

Capital: Venture funding not scaling to meet startup needs. Exit opportunities remaining limited, discouraging follow-on investment. Government support not translating to commercial viability for startups.

Endiya's View: Execution Separates Reality from Narrative

The critical question is no longer whether chips are produced, but whether facilities achieve economically viable yields within credible ramp timelines. First silicon without yield stability is a milestone; sustained yield performance is validation.

Similarly, ecosystem success will be measured not by additional tape-outs, but by commercial adoption. The transition of DLI-supported startups from prototype development to repeat customer revenue represents the real inflection point.

Talent dynamics form the third execution test. Training programs build capability; retention sustains ecosystems. Whether India can retain highly skilled manufacturing and design talent as global mobility increases will materially influence long-term competitiveness.

Over the next 18 months, India's semiconductor trajectory will be defined by a small set of outcome metrics:

- Yield performance over chip announcements
- Customer adoption over prototype activity
- Talent retention over training scale
- Commercial revenue over policy approvals

India's semiconductor ecosystem is now transitioning from a policy-driven phase to an execution-driven one. For both operators and investors, recognizing this shift, and aligning expectations accordingly, will determine value creation over the coming decade.

ABOUT US

Endiya Partners is an early-stage venture capital firm backing IP-driven product companies in AI, Deep Tech, and Healthcare & Life Sciences. Founded in 2015 and headquartered in Hyderabad, the firm leads Pre-Series A and select Series A rounds where technical depth matters. Endiya is currently investing from Fund III.

Notable exits include Darwinbox (seed to unicorn), Steradian Semiconductors (acquired by Renesas Electronics), and ShieldSquare (acquired by Radware). Kissht, a digital lending platform backed from seed stage, received SEBI approval for its IPO in January 2025 and is preparing for public listing.

In semiconductors, Endiya has backed companies across the design and manufacturing value chain. Steradian Semiconductors pioneered mmWave radar chip design before its acquisition by Renesas. Maieutic is building AI-assisted automation for analog chip design, addressing one of the most persistent bottlenecks in the semiconductor development cycle. ThirdAI Automation applies causal AI to root cause analysis inside semiconductor fabs, compressing diagnostics from days to minutes and improving yield.

India's semiconductor opportunity is no longer a future thesis.

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