

# Cryogenic Superconducting Current-Source Inverters Enabled Through $J_c(B)$ Switches

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**Abstract**—A superconducting inverter topology based on the use of  $J_c(B)$  switches has been developed and demonstrated in this work. The model was constructed using MATLAB Simulink using a mixture of traditional Simscape tools and custom electrical blocks. The inverter was used to produce a square wave output across its bridge. The results show that the unit produced during this research matches qualitatively with the constructed model. In addition, the unit was shown to be able to produce large AC waveforms across its bridge.

**Index Terms**—Superconducting Inverter,  $J_c(B)$  Switch, Cryogenic Inverter.

## I. INTRODUCTION

**I**NVERTERS are a subsection of electronic power converters that convert a direct current (DC) to an alternating current (AC) through the use of appropriately timed switches [1]. Inverters find use in a range of applications from high-voltage DC (HVDC) power transmission [2] to electronic motor speed controls [3] and are even used in solar farms [4]. There are challenges facing the future architecture of the transmission and distribution networks [5] with growing demand, requiring increased capacity on narrow rights of way [6].

Superconducting cables [7] could provide a transition to a superconducting grid [8]. Cryogenic inverters provide a solution to transition into distribution voltages [9]. The current state-of-art is cryo-cooled Gallium Nitride (GaN) semiconductor technology [10]. These devices allow fast switching speed and low on-state resistance [11] but cryogenic thermal power dissipation is still substantial due to the large band gap voltage of GaN devices [12]. An alternative cryogenic switch topology is required that delivers lower cryogenic thermal dissipation.

Superconducting dynamos and switch rectifiers have been demonstrated to operate at several thousands of amps [13–15] with extremely low voltage drop across their cryogenic switches [16]. The best performing uses a  $J_c(B)$  switch [17] which disrupts the superconducting state [18] and has extremely low voltage drop associated in the conducting state, and suitable for a superconducting inverter topology. We have modeled implementation in an inverter topology and demonstrated feasibility with implementation of an experimental superconducting inverter.

## II. BACKGROUND

The H-bridge topology [19] uses four switches in an “H” shape where the load sits across the horizontal section (bridge). In this topology, the switches can be controlled to switch a DC source to produce an alternating AC input to a transformer (and load) in its bridge.

### A. Primary Inverter Segments

The inverter has three primary components; HTS circuit, the  $J_c(B)$  switch, and transformer. 12 mm SuNAM YBCO coated conductor [20] was selected due to having a large  $J_c(B)$  dependence, whilst having a large critical current density ( $J_c$ ) under self-field [21].

$J_c(B)$  switches are used, using an applied magnetic field perpendicular to the HTS [22] that induces flux vortices in the superconductor, and lowers  $J_c$  [23]. Exceeding this  $J_c(B)$ , whilst still superconducting, exhibits resistive properties and switch action [16].

The final component is a step-up transformer, its function to take the high current in the superconductor and generate more traditional load-driving voltage levels. A superconducting primary and a copper secondary was chosen due to the lower required secondary currents and is more cost-effective.

### B. Secondary Driver Components

Control and drive of the  $J_c(B)$  switches a constant current semiconductor H-bridge driver was constructed to drive the electromagnet elements. The conventional semiconductor H-bridge allows bipolar control of current magnitude, whilst having the ability to drive at supply voltage rails for maximum inductive ramping speed.

## III. SYSTEM MODELLING

The partially superconducting transformer was modeled in Matlab Simulink [24] (see Figure 1) as a linear transformer with a zero resistance (superconducting) primary 1. The transformer parameters were collected from the as-wound 1:300 step up transformer and used in the simulations as seen in Table I. These parameters were obtained through a series of measurements. Specifically, the primary and secondary inductance's were measured with an LCR meter at  $20Hz$  while

the winding set not under inspection was left open circuit. The secondary resistance was measured via four point measurement at 77K. The magnetization resistance was determined with the primary windings open circuited by passing a low voltage 20Hz sine wave through the secondary windings and measuring the real input power, in the same test magnetization inductance was calculated from the RMS current. The formulae used to calculate magnetization resistance and inductance can be seen in equations 1 and 2 respectively.

$$R_m = \frac{V^2}{P_{core}} \quad (1)$$

$$L_m = \frac{V}{2\pi f I_m} \quad (2)$$

TABLE I  
SIMULATED TRANSFORMER PARAMETERS COLLECTED FROM A  
PRE-WOUND 1:300 TRANSFORMER

Primary Inductance, $L_1$	1.66 $\mu$ H
Magnetization Resistance, $R_m$	5 k $\Omega$
Magnetization Inductance, $L_m$	1.5 $\mu$ H
Secondary Inductance, $L_2$	192.26 mH
Secondary Resistance, $R_2$	0.43 $\Omega$

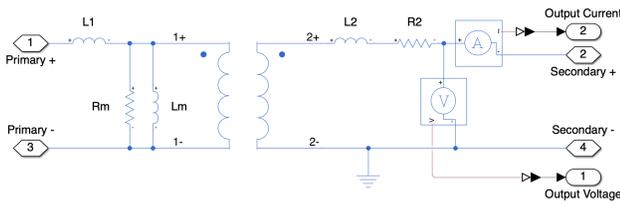


Fig. 1. Linear partially superconducting transformer modelled in MATLAB Simulink.

The  $J_c(B)$  switches were simulated as resistive elements with transport current, switch length, temperature, and applied external magnetic field as input parameters. Data for the field dependent critical current ( $J_c(B)$ ) was interpolated from SuNAM SAN04200 2G HTS data set [21]. The Simscape model for the superconducting  $J_c(B)$  inverter makes use of four  $J_c(B)$  switches with a load transformer and resistive load across its bridge section (Figure 2).

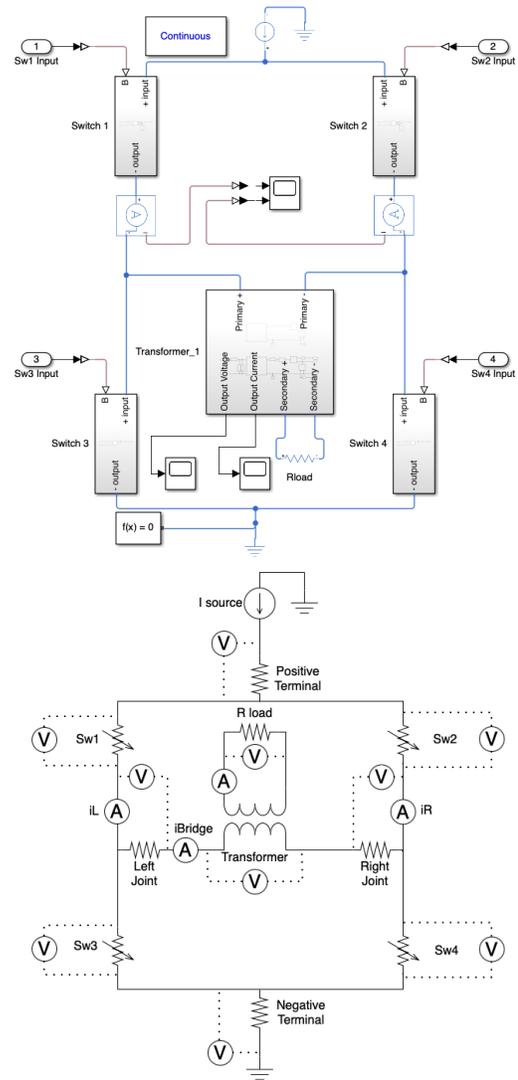


Fig. 2. (Top) Superconducting  $J_c(B)$  H-bridge inverter modelled in MATLAB Simulink. (Bottom) H-bridge circuit schematic including all resistive joints in the experimental circuit and the voltage and current sensing locations denoted "V" and "I" respectively.

Figure 3 shows the frequency response of the transformer primary current of the model inverter using a 0.5  $\Omega$  load resistor, 1.2 T applied switch field and a constant DC input of 300 A. These model input values were derived from measurements of a transformer and switch system built. The model assumed a square wave switch input with frequency equal to the desired output fundamental frequency. The transformer primary current, or bridge current waveform, indicates the peak to peak current deliverable by the superconducting inverter. It can be seen that the primary side current reduces with increasing frequency, due to the frequency response of the switch circuit when the switch resistance is frequency independent.

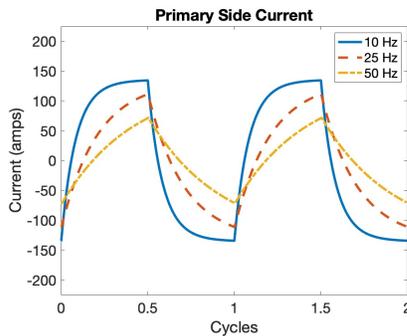


Fig. 3. Modelled transformer primary current waveform over frequencies, 10 Hz, 25 Hz, and 50 Hz with a 0.5  $\Omega$  load connected to the secondary.

Comparison of the primary current of the inverter transformer with resistive load was also investigated between 1 and 100  $\Omega$  and shown in Figure 4. Some frequency response sensitivity is also seen at higher impedance, though less pronounced due to the reduction in source impedance through the transformer [25]. This is a result of the changing time constant of the  $LR$  circuit.

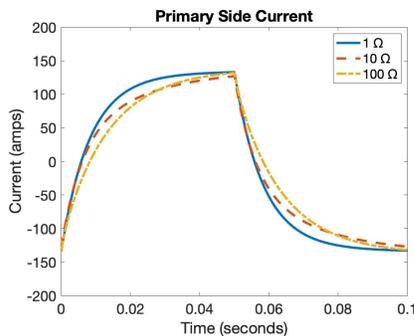


Fig. 4. Modelled 10 Hz transformer primary current waveform with a 1  $\Omega$ , 10  $\Omega$ , and 100  $\Omega$  resistive load on the secondary side.

#### IV. EXPERIMENTAL $J_c(B)$ SUPERCONDUCTING INVERTER

The body of the superconducting inverter was assembled primarily with 3D printed PLA conduit system components that provides a LEGO™ like mechanical structure for superconducting tapes, allowing for ease of development and iteration. These conduit pieces mount on a grid patterned board similar to an optical table.

A GFRP (G-10) breadboard was chosen for its low thermal coefficient of expansion as well as its low thermal conductivity. Although primarily constructed from PLA, several sections were constructed from metals; copper and aluminium for the inverter DC bus terminals and hall effect sensor mounts respectively. The terminal pieces were machined from copper to allow adequate electrical connectivity between the DC input leads and the superconducting tape.

The superconducting circuit uses 12 mm SuNAM YBCO coated conductor [20] was selected due to having a large  $J_c(B)$  dependence, whilst having a large critical current ( $J_c$ ) under self-field [21]. The switching core segments along with the transformer utilised C-shaped laminated silicon steel cores

to reduce losses [26]. These high saturation cores allowed a 1.2 T field to be applied to the superconducting tape. The switch windings were wound on PLA bobbins with 125 turns per switch. The switch windings are the copper windings wound around the electromagnet core used in providing the magnetic field to the superconducting tape. The C-shaped cores featured a 0.5 mm gap for the superconducting tape to pass through. This arrangement delivered the required 1.2 T field within a 10 A drive current in the switch windings.

Bifilar switch tape elements were used in order to maintain the self field  $I_c$  of the tape [17]. While in a unifilar configuration the self field  $I_c$  of a superconducting tape is degraded due to the magnetic field in the core gap lowering the  $I_c$  of the superconducting tape and reducing the  $J_c(B)$  switch performance in its ‘closed’ state [27].

A 1:300 step up transformer, consisting of a SuNAM SAN04200 primary and 0.44 mm<sup>2</sup> copper secondary was fabricated.

Cryogenic voltage measurements were made with twisted pair voltage taps in order to reduce electromagnetic interference on the differential measurements. Current measurements were made with an open loop hall effect sensor as this offers a non-invasive current measurement. We created our own open loop hall current sensors similar to that reported by James Rice in his PhD thesis [27].

RT voltage and current measurements were recorded on the differential inputs of the NI-9205 module which was used to collect all voltage and current measurements in the system. The NI-9205 was used for its multitude of differential inputs, individual programmable gains, and its micro-volt resolution [28]. Figure 5 shows the CAD design and realized Inverter.

Low temperature, Indium based, solder joints were used in order to produce low resistance joints without exceeding 200 °C to avoid  $J_c$  reduction of the REBCO tape [29]. Clamping modules incorporating a heater cartridge to heat two pre-tinned sections of REBCO tape and clamped together with a G-clamp. Once solder was seen to flow the clamp was then tightened and allowed to cool to ensure low resistance joints.

Four point measurement of resistance using an Agilent 34420A Nano-Volt Meter ensured an accurate measurement of the joint resistance. these values are shown in Table II.

TABLE II  
MEASURED INVERTER JOINT RESISTANCES

Positive Terminal	1.388 $\mu\Omega$
Negative Terminal	0.697 $\mu\Omega$
Left Bridge Joint	0.715 $\mu\Omega$
Right Bridge Joint	0.638 $\mu\Omega$

All experimental procedures were performed submerged in liquid nitrogen and a constant temperature of 77 K was assumed across the system sections set in the cryogenic environment. A constant current of 300 A was supplied at the DC bus terminals and the  $J_c(B)$  switch cores were brought to their knee point (1.2 T field) when in their open state.

Figure 6 shows a block diagram of the experimental setup.

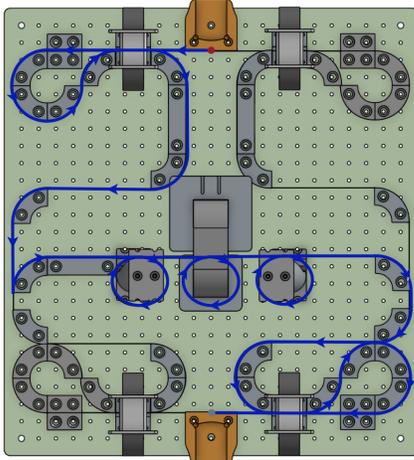
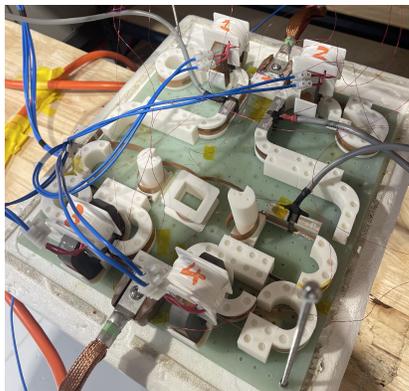
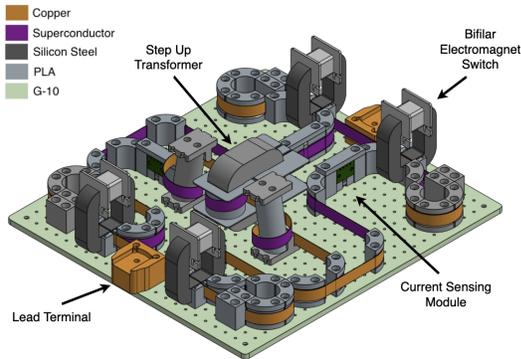


Fig. 5. CAD model for the superconducting inverter (top figure), assembled superconducting inverter prototype (middle figure), and a CAD model birds eye view showing the current path during the positive half cycle of the AC waveform (bottom figure). Noting that the purple superconducting face depicted in the CAD model is the superconducting side of the tape and not exposed superconducting material. The orange side of the tape is the substrate side and depicts the copper stabiliser which surrounds the tape and not an additional copper tape along side the superconductor.

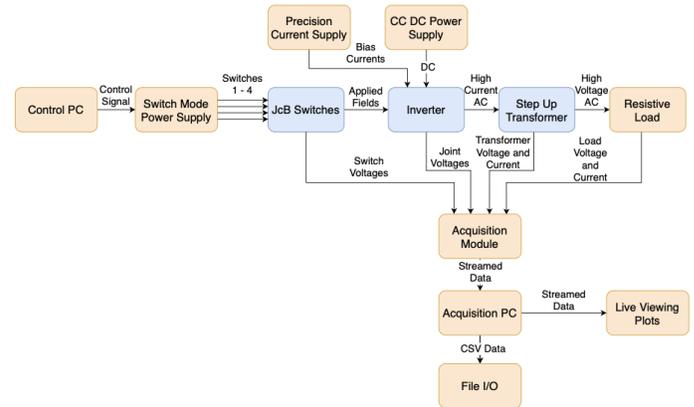


Fig. 6. System block diagram of the experimental setup. Orange represents the room temperature components and blue represents the cryogenic components.

### V. COMPARISON OF RESULTS AND MODEL

The model system had a switch resistance of  $13.24 \mu\Omega$ , switch resistance based on the nominal cross sectional area of the superconducting tapes conductive layers i.e., copper and silver, the temperature of the switches, and the switch length. The experimental derived values in Table III show good agreement with calculated.

TABLE III  
EXPERIMENTAL SWITCH RESISTANCES

Switch One	$13.76 \mu\Omega$
Switch Two	$14.78 \mu\Omega$
Switch Three	$13.56 \mu\Omega$
Switch Four	$13.29 \mu\Omega$

A base line demonstration experiment was carried out as can be seen in figure 7. Figure 7 shows the flow of current in the circuit and the impact of the switches on the current in each branch of the circuit.

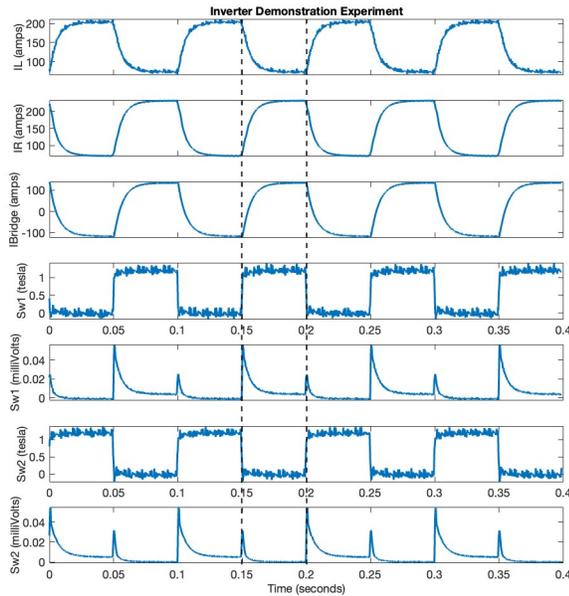


Fig. 7. Experimental results from the inverter demonstration experiment. From top to bottom is the left branch current, IL, right branch current, IR, bridge current, IBridge, switch one applied field, switch one voltage, switch two applied field, and switch two voltage. The dashed vertical lines indicate half-cycle transitions caused by the alternation of the switch pairs.

Side-by-side comparison of the inverter primary drive waveforms show qualitative agreement with the simulated results as shown in figure 8. This qualitative agreement shows a similar frequency response behaviour, and validates the model as a qualitative assessment tool.

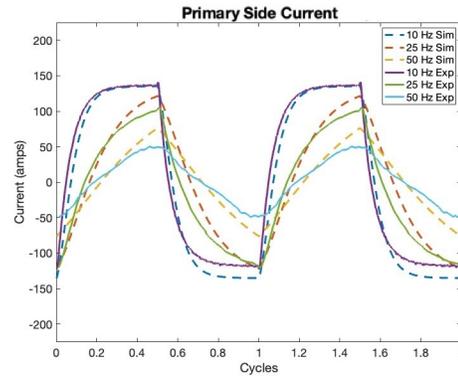


Fig. 8. Comparison of predicted (simulation) and measured transformer primary current wave from at 10, 25, and 50 Hz with a  $0.5 \Omega$  load.

Close inspection of the 10 Hz primary current waveform shows instantaneous spikes upon transitioning from the positive half cycle to the negative half cycle and vice-versa as shown in Figure 9. These spikes are not captured within the Simulink system model, and are an induction effect that was confirmed through a single half cycle operation. Figure 10 shows the measured transformer primary current and the field applied to the tape section when switching with no applied DC current confirming the induction from switch electromagnets.

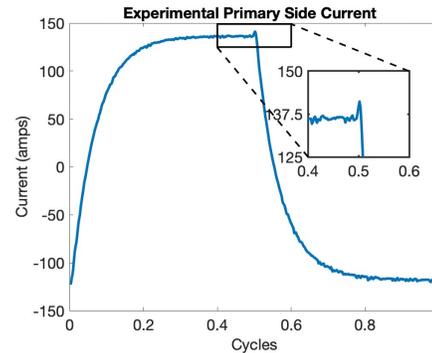


Fig. 9. Measured transformer primary current at 10 Hz with a  $0.5 \Omega$  secondary load. Zoomed in figure highlights inductive spike when transitioning half cycles.

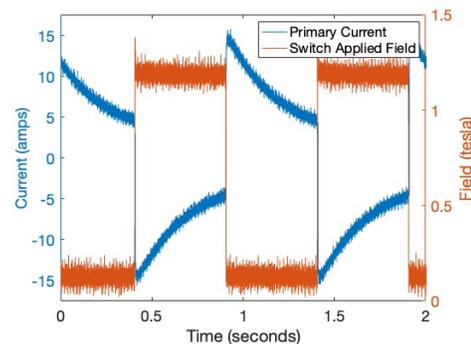


Fig. 10. Measured bridge current in the absence of a DC bus supply and transformer load showing the generation of an induction current when switches one and four are driven with a 1.2 T 1 Hz square input waveform.

Additionally, in figure 7 a secondary smaller voltage peak is seen across the switch that is closing. This is a result of dynamic resistance being generated in the switch due to a change in magnetic field within that region [30].

An important aspect of validating the inverter model is the power delivery performance. Although the experimental system was relatively low output power, it was still possible to complete this comparison. With a 300 A DC input and 0.5 Ω load the inverter's RMS power was measured over several operating frequencies and compared with the model in Figure 11. Both experimental and simulation show the same negative correlation with operating frequency. Noting that the power dissipation of the electromagnets has been ignored in the system efficiency as they overwhelm the power dissipation in the remainder of this specific circuit (~ 19.5W per switch). Additionally, the dissipation of the switch technology is unlikely to scale with the power output of the inverter due to the nature of the switching method.

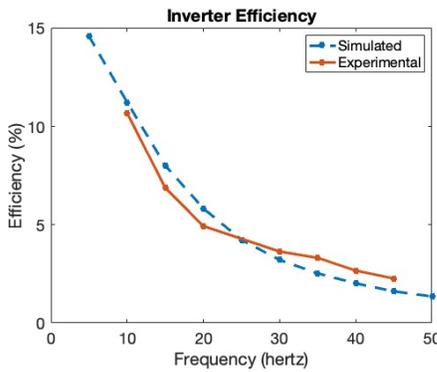


Fig. 11. Efficiency comparison between modelled and experimental results with a 0.5 Ω and increasing operational frequency.

Increasing the open state resistance of the switches would help the system overcome this frequency response limitation and improve deliverable power at higher frequencies. Furthermore, due to the low  $J_c(B)$  switch resistance relative to the load impedance a large proportion of the DC source is shorted through the “open”  $J_c(B)$  switches. This limits current transferred to the load and induces additional loss in the switch sections. This unintentional current flow through the switches can be seen in figure 7. Figure 12 shows the results of a model sweep over the switch resistance and confirms this assumption. Higher switch resistance improves performance at all frequencies.

Even with large switch resistances the peak efficiency of the inverter remains low. This is a result of the current lost due to the relatively high critical current during the open state of the switch along with the low magnetization inductance of the transformer which requires large magnetization currents to operate therefore driving up transformer losses and reducing system efficiency.

A decrease in output power with frequency is seen at the very low frequency range. This decrease is seen in both the scaled  $J_c(B)$  switch and the ideal case. This decrease is a direct impact of the transformers magnetization inductance. As is seen in the previous sections, the transformer is modeled

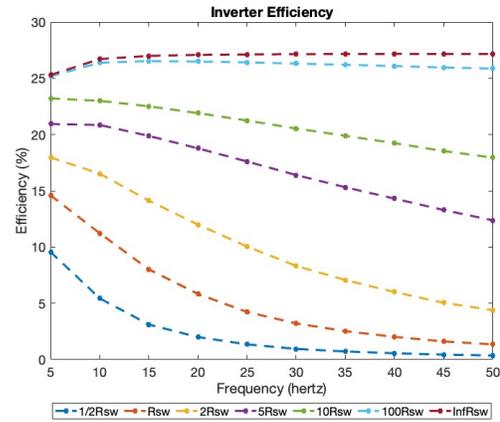


Fig. 12. Simulated efficiency with a 0.5 Ω load with increasing operational frequency and increasing switch resistance.

with a inductance in parallel with the ideal transformer windings. This parallel inductance shows decreasing reactance with decreasing frequency, therefore at extremely low frequencies this inductor behaves more and more like a short. This lowered reactance effectively allows more current to bypass the primary windings and therefore lower deliverable power to the load. An analytical expression of this behaviour can be seen in equation 3 which describes the peak power transfer of a transformer as a function of frequency.

$$P_{max}(f) = \sqrt{S_{max}^2 - \left(\frac{V_p^2}{2\pi f L_m}\right)^2} \quad (3)$$

Finally, with the main benefit of an H-bridge inverter over a two-level inverter being its ability to produce three distinct levels as opposed to two, the inverter was run to obtain a 1 Hz modified sine wave output as seen in Figure 13. A modified sine wave is a low effort approximation of a sine wave and the first step towards reduction in total harmonic distortion (THD) of the output waveform.

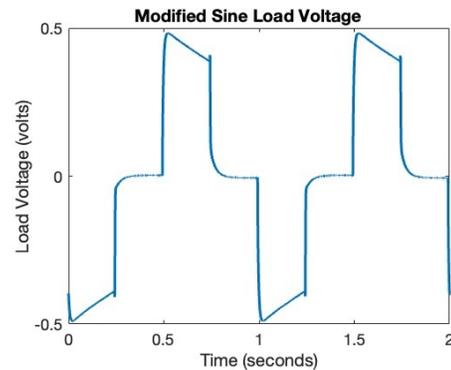


Fig. 13. Measured resistive load voltage for a 1 Hz modified sine wave output with a 0.5 Ω load.

The waveform in figure 13 was produced by applying a modified sine magnetic waveform to the switches. This in turn produced a modified sine wave across the inverter's bridge

section. Therefore, showing the viability of a fully functioning superconducting  $J_c(B)$  modified sine wave/H-bridge inverter. The ability to produce a modified sine wave is an important step towards sine wave inverters as it enables the ability to employ PWM control which in turn reduces THD of the output signal. Adequate reduction of THD ( $< 4\%$  THD) is necessary for grid integration of inverters.

## VI. DISCUSSION

The results show a  $J_c(B)$  superconducting inverter operating at grid frequencies is possible and that a Matlab Simulink model closely agrees with experimental results. Constant resistance in the  $J_c(B)$  switches limit the rise time of the transformer primary current, limits the frequency response and hence "square" AC waveform shape. It was seen that increasing resistive load on the secondary side also limits the frequency response due to the  $LR$  charging behaviour of the load. Both of these trends are a result of the impedance seen across the bridge relative to the impedance produced by the switching segments. Increasing switch resistance would reduce this time constant and produce higher frequency response in the current waveforms.

The superconducting  $J_c(B)$  switch topology allow a new design concept for cryogenic inverters with lower switch dissipation than current state-of-art technologies [10, 31]. It may be possible to interface superconducting DC transmission line and the room temperature AC networks.

The current performance limitation is due to switch "off" resistance and the output THD. Increasing switch resistance may be achieved through chemical etching, or ablation, removing both the copper and silver layer from the superconducting tape to increase the open state resistance. To reduce THD, a filtering segment could be used to remove the bulk of unwanted harmonics within the signal. Additionally, a multi-level implementation of the H-bridge topology, commonly referred to as a cascaded H-bridge, could be implemented as this would inherently lower the THD of the output waveform prior to filtering.

## VII. CONCLUSION

To conclude, in this research a superconducting  $J_c(B)$  current-source inverter was produced and was shown to produce results that agreed qualitatively with the constructed model. The superconducting inverter was able to produce an alternating waveform across its bridge at 50 Hz under a load of  $0.5 \Omega$ . Current peaks upon transitioning half cycles of the bridge waveform were seen and appropriately explained to be electromagnetic induction caused by the electromagnetic switch elements. The peak bridge current showed a negative correlation with bridge operating frequency likely caused by the increasing impedance of the bridge with frequency. Additionally, deliverable power to the load showed a negative correlation with bridge operating frequency again caused by the increasing bridge impedance with frequency. Finally, a modified sine wave output was produced across the bridge to validate the three voltage level operation of the inverter.

Currently the superconducting  $J_c(B)$  current-source inverter is limited primarily by switch resistance and output THD when targeting grid applications.

Due to the inherently low resistance of the  $J_c(B)$  switches in their open position the inverter is currently unable to overcome the impedance of the bridge when operating at grid frequencies. The output waveform harmonics are a limitation due to a grid requirement that AC waveforms distributed across the network must remain under  $4\%$  THD. Adding a filtering step to the inverter would reduce waveform harmonics and remove this limitation.

Further research in this area would see the improvement of switch resistances and the development of a post processing filtering stage to reduce waveform harmonics.

## ACKNOWLEDGEMENTS

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