## FEATURES

- 0.8 V – 1.6 V input voltage range
- 1.4 V – 1.8 V output voltage range
- 100 mA continuous load operation
- Integrated inductor
- 5 MHz switching frequency
- Soft-Start, OTP, SCP, cycle by cycle current limit
- Test points and sockets for VIN, VOUT and GND
- 7.9mm coin cell battery holder

## APPLICATIONS

- Hearing aids and wearables
- IoT sensors
- Single- and double-cell PV applications

## DESCRIPTION

The LMU20P1-EVB is a fully assembled and tested printed circuit board that demonstrates the LMU20P1 miniaturized step-up Power Supply in Package (PSiP). The LMU20P1 itself, offers small size, high efficiency and includes an integrated circuit and an inductor in a compact 2 mm x 2 mm x 0.75 mm package.

The LMU20P1 has a light-load efficiency enhancement function to achieve high efficiency across a wide load range and features a range of protection circuits that include soft start, over-temperature protection, short-circuit protection, and cycle-by-cycle current limit.

The evaluation board is equipped with test points and jumpers for testing most of the functionality of the device. There are also probing holes on critical nodes for precise measurements.

## TYPICAL APPLICATION

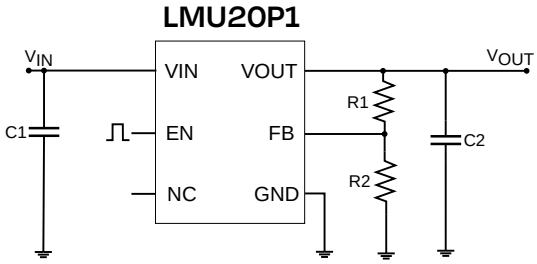


Figure 1: LMU20P1 application schematic

- C1 is the input capacitor
- C2 is the output capacitor
- R1 and R2 are the feedback resistors

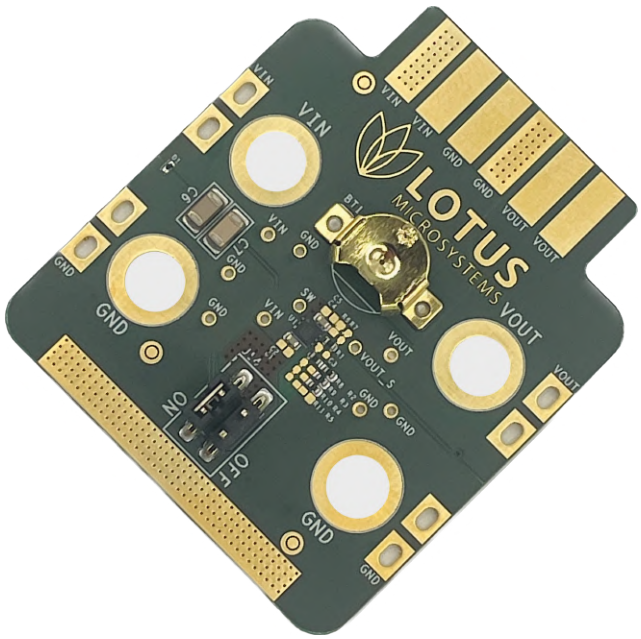

Figure 2: LMU20P1-EVB evaluation board

# EVALUATION BOARD SPECIFICATIONS

All values are measured or simulated at $T_A$ = +25 °C, $C_{IN}$ = $C_{IN}$ = 10 uF, $V_{IN}$ = $V_{EN}$ = 1.5 V, $V_{OUT}$ = 1.6 V, unless otherwise noted.

Table 1: LMU20P1-EVB specifications

| Specification | Symbol | Conditions & Notes | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input Quiescent Current | $I_{Q\_IN\_SD}$ | EN=LOW | | 0.18 | | µA |
| | $I_{Q\_IN\_NSW}$ | EN=HIGH, non-switching | | 0.7 | | µA |
| Input Voltage Range | $V_{IN}$ | | 0.8 | | 1.6 | V |
| Input Start-up Voltage | $V_{IN\_STRT}$ | | | 0.8 | | V |
| Output Voltage Accuracy | | PWM | | | ± 2 | % |
| | | PFM (Does not include feedback resistors tolerance) | | | ± 3 | % |
| Switching Frequency | $f_{SW}$ | | | 5.0 | | MHz |
| Output Voltage Range | $V_{OUT}$ | | 1.4 | | 1.8 | V |

# BOARD DESCRIPTION

Figures 3 and 4, below, show the top view and the top layer assembly of the LMU20P1-EVB. The left side of the board contains the input and ground connectors, while the right side of the board contains the output connectors. The lower side contains the jumpers that enables the LMU20P1. The upper side socket connector is used for internal purposes only.

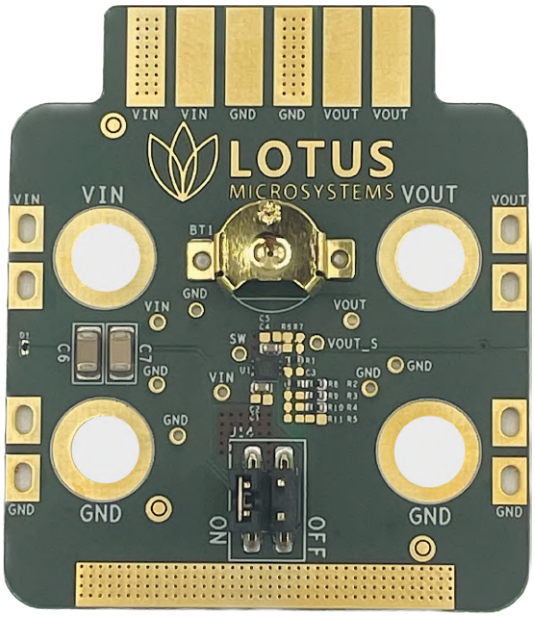


Figure 3: LMU20P1-EVB top layer assembly

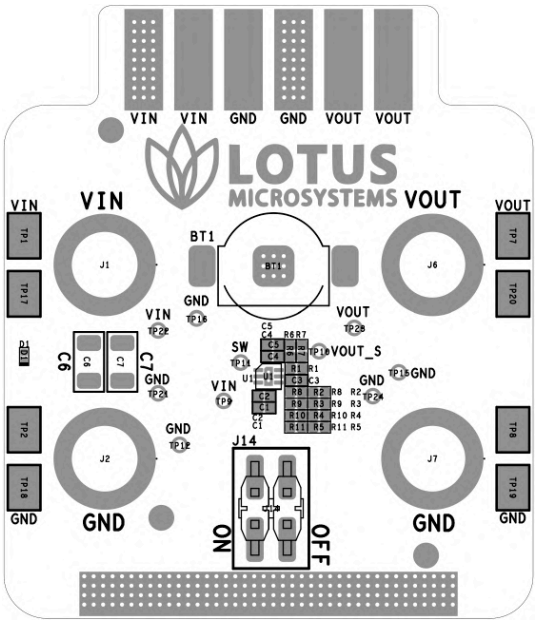


Figure 4: LMU20P1-EVB top layer layout

## DETAILED HARDWARE DESCRIPTION

### INPUT AND OUTPUT TERMINALS

The input voltage source of the LMU20P1-EVB can be connected to TP17 and TP1 or to J1 (not mounted), which enables installation of an optional banana jack terminal. In the same way, TP20, TP7 and J6 (not mounted) provide for a terminal to the output voltage. LMU20P1-EVB also provides for an optional coin cell battery holder (BT1) for portable application testing. BT1 must not be connected at the same time as the other input terminals to different voltage sources.

### DEVICE ENABLING AND DISABLING

The LMU20P1 is enabled or disabled by J14, connected to the EN pin of the device. Only one of the sides of J14 should be connected. See table 2 for more information.

### SETTING THE OUTPUT VOLTAGE

The evaluation board output voltage is set to 1.8 V by default. Use resistors R2 to R5 and R8 to R11 in order to set the desired voltage. Useful resistor footprints are set to mount the desired values. The tolerance of the feedback resistors is 1%.

### SW PIN SWITCHING NODE

The LMU20P1 includes an SW pin which can be utilized for debugging and monitoring purposes through TP11. Under normal operation it should be left floating.

### INPUT CAPACITORS AND PROTECTION

The LMU20P1-EVB includes C2 and C10 (not mounted) for the required input capacitance for the LMU20P1. They are located as close as possible to the device. C6 and C7 provide extra decoupling and filtering for cases where long wires or other noise or instability sources can affect the input voltage. The size of C6 and C7 depend on the application. The board also includes an ESD diode, D1, to provide protection at the board level.

### OUTPUT CAPACITORS

The LMU20P1-EVB includes C4 and C5(not mounted) as the required output capacitance for the LMU20P1. They are located as close as possible to the device. Increasing the capacitance reduces the output voltage ripple and improves the transient response.

## CONNECTORS AND JUMPERS

Table 2: LMU20P1-EVB connectors and jumpers

| Pin | Name | Description |
|---|---|---|
| J1, TP1, TP17 | VIN | Terminal. Connect input voltage source here |
| J6, TP7. TP20 | VOUT | Terminal. Connect output load here |
| J2, J7, TP2, TP8, TP19 | GND | Terminal. Connect ground here |
| J14 | ON/OFF | Short pins 1 and 2 (ON) / Short pins 3 and 4 (OFF) |
| BT1 | BT1 | Optional coin cell battery connector for the input source |

## QUICK START PROCEDURE

- Before connecting any equipment to the board set J14 to the OFF position.
- Set the feedback resistors according to the schematic of figure 5 to set the desired output voltage.
- Connect any testing equipment and load.
- Set J14 to the ON position.
- Turn on the equipment, such as input source, current meters and load.

## SCHEMATIC

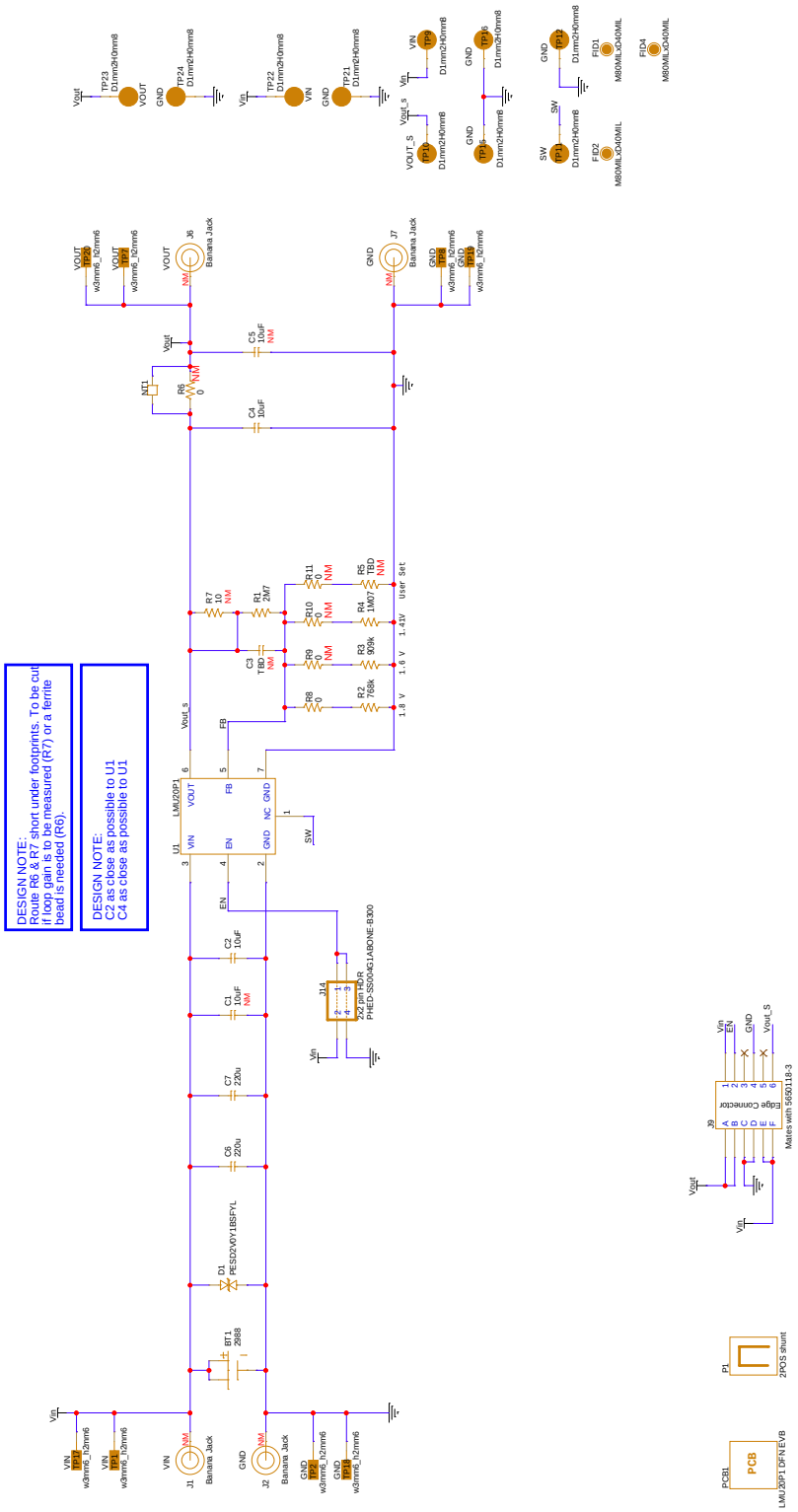


Figure 5: LMU20P1-EVB schematic

# BILL OF MATERIALS

Table 3: LMU20P1-EVB bill of materials

| Designator | Placing | Quantity | Description | Manufacturer | Part number |
|---|---|---|---|---|---|
| BT1 | Mounted | 1 | BAT_2988TR | Keystone Electronics | 2988TR |
| C1,C5 | Not Mounted | 2 | CAP CER 10UF 6V3 X5R 0402 | Murata | GRM155R60J106ME05J |
| C2,C4 | Mounted | 2 | CAP CER 10UF 6V3 X5R 0402 | Murata | GRM155R60J106ME05J |
| C3 | Mounted | 1 | TBD | | |
| C6,C7 | Mounted | 2 | CAP CER 220UF 2.5V X6S 1206 | Murata | GRM31CC80E227ME11 |
| D1 | Mounted | 1 | TVS DIODE 2VWM 3VC DSN0603-2 | Nexperia | PESD2V0Y1BSFYL |
| J1,J2,J6,J7 | Not Mounted | 4 | BANANA VERTICAL CONNECTOR | Keystone Electronics | 575-8 |
| J14 | Mounted | 1 | CONN HEADER SMD 4POS 2.54MM | Superior Tech | PHED-SS004G1ABONE-B300 |
| P1 | Mounted | 1 | JUMPER W/TEST PNT 1X2PINS 2.54MM | Sullins Connector Solutions | QPC02SXGN-RC |
| R1 | Mounted | 1 | RES 2.7M OHM 1% 1/16W 0402 | Yageo | RC0402FR-072M7L |
| R2 | Mounted | 1 | RES 768k OHM 1% 1/16W 0402 | Yageo | RC0402FR-07768KL |
| R3 | Mounted | 1 | RES 909k OHM 1% 1/16W 0402 | Yageo | RC0402FR-07909KL |
| R4 | Mounted | 1 | RES 1M07 OHM 1% 1/16W 0402 | Yageo | RC0402FR-071M07L |
| R5 | Not Mounted | 1 | RES TBD 0402 | | |
| R6,R9,R10,R11 | Not Mounted | 4 | RES 0 OHM JUMPER 1/16W 1A 0402 | Yageo | RC0402FR-070RL |
| R7 | Not Mounted | 1 | RES 10 OHM 1% 1/16W 0402 | Yageo | RC0402FR-0710RL |
| R8 | Mounted | 1 | RES 0 OHM JUMPER 1/16W 1A 0402 | Yageo | RC0402FR-070RL |
| U1 | Mounted | 1 | 100mA Synchronous Boost Converter | Lotus Microsystems | LMU20P1 |

## PCB LAYOUT

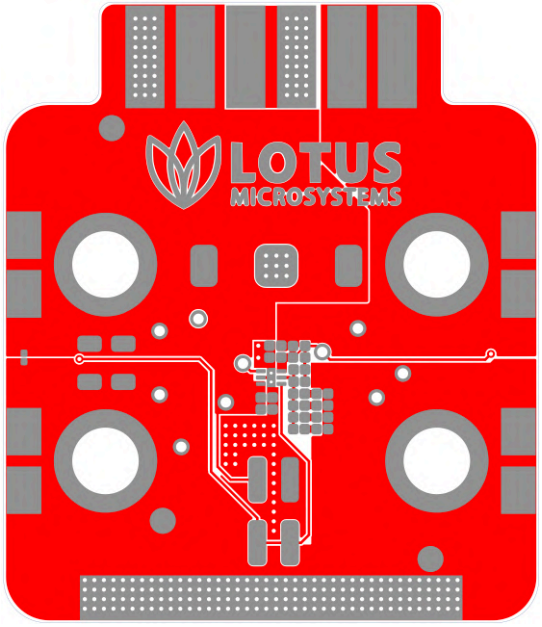


Figure 6: LMU20P1-EVB top layer layout

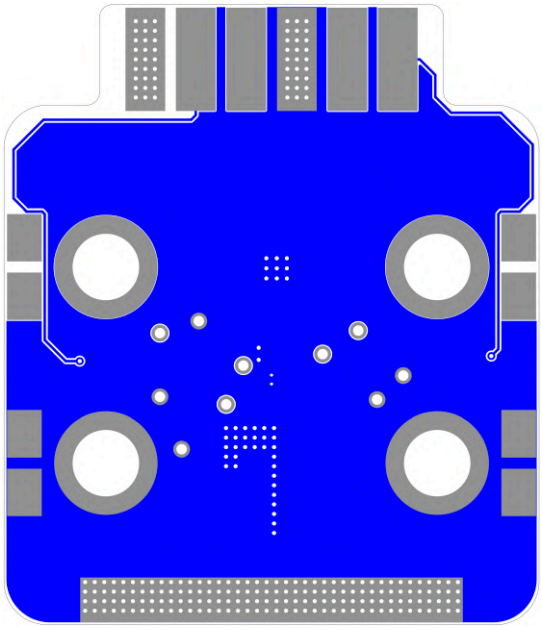

Figure 7: LMU20P1-EVB bottom layer layout (not mirrored)

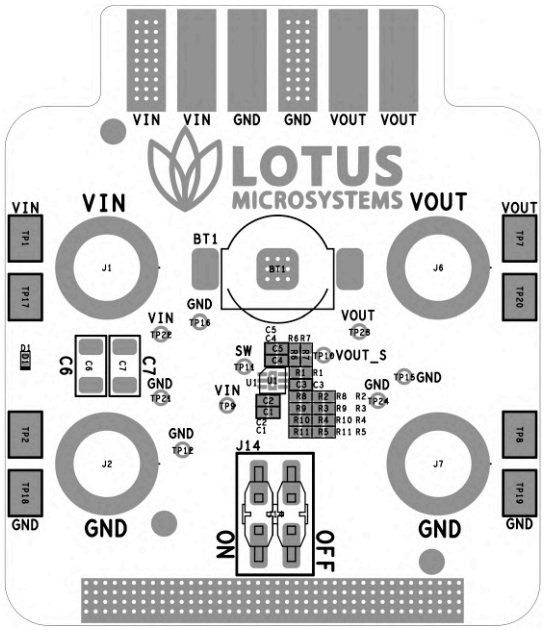


Figure 8: LMU20P1-EVB top layer assembly

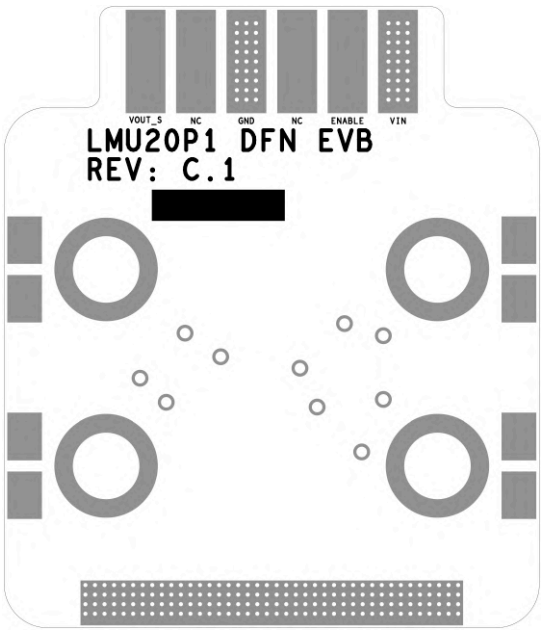


Figure 9: LMU20P1-EVB bottom layer assembly (mirrored)

# REVISION HISTORY

| Revision Number | Revision Date | Description | Pages Changed |
|---|---|---|---|
| 0.9 | 28/02/2024 | Preliminary release | - |
| 0.91 | 07/03/2024 | Update EVB picture | 1,2 |
| 1.0 | 09/04/2025 | Clean up for public release | - |

# IMPORTANT INFORMATION AND DISCLAIMER

1. The product, product specifications and any other information contained herein are subject to change without notice. Consult us, or our representatives, before use, to confirm that the information in this datasheet is up to date.
2. Please use the products listed in this datasheet only within the specified ranges.
3. We assume no responsibility for damage or loss due to abnormal use
4. Please ensure suitable shipping controls (including fail-safe designs and aging protection) are in force for equipment employing products listed in this datasheet.
5. We make no representation that the interconnection of our circuits or use of the information herein will not infringe any patents, patent rights, or other rights.
6. The products in this datasheet are not developed, designed, or approved for use with equipment whose failure or malfunction can be reasonably expected to directly endanger the life of, or cause significant injury to, the user (such as high-power or nuclear energy, aerospace, transport, combustion, and safety equipment associated therewith).
7. The information provided in this document represents our knowledge and belief as of the date it was provided. We base our knowledge and belief on information provided by third parties, and make no representation or warranty as to the accuracy of such information.
8. We continue to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
9. We and our suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.
10. In no event shall our liability arising out of the use of the information in this paper exceed the total purchase price of the Lotus part(s) at issue in this document sold to you on an annual basis.



LOTUS MICROSYSTEMS