LOTUS MICROSYSTEMS

DESCRIPTION

LTG devices from Lotus Microsystems are thermally conductive yet electrically isolated, silicon-based thermal jumpers.

These devices are designed to guide heat away from hot electronic components, toward heat sinks or cooler areas (such as ground planes), without establishing an electrical connection.

LTG devices significantly enhance thermal conductivity, particularly in scenarios with limited or no direct access to a ground plane or heat sink, such as high-side switches in a half-bridge configuration.

Silicon, as an alternative to traditional ceramic materials, offers a cost-effective substrate with high thermal conductivity and excellent thermo-mechanical properties and reliable processing. By improving thermal management, LTG devices help reduce component temperatures, supporting higher circuit reliability and longer service life.

FEATURES

- High thermal conductivity, up to 140 W/(m K)
- High electrical isolation resistance
- Low parasitics
- High precision standard package dimensions
- Low coefficient of thermal expansion (CTE)
- RoHS compliant

APPLICATIONS

- High-power LEDs
- Pin and laser diodes
- Power converters and amplifiers
- xPU and FPGA boards
- Semiconductor packages
- Optical Transceivers

Abstract

This application note evaluates the use of Lotus Microsystems Thermal Guide (LTG) devices to improve the thermal management of a common-drain dual MOSFET configuration. LTGs provide an electrically isolated thermal path between the active drain region and a larger grounded copper area, enabling heat to be dissipated without increasing the size of the electrically active node. Evaluation boards using LTG0402, LTG0603, and LTG0805 devices are developed. The LTG0402 and LTG0603 implementations are experimentally characterized using electrical measurements and infrared thermal imaging, while the LTG0805 implementation remains under development. The LTG0402 implementation achieves an average device surface-temperature reduction of 42.9 °C, a mean power-loss reduction of 7.04 %, and an efficiency improvement of 0.44 p.p. The LTG0603 implementation achieves an average temperature reduction of 28.2 °C, a mean loss reduction of 3.01 %, and an efficiency improvement of 0.13 percentage points. The results demonstrate that LTGs can significantly reduce device temperature and conduction losses, particularly in compact PCB layouts where the available drain-connected copper area is limited.

Figure 1: LTG 3D package representation.

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1 Application Description

Multiple compact electronic systems rely on dual MOSFET devices to implement functionalities such as bidirectional switching, reverse-current blocking or battery protection. These devices can use either common-drain or common-source configurations. The dual MOSFET device evaluated in this application uses the common-drain configuration shown in Figure 2.

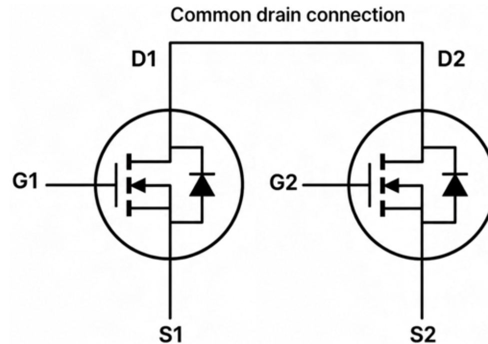


Figure 2: Common-drain configuration.

The increasing power density and reduced package dimensions of modern MOSFETs lead to highly concentrated heat generation. Thermal management becomes particularly challenging when the electrically active drain node cannot be directly connected to a grounded heatsink or to a large cooling plane. Under these conditions, the available copper may be insufficient to spread the generated heat effectively, leading to higher MOSFET temperatures, increased conduction losses, reduced overall system efficiency, and accelerated component ageing that may shorten the device lifetime.

Lotus Microsystems Thermal Guides (LTG) can provide an electrically isolated thermal path between the MOSFET and a lower-temperature, larger copper area. This allows heat to be transferred away from the electrically active nodes without creating a conductive connection between the two regions.

This application note evaluates the performance of LTGs when integrated with a common-drain dual MOSFET. Three evaluation boards (EVBs) are developed using LTG0402, LTG0603, and LTG0805 devices, respectively. Each board uses the same MOSFET and the same number of LTGs, enabling to experimentally assess the thermal performance of the three different implementations.

2 Operating Principle

As presented in Figure 2, two N-channel MOSFETs can be connected in a common-drain configuration. When both devices are turned on, current flows through the two MOSFETs connected in series. The resulting conduction losses can be approximated as:

$$P_{\text{loss,cond}} \approx I^2 \left(R_{\text{DS(on)},1} + R_{\text{DS(on)},2}\right), \tag{1}$$

When the MOSFETs are turned off, their opposing body diodes prevent continuous current flow in either direction. Since $R_{DS(on)}$ typically increases with junction temperature, insufficient heat extraction can increase both the device temperature and its conduction losses.

A larger common-drain copper area would improve heat spreading, but it would also increase the size of the electrically active drain node. The proposed approach keeps this drain node compact while transferring its heat to a larger grounded copper plane through electrically isolated LTG devices. Consequently, the ground plane can be used as an extended heat-spreading area without increasing the physical size of the drain node.

3 Evaluation Method

3.1 Experimental Test Setup

The experimental setup consists of a power supply connected to the board input, two supplies used to turn on the MOSFETs, and an electronic load connected at the output controlling the load current. Electrical quantities are recorded during the tests, while the device temperature is monitored using a thermal camera. Figure 3 shows the circuit diagram of the presented test setup.

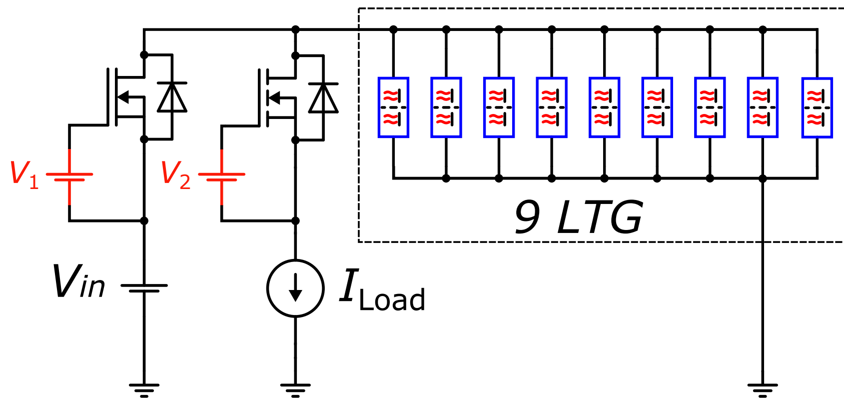
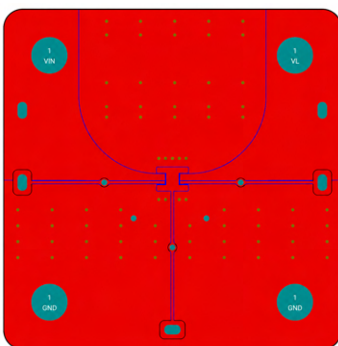


Figure 3: Schematic diagram of the experimental test setup.

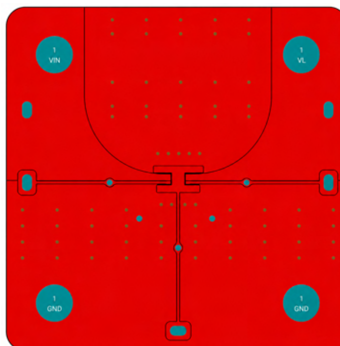
3.2 Evaluation Board

Three EVBs are developed to assess the performance of the dual MOSFET using different LTG package sizes: LTG0402, LTG0603, and LTG0805. For each package size, the performance of the EVB incorporating LTGs is compared with that of the same EVB without LTGs. The LTG0402 and LTG0603 implementations are fabricated and experimentally evaluated, whereas the LTG0805 implementation is currently under development.

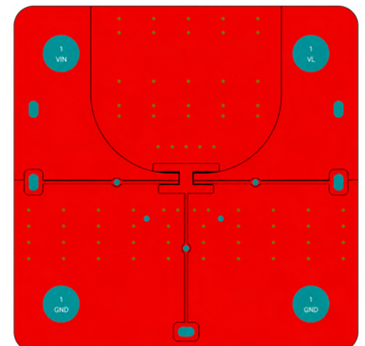
In all implementations, the same circuit topology and the same number of LTGs are used. However, the larger footprints of the LTG0603 and LTG0805 devices require a correspondingly larger copper area connected to the common-drain node. This effect is illustrated in Figure 4. Since the additional drain-connected copper also contributes to heat spreading, a direct comparison between LTG package sizes is not fully independent of the PCB layout. Therefore, each implementation is primarily evaluated against its corresponding reference EVB without LTGs.



(a) LTG0402 EVB layout.



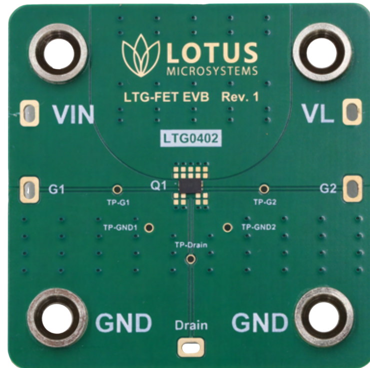
(b) LTG0603 EVB layout.



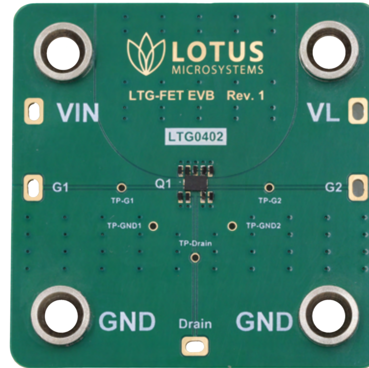
(c) LTG0805 EVB layout.

Figure 4: Top-layer PCB layouts for the three LTG package sizes.

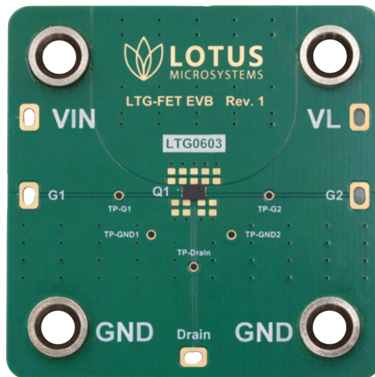
The selection of a particular LTG package ultimately depends on the thermal, electrical, and layout constraints of the target application. Figure 5 presents the LTG0402 and LTG0603 EVBs used in the experimental evaluation.



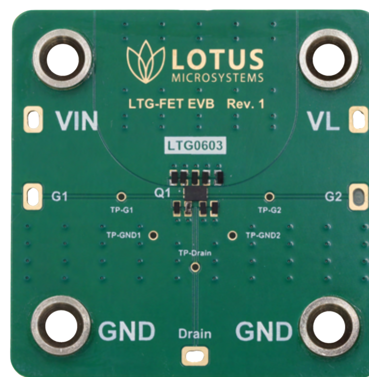
(a) LTG0402 EVB without LTGs.



(b) LTG0402 EVB with LTGs.



(c) LTG0603 EVB without LTGs.



(d) LTG0603 EVB with LTGs.

Figure 5: LTG0402 and LTG0603 EVBs used in the experimental evaluation.

3.3 Measurement Procedure

The operating conditions applied to all EVBs are summarized in Table 1.

Table 1: Experimental operating conditions.

Parameter	Symbol / Mode	Value
Input power supply voltage	V_{in}	5 V
MOSFET 1 gate-to-source voltage	V_{GS1}	4.5 V
MOSFET 2 gate-to-source voltage	V_{GS2}	4.5 V
Load current	I_{load}	9 A

Once the operating point is established, the input (V_{in}) and output (V_{out}) voltages are measured at the board terminals to calculate the conduction losses and the thermal pictures are taken. Since the same load current flows through the input and output terminals, the conduction losses and efficiency can be calculated using Equations (2) and (3), respectively

$$P_{\text{loss}} = (V_{\text{in}} - V_{\text{out}})\, I_{\text{load}}, \tag{2}$$

$$\eta = \frac{P_{\text{out}}}{P_{\text{in}}} \times 100 = \frac{V_{\text{out}}}{V_{\text{in}}} \times 100, \tag{3}$$

4 Experimental Results

Two identical tests are performed for each LTG configuration under the operating conditions defined in Table 1. In each test, the electrical and thermal measurements are recorded 15 min after the MOSFETs begin conducting, allowing the device temperature to stabilize. Repeating the test provides a basic validation of measurement consistency and avoids drawing conclusions from a single experimental result.

The maximum temperature reported in this section corresponds to the highest surface temperature measured by the infrared camera and does not represent a direct measurement of the MOSFET junction temperature.

4.1 LTG0402

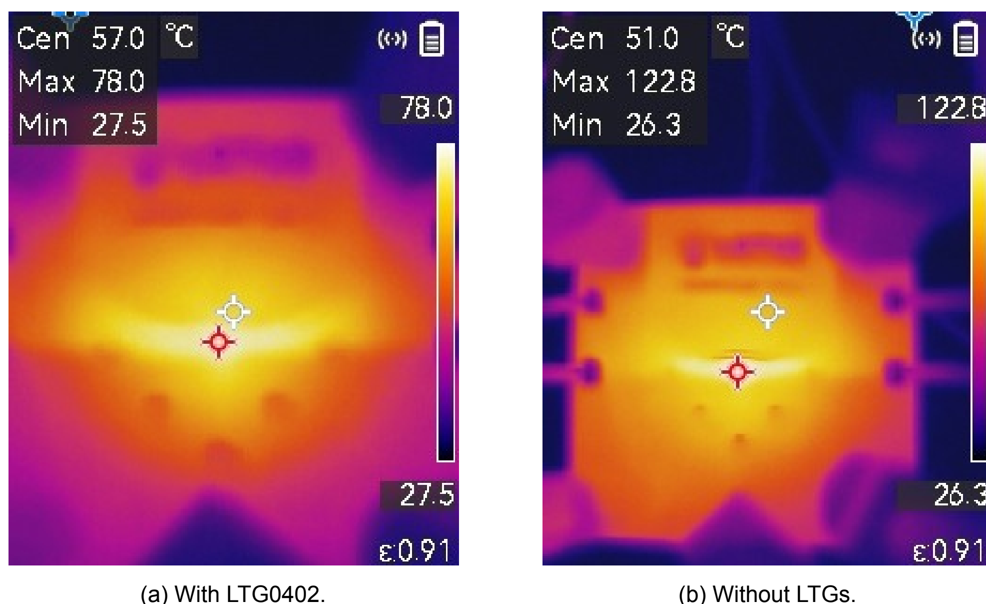
The results obtained with the LTG0402 EVB are summarized in Table 2. The two tests consistently show a reduction in the maximum MOSFET surface temperature and power loss when the LTGs are included, while increasing the overall efficiency.

Table 2: Experimental results for the LTG0402 EVB.

	Maximum surface temperature			Power loss			Efficiency		
Test	**With LTG** (°C)	**Without LTG** (°C)	ΔT (°C)	**With LTG** (W)	**Without LTG** (W)	ΔP_{loss} (W)	**With LTG** (%)	**Without LTG** (%)	$\Delta\eta$ (pp)
Test 1	78.0	122.8	44.8	2.295	2.466	0.171	94.47	94.04	0.43
Test 2	80.4	121.4	41.0	2.223	2.394	0.171	94.67	94.23	0.44

LTG0402, Test 1
The thermal images corresponding to Test 1 are presented in Figure 6. The implementation without LTGs reaches a maximum temperature of 122.8 °C, whereas the LTG0402 implementation stabilizes at 78.0 °C. This corresponds to a temperature reduction of 44.8 °C.

The measured power loss decreases by 0.171 W, from 2.466 W to 2.295 W, while the calculated efficiency increases by 0.43 percentage points.

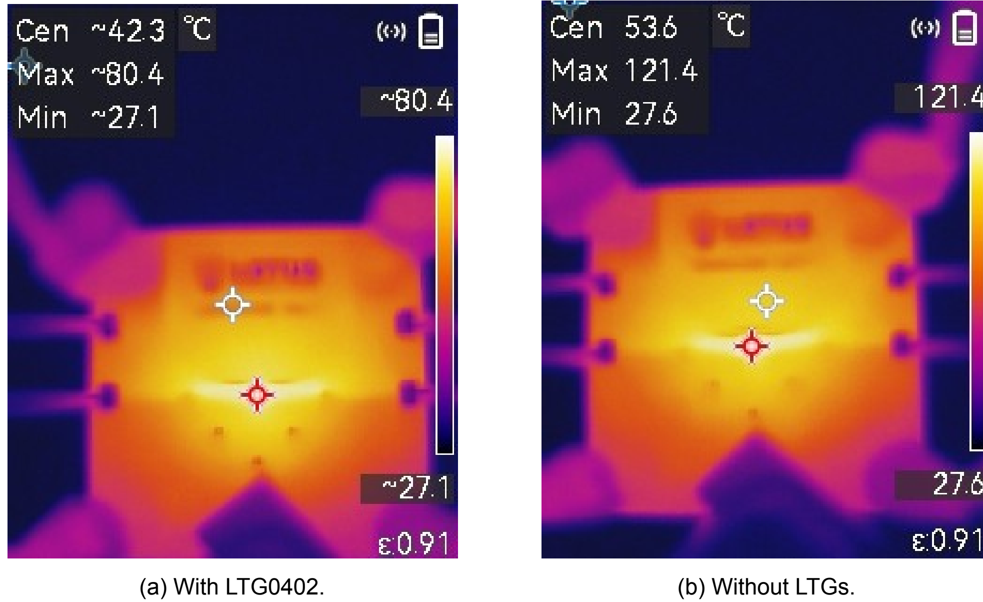


(a) With LTG0402. (b) Without LTGs.

Figure 6: LTG0402 EVB thermal measurements obtained during Test 1.

LTG0402, Test 2
Figure 7 presents the thermal images obtained during Test 2. The maximum temperature decreases from 121.4 °C without LTGs to 80.4 °C with LTG0402 devices, giving a temperature reduction of 41.0 °C.

The measured power loss decreases by 0.171 W, while the calculated efficiency increases by 0.44 percentage points.



(a) With LTG0402. (b) Without LTGs.

Figure 7: LTG0402 EVB thermal measurements obtained during Test 2.

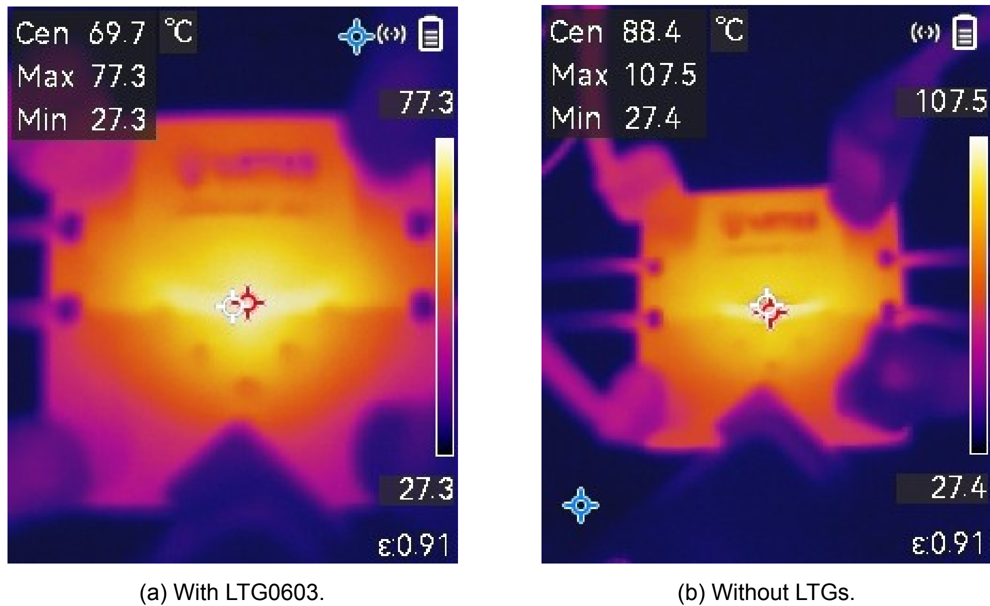
4.2 LTG0603

The LTG0603 results are summarized in Table 3. As observed for the LTG0402 implementation, all tests show a lower maximum surface temperature when the LTGs are included.

Table 3: Experimental results for the LTG0603 EVB.

Test	Maximum surface temperature			Power loss			Efficiency		
	With LTG (°C)	Without LTG (°C)	ΔT (°C)	With LTG (W)	Without LTG (W)	ΔP_{loss} (W)	With LTG (%)	Without LTG (%)	$\Delta\eta$ (pp)
Test 1	77.3	107.5	30.2	2.151	2.223	0.072	94.80	94.64	0.16
Test 2	83.4	109.6	26.2	2.205	2.268	0.063	94.66	94.57	0.09

LTG0603, Test 1
The thermal measurements obtained during Test 1 are presented in Figure 8. The maximum surface temperature decreases from 107.5 °C without LTGs to 77.3 °C with LTG0603 devices, resulting in a temperature reduction of 30.2 °C.



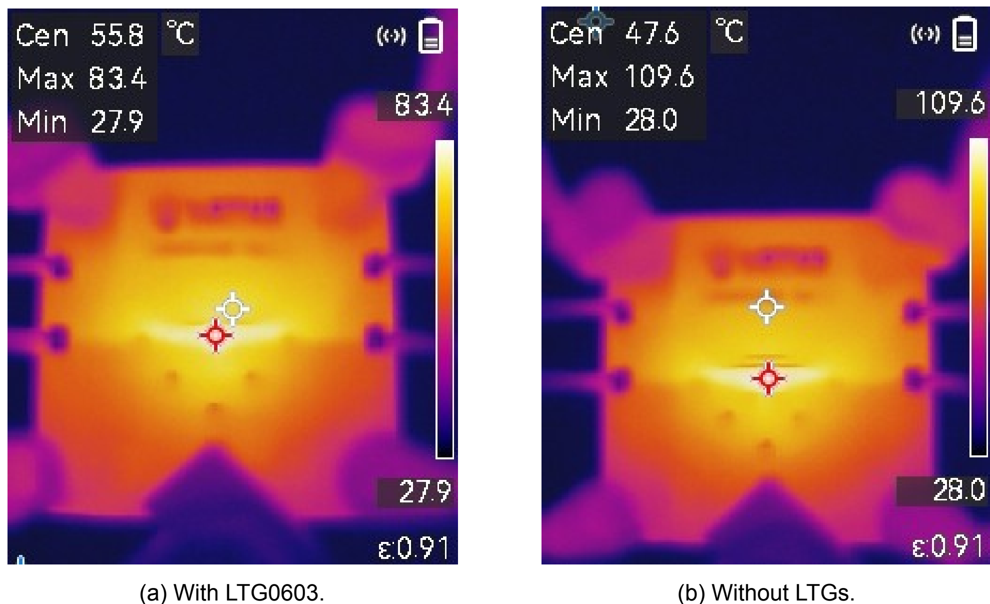
(a) With LTG0603. (b) Without LTGs.

Figure 8: LTG0603 EVB thermal measurements obtained during Test 1.

LTG0603, Test 2

Figure 9 presents the thermal measurements obtained during Test 2. The maximum surface temperature decreases from 109.6 °C to 83.4 °C, corresponding to a temperature reduction of 26.2 °C.

The power-loss reduction is 0.063 W, while the calculated efficiency increases by 0.09 percentage points.



(a) With LTG0603. (b) Without LTGs.

Figure 9: LTG0603 EVB thermal measurements obtained during Test 2.

4.3 Results Summary

The improvements obtained from the tests are summarized in Table 4. Both evaluated LTG implementations provide a consistent reduction in maximum measured device temperature and power loss.

Table 4: Average improvement obtained from Tests 1 and 2.

LTG size	$\overline{\Delta T}$	$\overline{\Delta P_{\text{loss}}}$	**Mean loss reduction**	$\overline{\Delta \eta}$
	°C	W	%	(p.p.)
LTG0402	42.9	0.171	7.04	0.44
LTG0603	28.2	0.068	3.01	0.13
LTG0805	–	–	–	–

The mean loss reduction is calculated as the average absolute reduction in power loss across Tests 1 and 2, normalized to the average power loss measured without LTGs:

$$\overline{\Delta P_{\text{loss,rel}}} = \frac{\frac{1}{n}\sum_{i=1}^{n}\left(P_{\text{loss,without},i} - P_{\text{loss,with},i}\right)}{\frac{1}{n}\sum_{i=1}^{n} P_{\text{loss,without},i}} \times 100, \tag{4}$$

where $n = 2$ for the two tests considered.

Figure 10 compares the maximum surface temperatures with and without LTGs for all completed experiments.

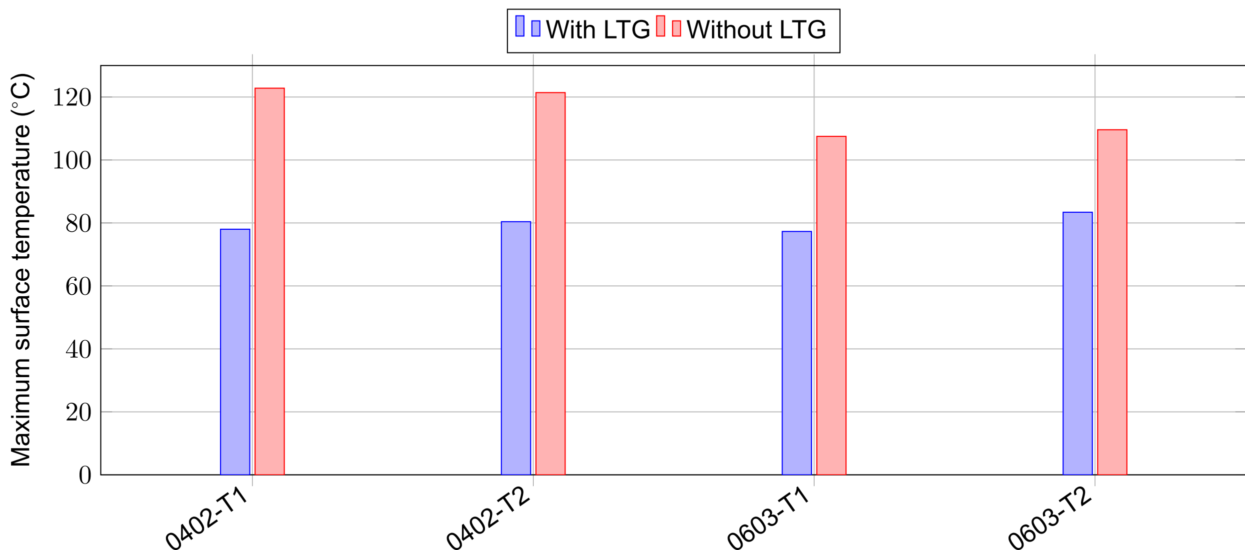


Figure 10: Maximum surface temperature with and without LTGs during Tests 1 and 2.

Figure 11 directly compares the temperature reduction achieved during Tests 1 and 2.

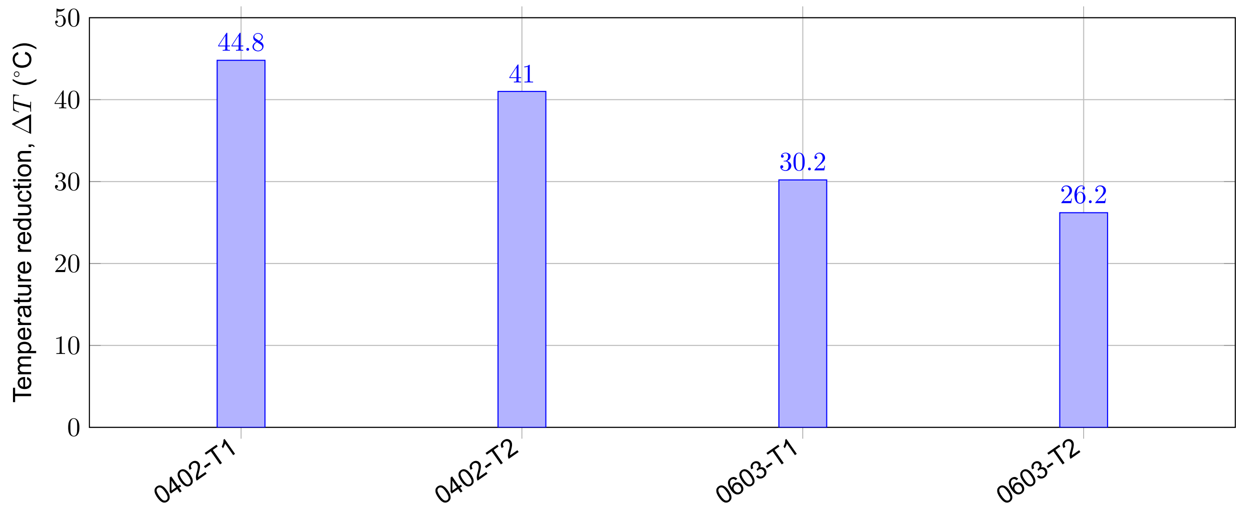


Figure 11: Reduction in maximum surface temperature caused by the LTGs during Tests 1 and 2.

Figure 12 compares the power losses with and without LTGs during Tests 1 and 2.

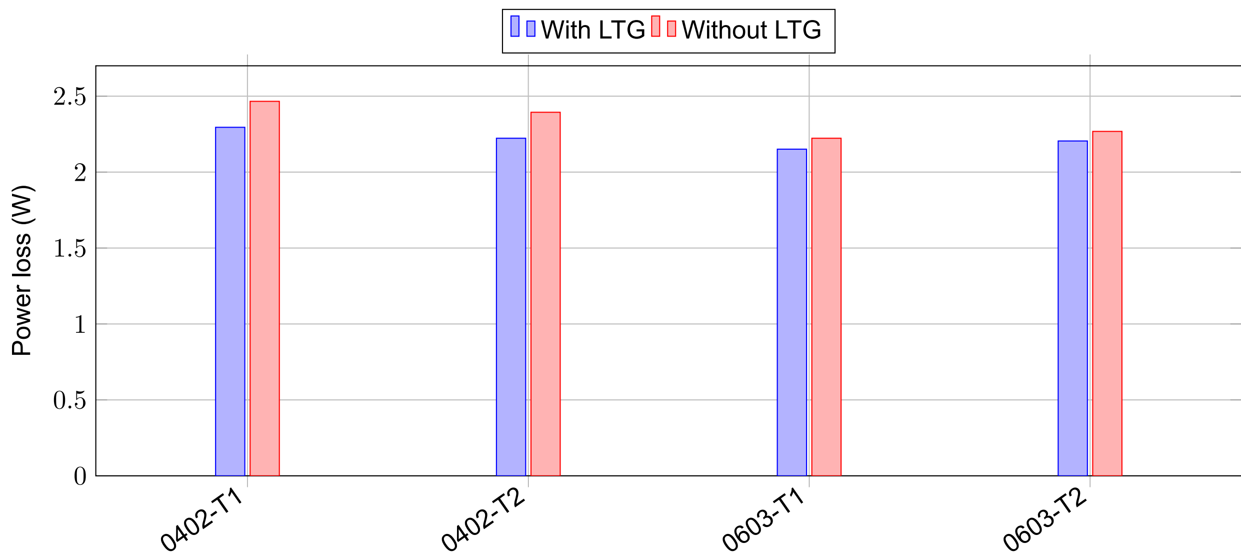


Figure 12: Calculated power loss with and without LTGs during Tests 1 and 2.

5 Conclusion

The experimental results demonstrate that the integration of LTGs improves the thermal performance of the common-drain dual MOSFET. For the LTG0402 implementation, the device surface-temperature reductions are 44.8 °C in Test 1 and 41.0 °C in Test 2, corresponding to an average reduction of 42.9 °C. For the LTG0603 implementation, the reductions are 30.2 °C in Test 1 and 26.2 °C in Test 2, resulting in an average reduction of 28.2 °C. The larger improvement obtained with LTG0402 is particularly relevant because this implementation uses the smallest drain-connected copper area, demonstrating a clear advantage for space-constrained, power-dense compact electronic systems.

The lower operating temperature also reduces conduction losses and improves efficiency. For LTG0402, the mean conduction-loss reduction is 7.04 %, while the efficiency increases by 0.43 and 0.44 percentage points in Tests 1 and 2, respectively, corresponding to an average improvement of approximately 0.44 percentage points. For LTG0603, the mean conduction-loss reduction is 3.01 %, while the efficiency increases by 0.16 and 0.09 percentage points, resulting in an average improvement of approximately 0.13 percentage points. These improvements can reduce thermal stress, limit the temperature-dependent increase in $R_{DS(on)}$, improve component reliability and lifetime, reduce cooling requirements, and enable higher power density in space-constrained designs.

6 Changelog

Revision Number	Revision Date	Description	Sections Changed
1.0	2026-07-06	Initial release	-

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