DESCRIPTION

LTG devices from Lotus Microsystems are thermally conductive yet electrically isolated, silicon-based thermal jumpers.

These devices are designed to guide heat away from hot electronic components, toward heat sinks or cooler areas (such as ground planes), without establishing an electrical connection.

LTG devices significantly enhance thermal conductivity, particularly in scenarios with limited or no direct access to a ground plane or heat sink, such as high-side switches in a half-bridge configuration.

Silicon, as an alternative to traditional ceramic materials, offers a cost-effective substrate with high thermal conductivity and excellent thermo-mechanical properties and reliable processing. By improving thermal management, LTG devices help reduce component temperatures, supporting higher circuit reliability and longer service life.

FEATURES

- High thermal conductivity, up to 140 W/(m K)
- High electrical isolation resistance
- Low parasitics
- High precision standard package dimensions
- Low coefficient of thermal expansion (CTE)
- RoHS compliant

APPLICATIONS

- High-power LEDs
- Pin and laser diodes
- Power converters and amplifiers
- xPU and FPGA boards
- Semiconductor packages
- Optical Transceivers

Abstract

This application note evaluates the use of Lotus Microsystems Thermal Guide (LTG) devices to improve the thermal management of a common-drain dual MOSFET configuration. LTGs provide an electrically isolated thermal path between the active drain region and a larger grounded copper area, enabling heat to be dissipated without increasing the size of the electrically active node. Evaluation boards using LTG0402, LTG0603, and LTG0805 devices are developed. The LTG0402 and LTG0603 implementations are experimentally characterized using infrared thermal imaging after 5 min and 15 min of continuous operation, while the LTG0805 implementation remains under development. The LTG0402 implementation achieves maximum measured surface-temperature reductions of 29.0 °C and 30.8 °C after 5 min and 15 min, respectively. The corresponding reductions obtained with the LTG0603 implementation are 30.8 °C and 29.5 °C. After 15 min, both LTG-equipped EVBs remain at approximately 95 °C, while their corresponding reference EVBs without LTGs reach approximately 125 °C to 126 °C. The results demonstrate that LTGs provide a substantial and sustained reduction in the maximum MOSFET surface temperature, particularly in compact PCB layouts where the available drain-connected copper area is limited.

Figure 1: LTG 3D package representation.

Contents

1 Application Description

Multiple compact electronic systems rely on dual MOSFET devices to implement functionalities such as bidirectional switching, reverse-current blocking or battery protection. These devices can use either common-drain or common-source configurations. The dual MOSFET device evaluated in this application uses the common-drain configuration shown in Figure 2.

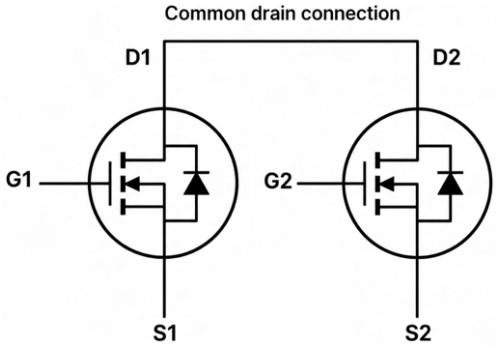


Figure 2: Common-drain configuration.

The increasing power density and reduced package dimensions of modern MOSFETs lead to highly concentrated heat generation. Thermal management becomes particularly challenging when the electrically active drain node cannot be directly connected to a grounded heatsink or to a large cooling plane. Under these conditions, the available copper may be insufficient to spread the generated heat effectively, leading to higher MOSFET temperatures, increased conduction losses, reduced overall system efficiency, and accelerated component ageing that may shorten the device lifetime.

Lotus Microsystems Thermal Guides (LTG) can provide an electrically isolated thermal path between the MOSFET and a lower-temperature, larger copper area. This allows heat to be transferred away from the electrically active nodes without creating a conductive connection between the two regions.

This application note evaluates the performance of LTGs when integrated with a common-drain dual MOSFET. Three evaluation boards (EVBs) are developed using LTG0402, LTG0603, and LTG0805 devices, respectively. Each board uses the same MOSFET and the same number of LTGs, enabling to experimentally assess the thermal performance of the three different implementations.

2 Operating Principle

As presented in Figure 2, two N-channel MOSFETs can be connected in a common-drain configuration. When both devices are turned on, current flows through the two MOSFETs connected in series. The resulting conduction losses can be approximated as:

$$P_{\text{loss,cond}} \approx I^2 \left(R_{\text{DS(on),1}} + R_{\text{DS(on),2}} \right), \tag{1}$$

When the MOSFETs are turned off, their opposing body diodes prevent continuous current flow in either direction. Since $R_{DS(on)}$ typically increases with junction temperature, insufficient heat extraction can increase both the device temperature and its conduction losses.

A larger common-drain copper area would improve heat spreading, but it would also increase the size of the electrically active drain node. The proposed approach keeps this drain node compact while transferring its heat to a larger grounded copper plane through electrically isolated LTG devices. Consequently, the ground plane can be used as an extended heat-spreading area without increasing the physical size of the drain node.

3 Evaluation Method

3.1 Experimental Test Setup

The experimental setup consists of a power supply connected to the board input, two supplies used to turn on the MOSFETs, and an electronic load connected at the output controlling the load current. Figure 3 shows the circuit diagram of the presented test setup.

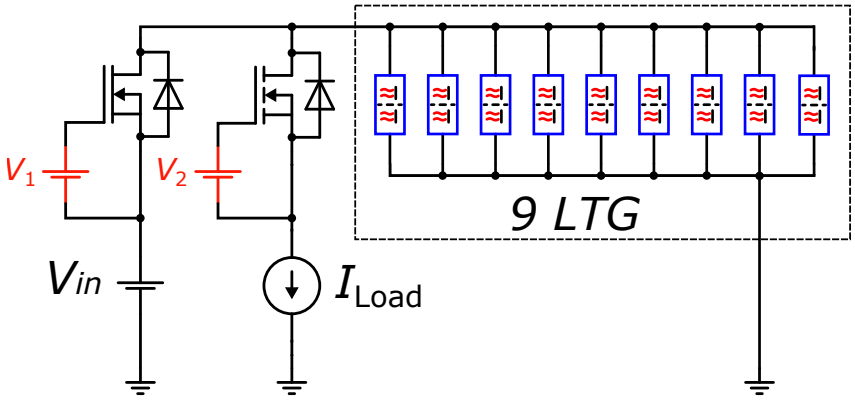
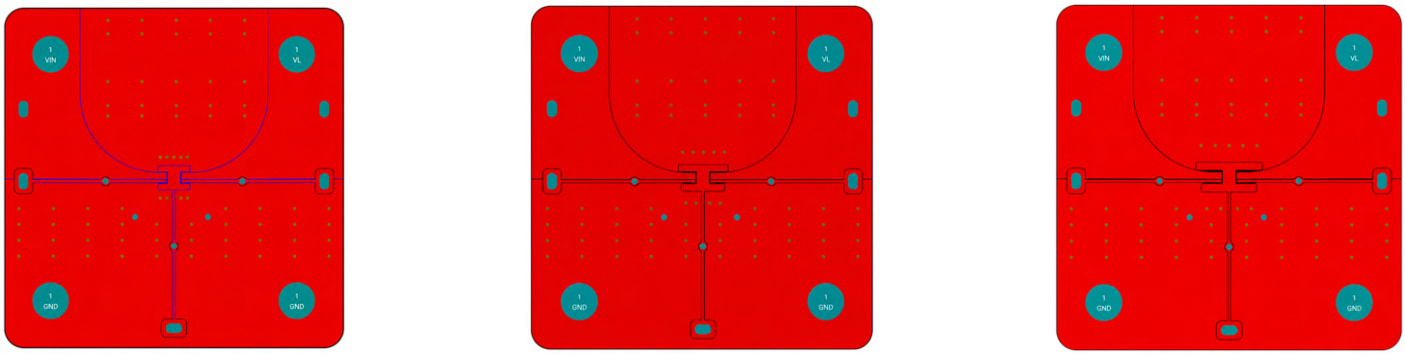


Figure 3: Schematic diagram of the experimental test setup.

3.2 Evaluation Board

Three EVBs are developed to assess the performance of the dual MOSFET using different LTG package sizes: LTG0402, LTG0603, and LTG0805. For each package size, the performance of the EVB incorporating LTGs is compared with that of the same EVB without LTGs. The LTG0402 and LTG0603 implementations are fabricated and experimentally evaluated, whereas the LTG0805 implementation is currently under development.

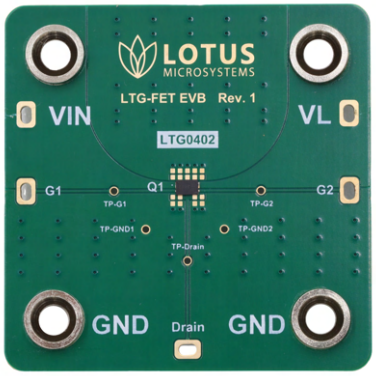
In all implementations, the same circuit topology and the same number of LTGs are used. However, the larger footprints of the LTG0603 and LTG0805 devices require a correspondingly larger copper area connected to the common-drain node. This effect is illustrated in Figure 4. Since the additional drain-connected copper also contributes to heat spreading, a direct comparison between LTG package sizes is not fully independent of the PCB layout. Therefore, each implementation is primarily evaluated against its corresponding reference EVB without LTGs.



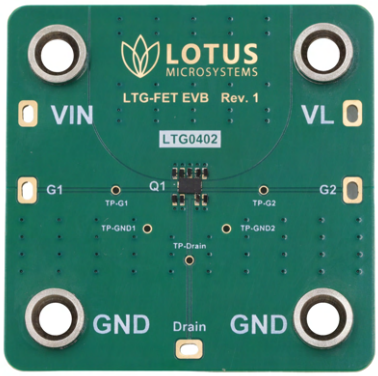
(a) LTG0402 EVB layout. (b) LTG0603 EVB layout. (c) LTG0805 EVB layout.

Figure 4: Top-layer PCB layouts for the three LTG package sizes.

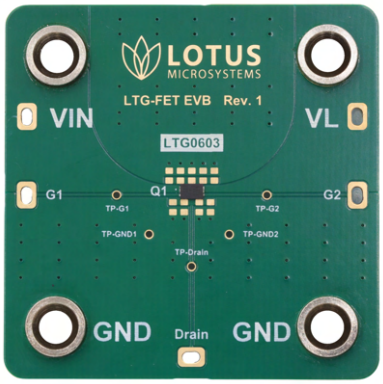
The selection of a particular LTG package ultimately depends on the thermal, electrical, and layout constraints of the target application. Figure 5 presents the LTG0402 and LTG0603 EVBs used in the experimental evaluation.



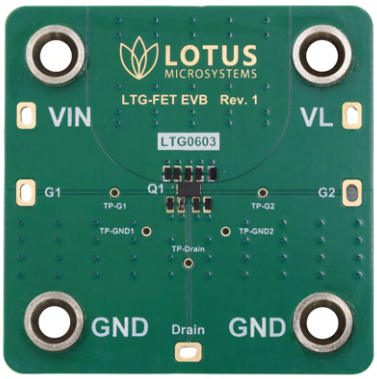
(a) LTG0402 EVB without LTGs.



(b) LTG0402 EVB with LTGs.



(c) LTG0603 EVB without LTGs.



(d) LTG0603 EVB with LTGs.

Figure 5: LTG0402 and LTG0603 EVBs used in the experimental evaluation.

3.3 Measurement Procedure

The operating conditions applied to all EVBs are summarized in Table 1. The same electrical operating point and thermal-camera configuration are used for the EVBs with and without LTGs.

Table 1: Experimental operating and measurement conditions.

Parameter	Symbol / Mode	Value
Input power supply voltage	V_{in}	5 V
MOSFET 1 gate-to-source voltage	V_{GS1}	4.5 V
MOSFET 2 gate-to-source voltage	V_{GS2}	4.5 V
Load current	I_{load}	9 A
Measurement times	t_{meas}	5 min, 15 min

4 Experimental Results

For each LTG implementation, the corresponding EVBs with and without LTGs are operated continuously under the conditions defined in Table 1. During each test, measurements are recorded after 5 min and 15 min of operation.

The first measurement characterizes the thermal behavior of the EVB during the initial operating period, after the fastest thermal

transient has subsided. The second measurement evaluates its behavior after a longer thermal-settling period and determines whether the effect of the LTGs is maintained during extended operation.

Thermal images are recorded at both measurement points. The maximum temperature reported in this section corresponds to the highest surface temperature measured by the infrared camera and does not represent a direct measurement of the MOSFET junction temperature.

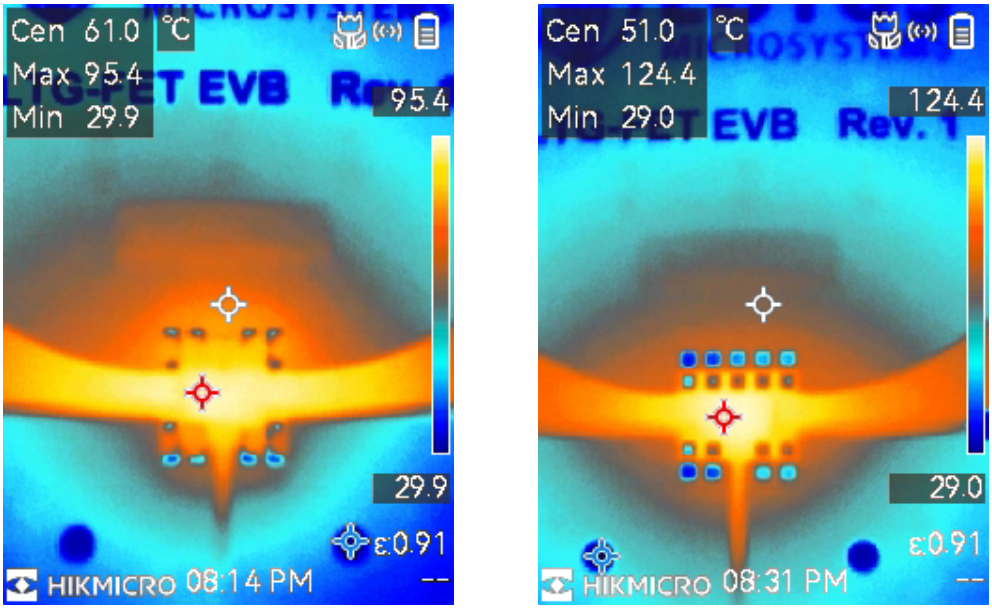
4.1 LTG0402

The results obtained with the LTG0402 EVB are summarized in Table 2. The measurements consistently show a reduction in the maximum MOSFET surface temperature when the LTGs are included.

Table 2: Experimental thermal results for the LTG0402 EVB.

Measurement time	**With LTGs** (°C)	**Without LTGs** (°C)	ΔT (°C)
5 min	95.4	124.4	29.0
15 min	95.3	126.1	30.8

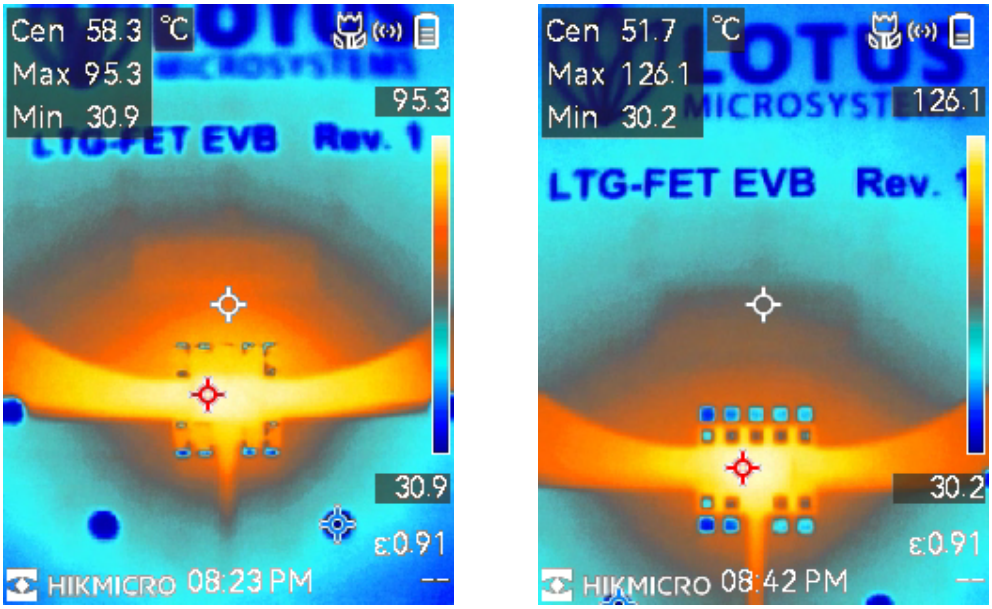
LTG0402, Measurements after 5 min of operation
The thermal images corresponding to the first measurements are presented in Figure 6. The maximum temperature decreases from 124.4 °C without LTGs to 95.4 °C with LTG0402 devices. This corresponds to a temperature reduction of 29.0 °C.



(a) With LTG0402. (b) Without LTGs.

Figure 6: LTG0402 EVB thermal measurements obtained after 5 min of operation.

LTG0402, Measurements after 15 min of operation
Figure 7 presents the thermal images obtained after 15 min of operation. The maximum temperature decreases from 126.1 °C without LTGs to 95.3 °C with LTG0402 devices, giving a temperature reduction of 30.8 °C.



(a) With LTG0402.

(b) Without LTGs.

Figure 7: LTG0402 EVB thermal measurements obtained after 15 min of operation.

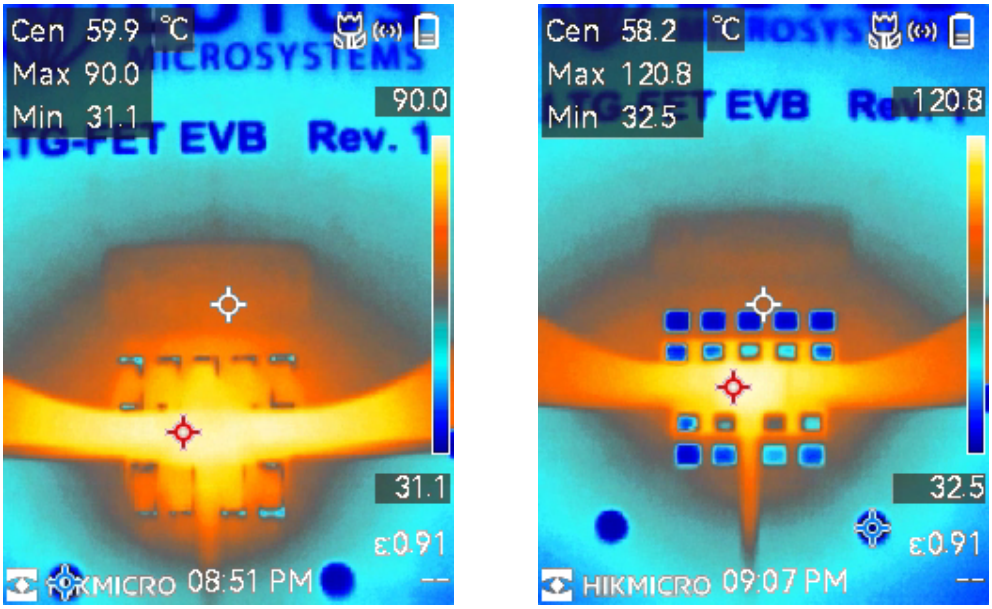
4.2 LTG0603

The LTG0603 results are summarized in Table 3. As observed for the LTG0402 implementation, both measurement points show a lower maximum surface temperature when the LTGs are included.

Table 3: Experimental thermal results for the LTG0603 EVB.

Measurement time	**With LTGs** (°C)	**Without LTGs** (°C)	ΔT (°C)
5 min	90.0	120.8	30.8
15 min	95.2	124.7	29.5

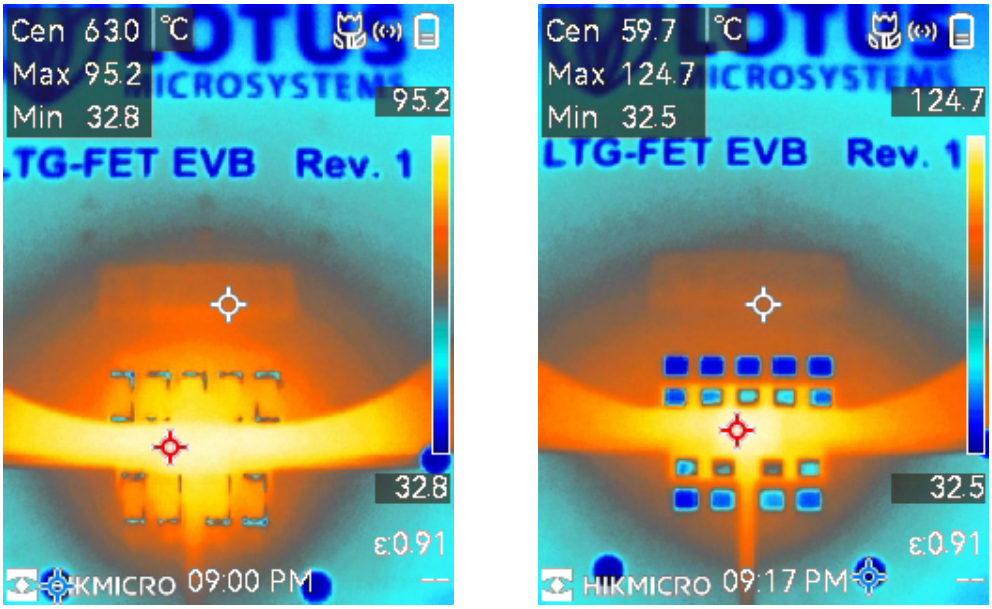
LTG0603, Measurements after 5 min of operation
The thermal images corresponding to the first measurement point are presented in Figure 8. The maximum surface temperature decreases from 120.8 °C without LTGs to 90.0 °C with LTG0603 devices, resulting in a temperature reduction of 30.8 °C.



(a) With LTG0603. (b) Without LTGs.

Figure 8: LTG0603 EVB thermal measurements obtained after 5 min of operation.

LTG0603, Measurements after 15 min of operation
The maximum surface temperature decreases from 124.7 °C without LTGs to 95.2 °C with LTG0603 devices, corresponding to a temperature reduction of 29.5 °C.



(a) With LTG0603. (b) Without LTGs.

Figure 9: LTG0603 EVB thermal measurements obtained after 15 min of operation.

4.3 Results Summary

The thermal improvements obtained at both measurement points are summarized in Table 4. All measurements show a substantial reduction in the maximum measured MOSFET surface temperature when LTGs are incorporated. Across the two evaluated LTG implementations and both measurement points, the temperature reduction remains between 29.0 °C and 30.8 °C.

Table 4: Maximum surface-temperature reduction provided by each LTG implementation.

LTG size	ΔT **after 5 min**	ΔT **after 15 min**
	°C	°C
LTG0402	29.0	30.8
LTG0603	30.8	29.5

After 15 min of continuous operation, the maximum surface temperatures measured with the LTG0402 and LTG0603 implementations are 95.3 °C and 95.2 °C, respectively. Their corresponding reference EVBs without LTGs reach 126.1 °C and 124.7 °C.

The practical significance of these results is that the approximately 30 °C temperature reduction is achieved without increasing the size of the electrically active common-drain node. By providing an electrically isolated thermal path, the LTGs decouple the heat-spreading area from the electrical node and allow a larger grounded copper plane to be used for heat dissipation. This provides additional thermal-design flexibility while preserving a compact common-drain layout.

Since the LTG0402 and LTG0603 layouts require different common-drain copper areas, the results should primarily be interpreted as paired comparisons between each LTG-equipped EVB and its corresponding reference board. Consequently, they are not intended to provide a direct performance ranking between LTG package sizes.

Figure 10 compares the maximum surface temperatures measured with and without LTGs at both measurement points. Figure 11 presents the corresponding temperature reductions.

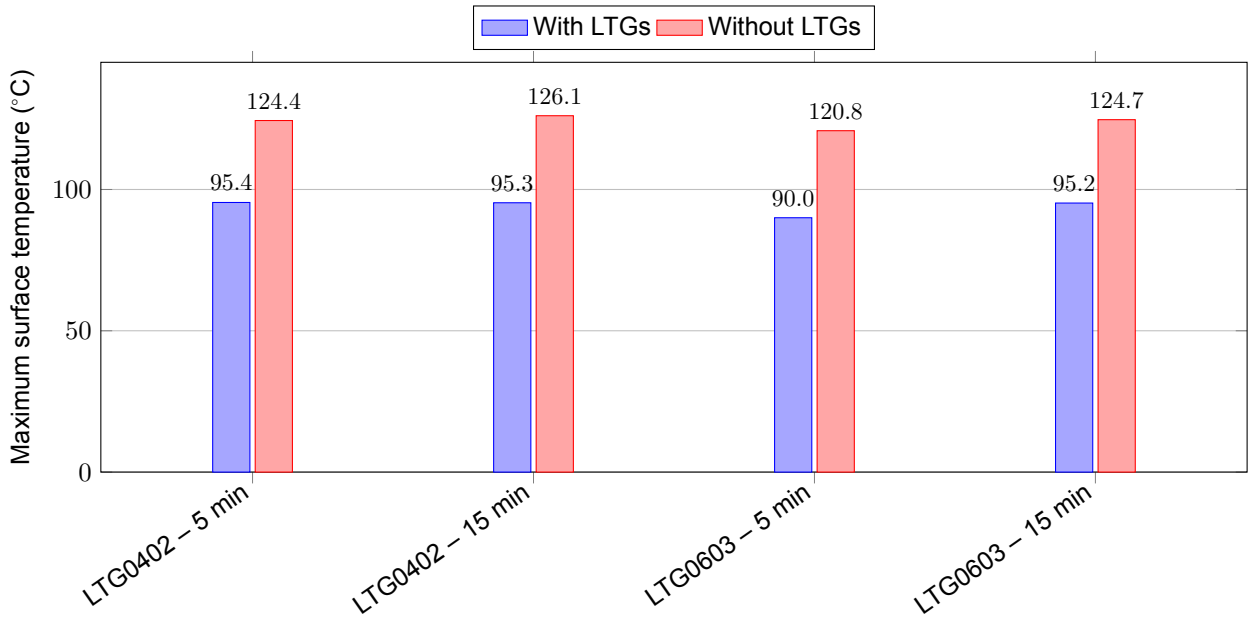


Figure 10: Maximum surface temperature measured with and without LTGs after 5 min and 15 min of operation.

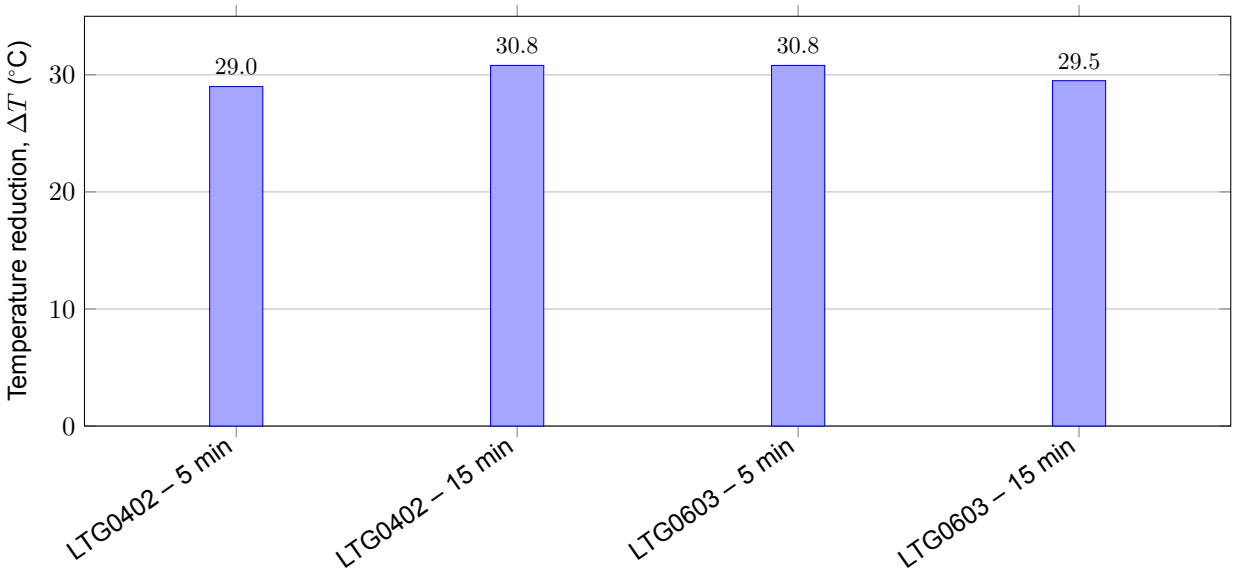


Figure 11: Reduction in maximum surface temperature provided by the LTGs after 5 min and 15 min of operation.

5 Conclusion

The experimental results demonstrate that the integration of LTGs substantially improves the thermal performance of the common-drain dual MOSFET. For the LTG0402 implementation, the maximum measured temperature reductions are 29.0 °C after 5 min and 30.8 °C after 15 min. For the LTG0603 implementation, the corresponding reductions are 30.8 °C and 29.5 °C. After 15 min of continuous operation, the LTG0402 and LTG0603 EVBs reach maximum surface temperatures of 95.3 °C and 95.2 °C, respectively, while their corresponding reference EVBs without LTGs reach 126.1 °C and 124.7 °C. The close agreement between the reductions obtained at both measurement points demonstrates that the thermal improvement is maintained during extended operation.

Since the LTG0402 and LTG0603 implementations use different drain-connected copper areas, the results should be interpreted as paired comparisons between each LTG-equipped EVB and its corresponding reference board, rather than as a direct performance ranking between LTG package sizes. Nevertheless, the LTG0402 results are particularly significant. Despite using the smallest drain-connected copper area among the evaluated layouts, this implementation provides a sustained maximum surface-temperature reduction of approximately 30 °C.

This result highlights the principal advantage of the LTG approach: substantial heat spreading can be achieved without enlarging the electrically active common-drain node. By providing an electrically isolated thermal path, the LTGs allow the MOSFET heat to be transferred to a larger grounded copper plane, effectively decoupling the available heat-spreading area from the electrical and layout constraints of the drain node. This capability is especially valuable in compact and power-dense systems, where increasing the active copper area may be impractical or undesirable.

The resulting reduction in operating temperature can reduce thermal stress, limit the temperature-dependent increase in $R_{DS(on)}$, improve component reliability and lifetime, reduce cooling requirements, and provide additional margin for higher load current or greater power density. Therefore, LTGs offer not only a reduction in device temperature, but also increased freedom in the electrical, thermal, and mechanical design of space-constrained electronic systems.

6 Changelog

Revision Number	Revision Date	Description	Sections Changed
1.0	2026-07-06	Initial release	-
1.1	2026-07-23	Updated thermal images for better resolution	Section 3.3 Section 4 Section 4.3 Section 5

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