DESCRIPTION

The LMU20P1 is a miniaturized step-up Power Supply in Package (PSiP) offering small size and high efficiency. The PSiP includes an integrated switching controller, FETs, and an inductor in a compact 6-pin LGA package (2 mm × 2 mm × 0.75 mm), optimized for automated assembly by standard surface-mount pick-and-place equipment.

The LMU20P1 has a light-load efficiency enhancement function to achieve high efficiency across a wide load range and features a range of protection circuits that include soft start, over-temperature protection, short-circuit protection, and cycle-by-cycle current limit. The LMU20P1 has up to 92 % efficiency and up to 80 % efficiency at 100 µA load.

The LMU20P1 offers exceptionally low near-field radiation levels and a proprietary start-up circuit to minimize input inrush current.

FEATURES

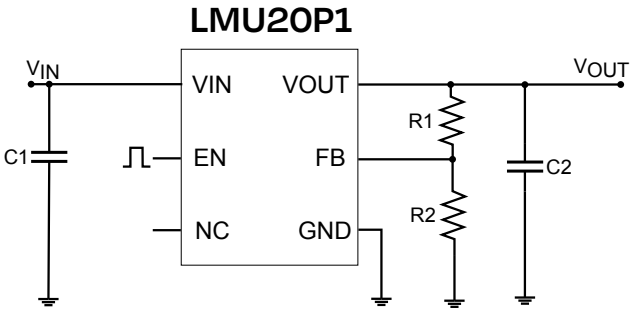
- Fully integrated boost converter with inductor
- 0.5 V - 1.6 V input range[a]
- 1.4 V - 1.8 V output range
- 100 mA load continuous range
- Up to 92% efficiency
- 5 MHz switching frequency (PWM)
- PFM light load deviceModel
- 2 mm x 2 mm 6-pin LGA Package
- 0.75 mm maximum profile
- internal loop compensation
- Soft-start, OTP, SCP
- RoHS compliant

APPLICATIONS

- Hearing aids and wearables
- IoT sensors
- Singlel- and double-cell PV applications

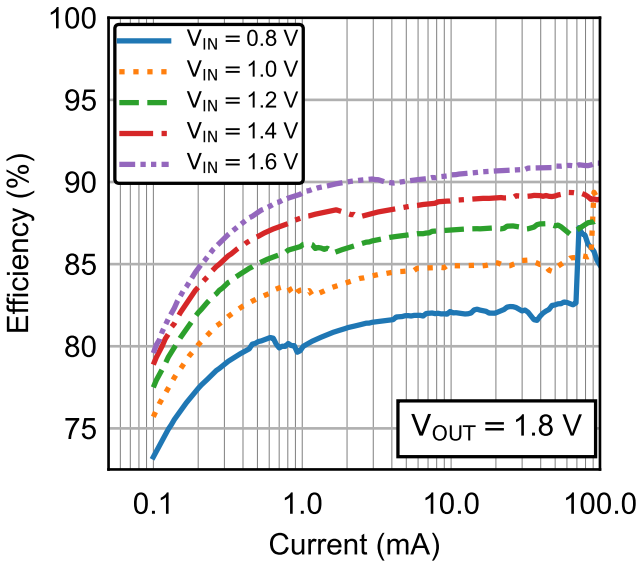
[a]Derating below 0.8 V

Typical Application



- C1 is the input capacitor
- C2 is the output capacitor
- R1 and R2 are the feedback resistors

Efficiency



Contents

1 Absolute Maximum Rating

[1] All pins to GND ..... 0.2 V to 1.98 V
Operating Temperature Range ..... −40 °C to 85 °C
Junction Temperature Range ..... −40 °C to 150 °C
Maximum Reflow Temperature ..... 260 °C

2 Electrical Characteristics

All values are measured or simulated at T_A = 25 °C , $C_{IN} = C_{OUT}$ = 10 µF , $V_{IN} = V_{EN}$ = 1.5 V , V_{OUT} = 1.6 V , Load = 18 Ω , unless otherwise specified.

Table 1

Parameter	Symbol	Conditions & Notes	Min	Typ	Max	Unit
Input Quiescent Current	$I_{Q\_in\_SD}$	EN=LOW		0.18		µA
	$I_{Q\_in\_NSW}$	EN=HIGH, non-switching		0.7		µA
Input Voltage Range	V_{IN}	Derating at high load below 0.8 V	0.5		1.6 V	V
Min. input Start-up voltage	V_{IN_STRT}			0.8		V
Enable Voltage Threshold	V_{EN_HTL}	HIGH to LOW	0.3	0.5		V
	V_{EN_LTH}	LOW to HIGH		0.6	0.8	V
Enable Pin Leakage	I_{EN_LK}	V_{EN} = 1.6 V		0.5		V
Feedback Pin Leakage	I_{FB_LK}	V_{EN} = 1.6 V		0.5		V
Switching Frequency	f_{SW}			5.0		MHz
Feedback Voltage Reference	V_{REF}		394	400	407	mV
Output Quiescent Current	$I_{Q\_OUT\_NSW}$	EN = HIGH, non-switching		15		µA
Output Voltage Range	V_{OUT}		1.4		1.8	V
Output Current Limit	I_{OUT_LIM}		100			mA
Output Voltage Accuracy	$V_{OUT\_ACC\_PWM}$	PWM (Does not include feedback resistors tolerance)			2	%

[1] Exposing the device to conditions beyond what is listed under “Absolute maximum ratings” may affect the reliability of the device or cause permanent damage.

3 Pin Configuration and Function

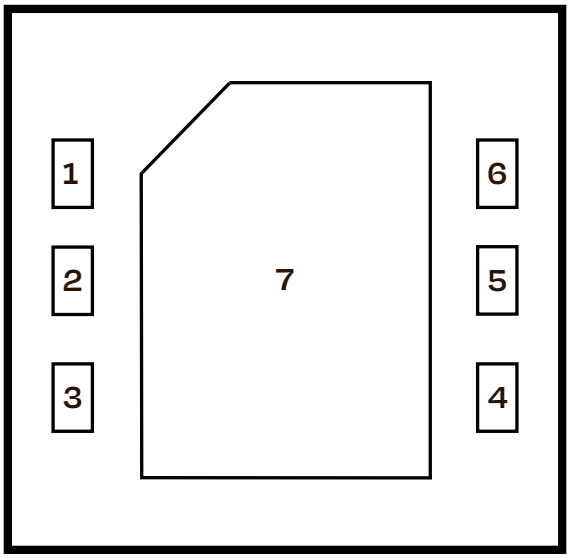


Figure 1: LMU20P1 Top View

Table 2: Pin definitions

Pin	Name	Description
1	NC	Do Not Connect
2	GND	Power and signal ground
3	VIN	Input voltage pin. Connect to the input capacitor
4	EN	Enable pin. Connect to logic HIGH for normal operation
5	FB	Feedback pin. Connect to VOUT through a resistor divider
6	VOUT	Output voltage pin. Connect to the output capacitor
7	GND	Thermal pad. Internally connected to ground

4 Functional Block Diagram

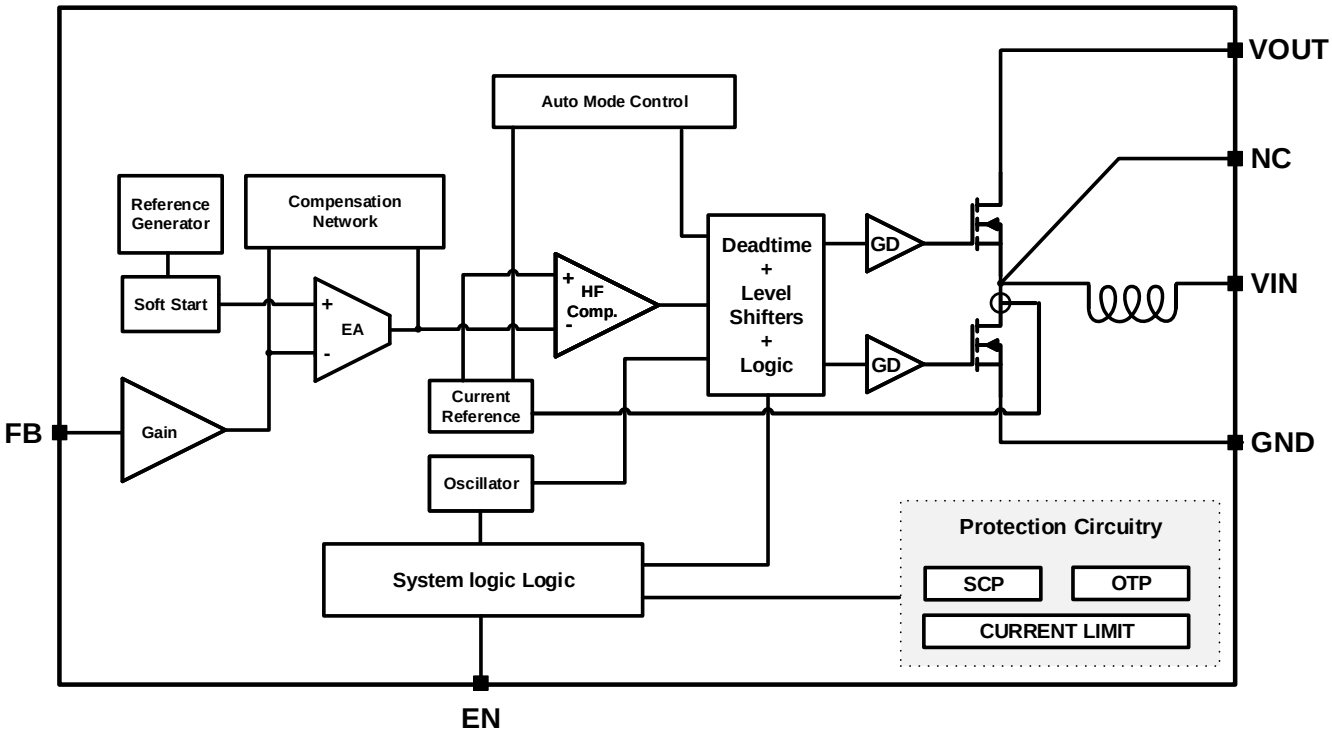


Figure 2: Functional block diagram

5 Typical Performance Characteristics

All values are measured or simulated at T_A = 25 °C , $C_{IN} = C_{OUT}$ = 10 µF unless otherwise specified.

Efficiency

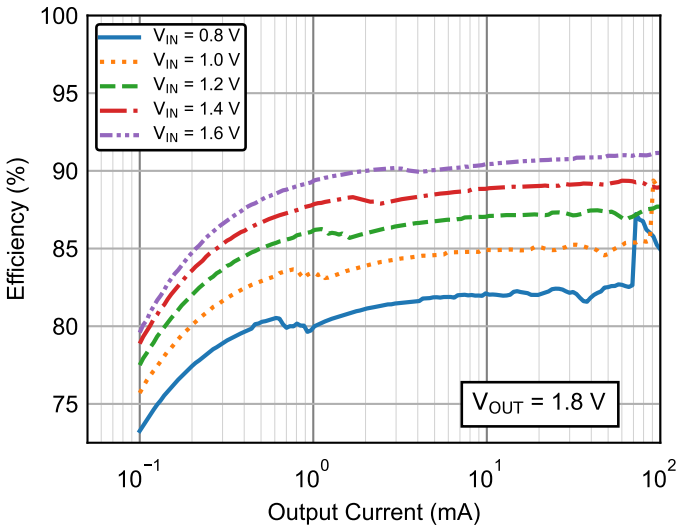


Figure 3(a)

Efficiency

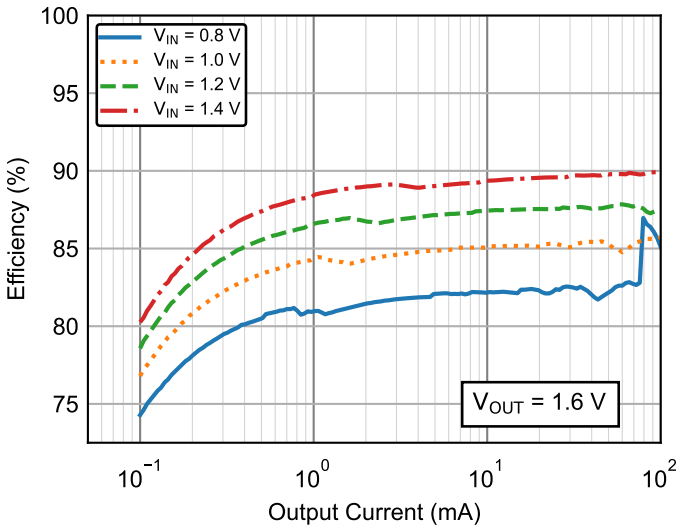


Figure 3(b)

Line/Load Regulation

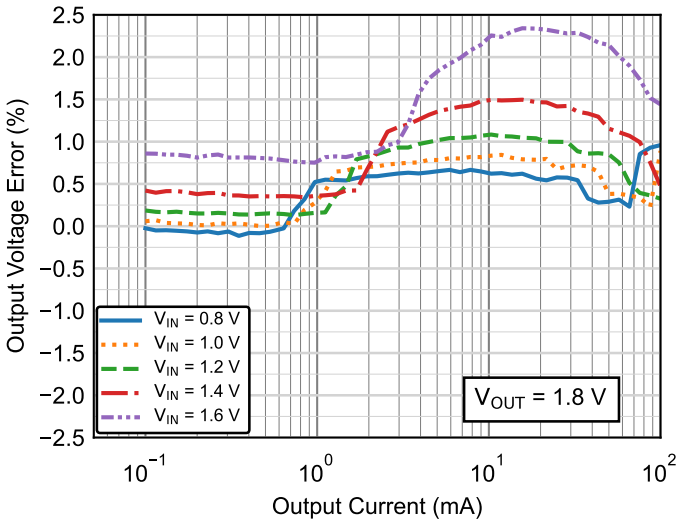


Figure 3(c)

Line/Load Regulation

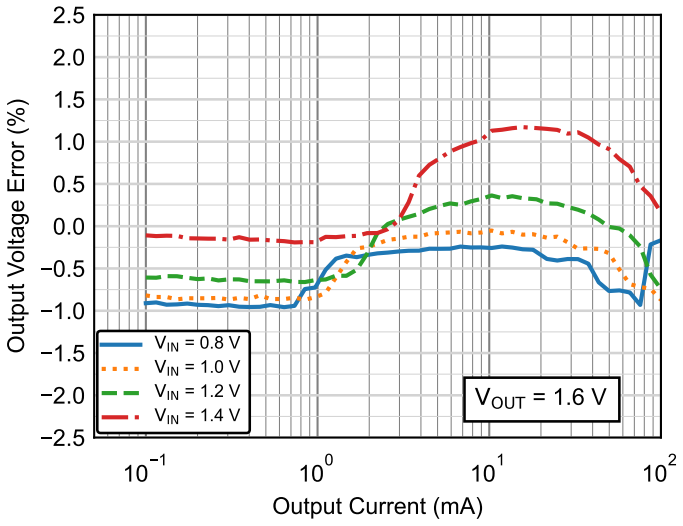


Figure 3(d)

V_{OUT} Ripple Waveform (PWM)

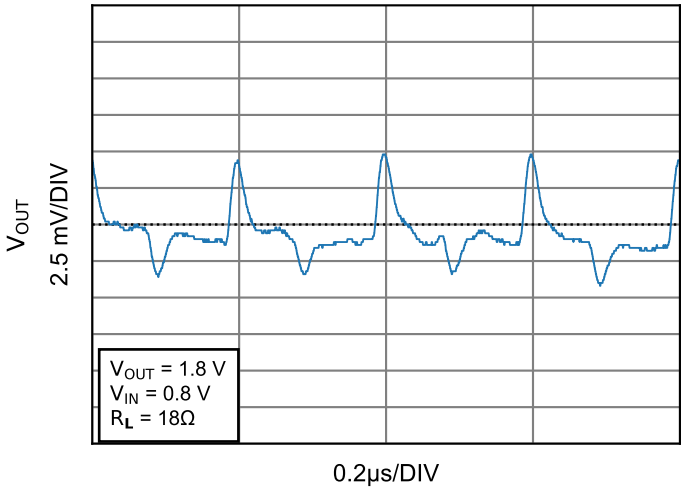


Figure 3(e)

V_{OUT} Ripple Waveform (PFM)

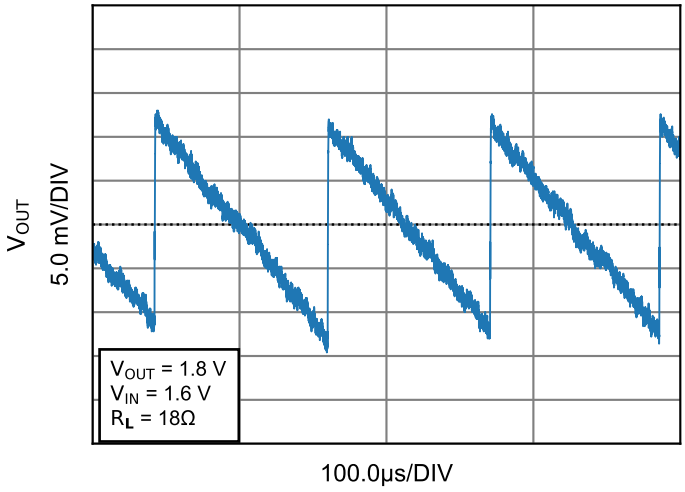


Figure 3(f)

PFM/PWM Current Threshold

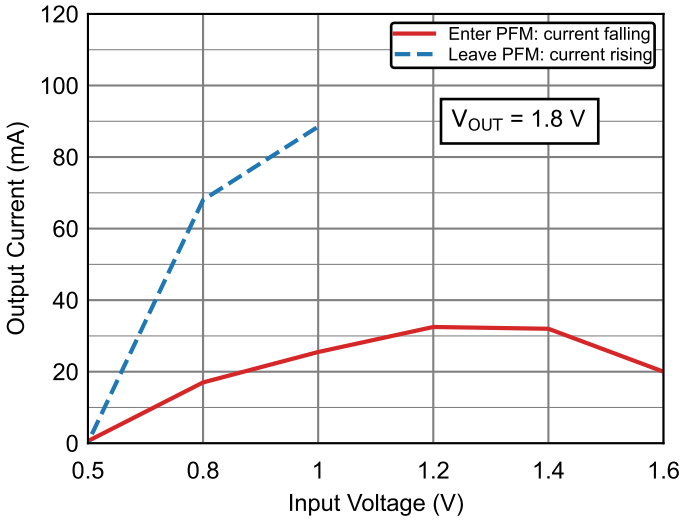


Figure 3(g)

PFM/PWM Current Threshold

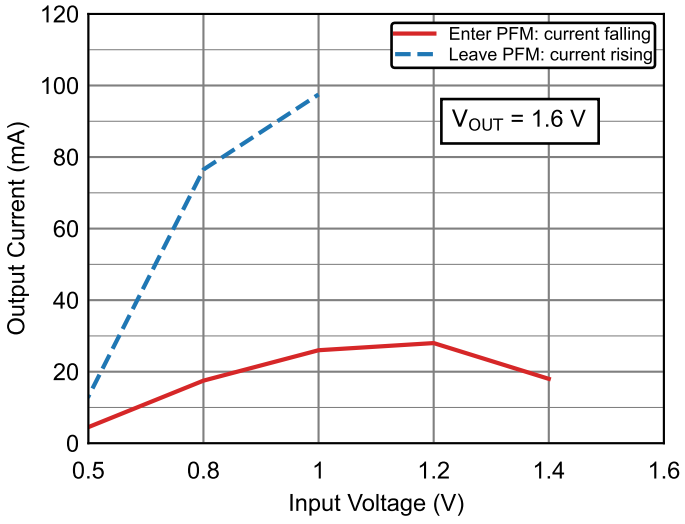
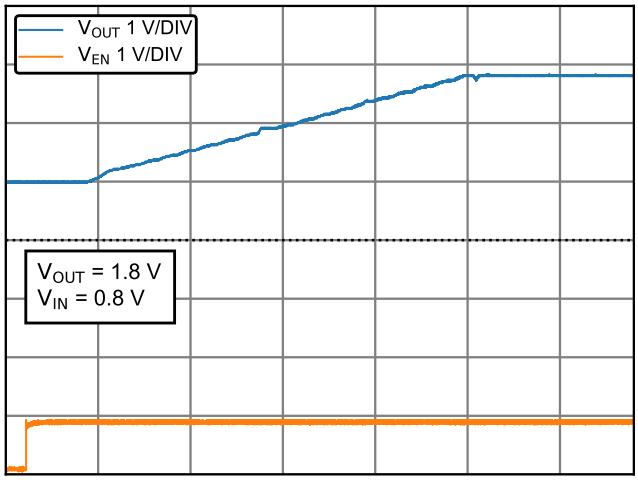


Figure 3(h)

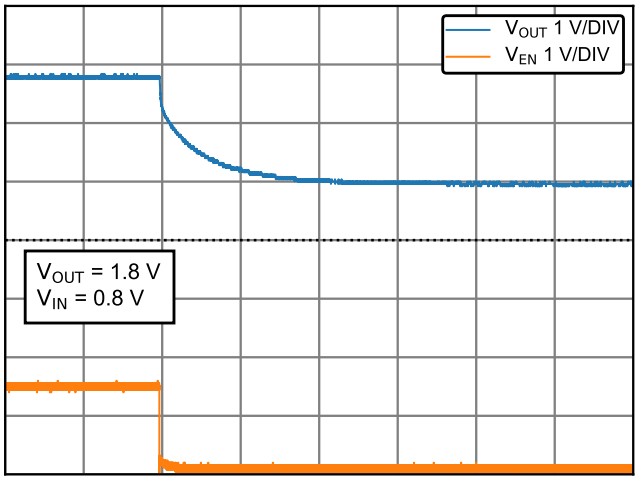
V_{OUT} and Start-Up Waveform



0.5 ms/DIV

Figure 3(i)

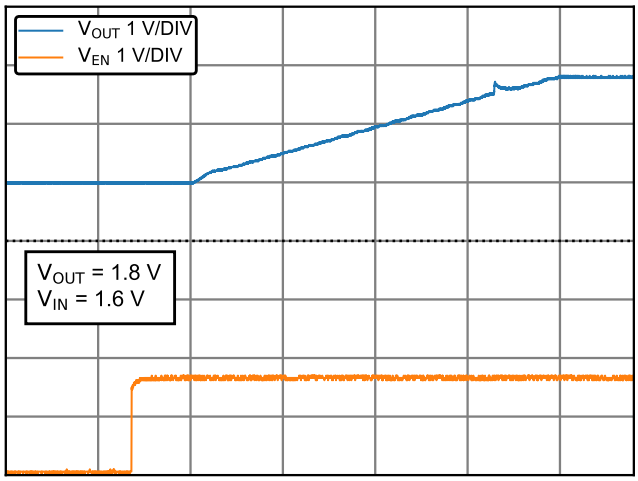
V_{OUT} and Shutdown Waveform



0.25 ms/DIV

Figure 3(j)

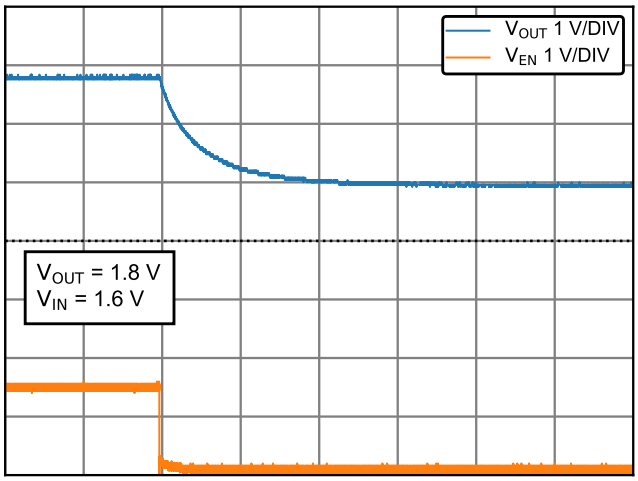
V_{OUT} and Start-Up Waveform



0.5 ms/DIV

Figure 3(k)

V_{OUT} and Shutdown Waveform



0.25 ms/DIV

Figure 3(l)

Load Transient Waveform

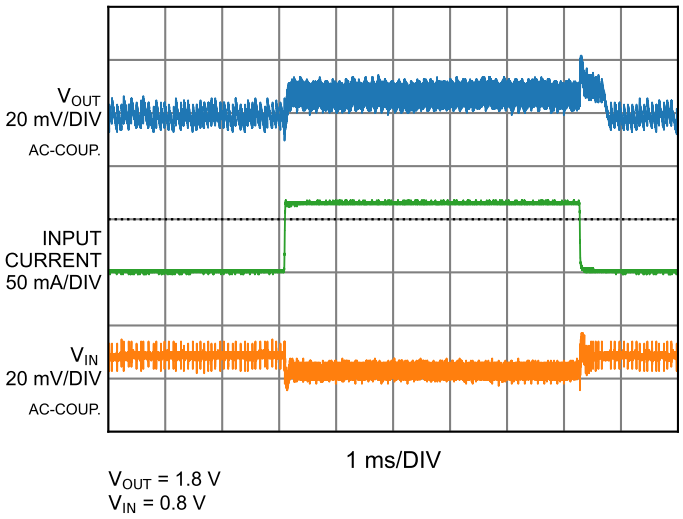


Figure 3(m)

Load Transient Waveform

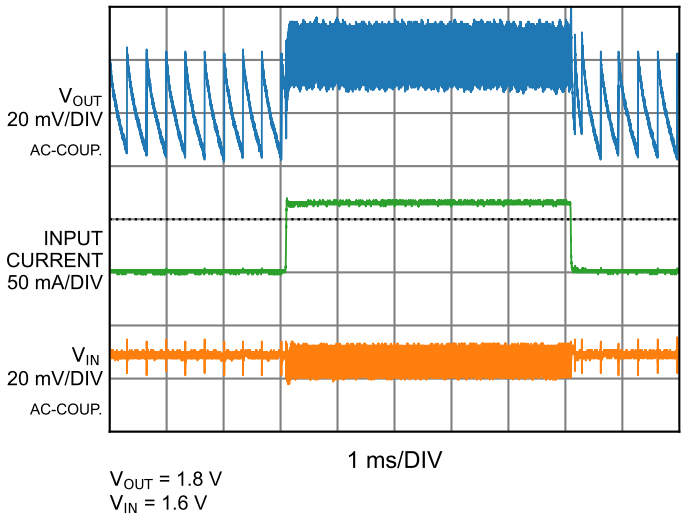


Figure 3(n)

No load I_{IN} vs V_{IN}

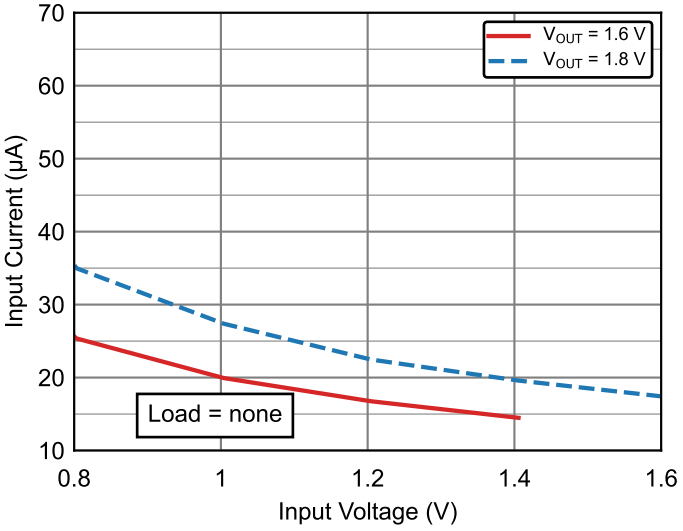


Figure 3(o)

Minimum V_{IN} at high load

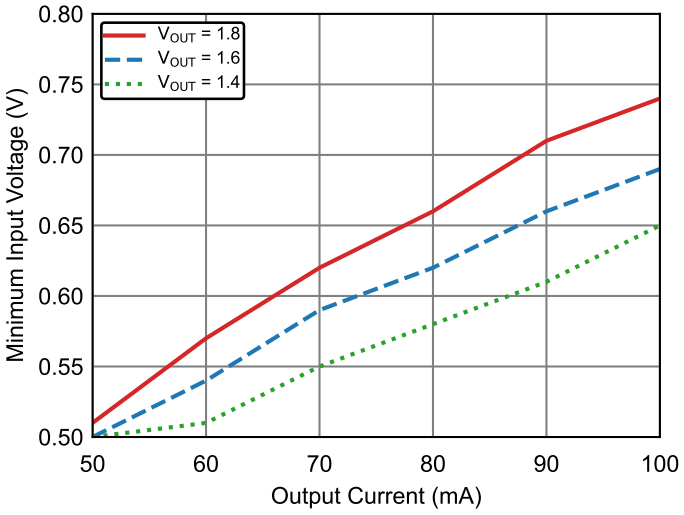


Figure 3(p)

6 Detailed Operation Description

6.1 Modes of Operation

The LMU20P1 can operate in two different modes depending on load conditions to optimize efficiency and performance at all times. These modes are described below.

6.1.1 Normal Operation

The LMU20P1 is designed to operate in continuous-conduction mode (CCM) using pulse-width modulation (PWM) with a constant switching frequency of 5 MHz. A current-mode controller regulates the configured output voltage based on the measured low-side FET current.

6.1.2 Light Load Operation

For loads below a specified threshold, the LMU20P1 enters light-load operation mode. The device operates using pulsed frequency modulation (PFM), delivering a pulse of energy to the output capacitor upon detecting an error in the feedback voltage. As long as no error is detected, the switching node maintains a high-impedance state. In PFM, the device operates with a lower switching frequency depending on the input and output voltages, output capacitor size and load. This mode offers excellent light-load efficiency, due to a substantial reduction in switching losses and quiescent current. The table below provides an example of how the switching frequency changes under different load conditions.

Table 3: Switching frequency at different load conditions for $C_{IN} = C_{OUT}$ = 10 µF

V_{OUT}	V_{IN}	Load = 0 mA	Load = 15 mA	Load = 100 mA
1.8 V	0.8 V	740 Hz	400 kHz	5 MHz
1.8 V	1.6 V	145 Hz	100 kHz	5 MHz

6.2 Shutdown

The LMU20P1 enters shutdown mode by pulling the enable pin low or by triggering one of the protection circuits. In shutdown, the quiescent current is reduced and a minimum number of internal circuits are active. The device will return to normal operation after soft start.

6.3 Soft Start Circuit

The LMU20P1 includes an internal soft-start circuit that slowly ramps the output voltage from 0 V to its set point. The soft start lasts approximately 2 ms and ramps the output voltage in steps of 20 mV in a stair-case pattern with a step-period of approximately 100 µs in a staircase pattern. During soft-start the converter operates in asynchronous PWM mode with a temporary higher peak-current limit of 600 mA. This enables the converter to start during max load conditions, given a purely resistive load, and eliminates negative inductor currents. The soft-start circuit resets with each shutdown and protection event.

6.4 Over-Temperature Protection

The LMU20P1 enters thermal protection mode if the temperature of the internal die in the integrated circuit exceeds 150 °C. During thermal protection mode the power-stage is off, and the output is high-impedance. The device will resume operation and initialize soft start, once the temperature of the integrated circuit die falls below 135 °C.

6.5 Short-Circuit Protection

To reduce the chances of permanent damage to the module, the LMU20P1 incorporates a short-circuit protection function. The short-circuit protection works by monitoring the feedback voltage, during both soft-start and normal operation, and triggers when the feedback voltage drops below 50 % of VREF. In case of a short-circuit event, the on-chip peak-current limiter will limit the peak current to approximately 500 mA. Once the short-circuit protection circuit triggers, the LMU20P1 will enter protection mode,

keeping the module off for 10 ms before attempting a restart. If the short-circuit event persists, the module will continuously attempt to restart until it can recover.

6.6 Output Current Limit

During PWM mode, the LMU20P1 has a cycle-by-cycle inductor current limit of aproximately 500 mA. This limits the total amount of power delivered to the output. If the operating conditions causes the converter to reach the cycle-by-cycle current limit, the converter will be unable to maintain the given output voltage and the output voltage will decrease until the short-circuit protection is triggered.

6.7 Low Voltage Startup

The LMU20P1 features a dedicated start-up circuit that enables start-up from an input voltage as low as 0.8 V. The feature is supported with soft-start and inrush-current limit operation. Once the output voltage reaches 95 % of the target value, the internal circuitry is powered from the output and becomes independent of the input voltage source.

7 Application Information

7.1 LMSsubsection

Typical Application Circuit

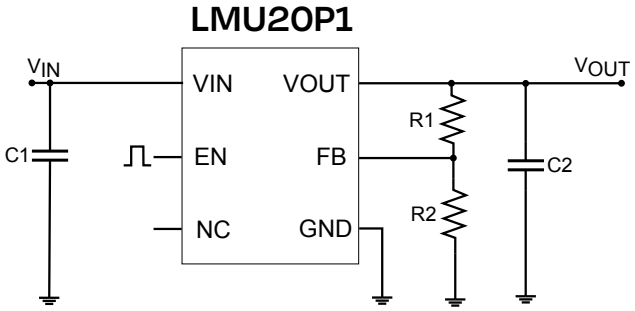


Figure 4: Typical circuit implementation of the LMU20P1

7.2 Input Capacitor Selection (C1)

A low ESL/ESR capacitor must be placed as close as possible to the package between the VIN pin and the GND pin. A 1 µF, 6.3 V X5R/X7R ceramic capacitor is required as a minimum input capacitor, though a 10 µF capacitor is recommended due to capacitance derating. If there is a long connection between the DC source and the part, an additional bulk capacitor should be inserted between the DC source and input capacitor to provide a stable DC voltage.

7.3 Output Capacitor Selection (C2)

A low ESL/ESR capacitor must be placed as close as possible to the package between the VOUT pin and the GND pin. A 4.7 µF 6.3 V X5R/X7R ceramic capacitor is required as a minimum output capacitor, though a 10 µF capacitor is recommended due to capacitance derating. The output ripple is a function of the output capacitance and the parasitic ESL and ESR. Lower ESR and ESL (e.g. high-quality capacitors) and higher capacitance will reduce the ripple and improve the transient response. The loop compensation has no minimum requirement for ESR or ESL.

7.4 Feedback Resistor Selection

The output voltage of LMU20P1 is configured through resistors R1 and R2. The relationship between the resistor divider and the output voltage is given by:

$$\frac{R_1}{R_2} = \frac{V_{OUT}}{V_{REF}} - 1 \tag{1}$$

Rearranging for V_{OUT} yields:

$$V_{OUT} = \left(1 + \frac{R_1}{R_2}\right) \cdot V_{REF} \tag{2}$$

Careful consideration of sizing the resistor divider is necessary. Large values contribute to a better light-load efficiency; however, they will impact the robustness and stability of the converter. It is recommended to select a value of 2.7 MΩ for R1 and select R2 according to equation 2. It is also recommended to keep the feedback trace as short and close to the module as possible.

7.5 Recommended Parts

Table 4: Recommended component manufacturers and series.

Capacitors		**Resistors**	
Manufacturer	**Family**	**Manufacturer**	**Family**
Samsung	CL	Yageo	RC_L
Würth Elektronik	WCAP-CSGP	Panasonic	ERJ-2RK
Murata	GRM	Vishay	CRCW-C
TDK	C	Stackpole	RMCF

8 Layout Guidelines

To achieve optimal performance with the LMU20P1, the board layout requires careful attention. Figure 5 shows the recommended printed circuit board (PCB) layout for the LMU20P1.

The input and output capacitors should be placed close to VIN and VOUT, respectively, to minimize trace lengths. The ground should be unbroken and connected to the LMU20P1 exposed pad and GND pin. The unbroken ground connection yields short inductive loops and reduces EMI and ripple. To further reduce ESL, high-quality 0402 capacitors should be used.

The feedback resistor divider must be placed close to the sensing output node, connecting the middle reference point to the FB pin. Thin traces should be used to reduce the capacitive coupling to other layers. For a multilayer PCB, a large ground plane can be added to reduce the operational temperature of the LMU20P1.

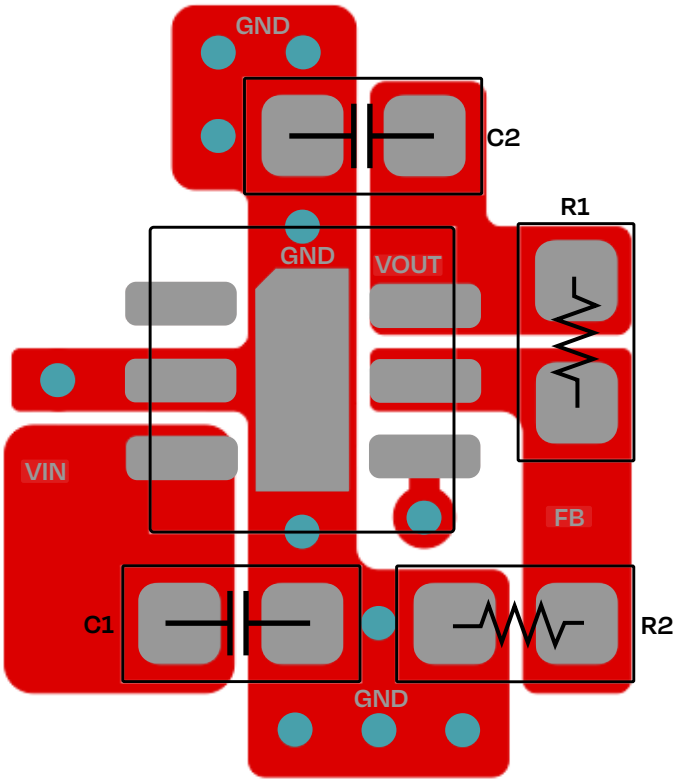


Figure 5: Recommended layout for optimal performance (top)

9 Package Information

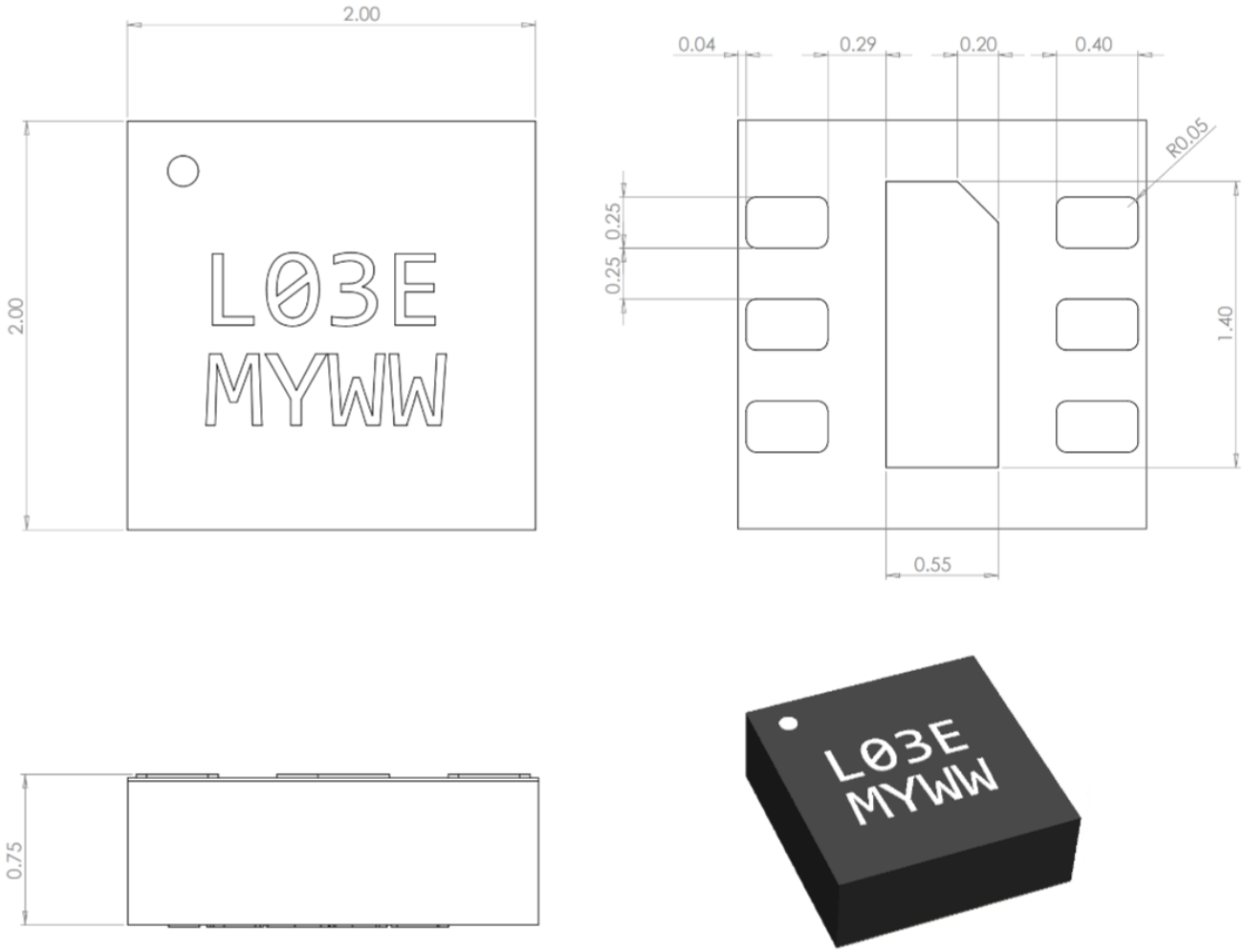


Figure 6: Package dimensions. All dimensions in mm, unless otherwise specified.

10 Tape and Reel Information

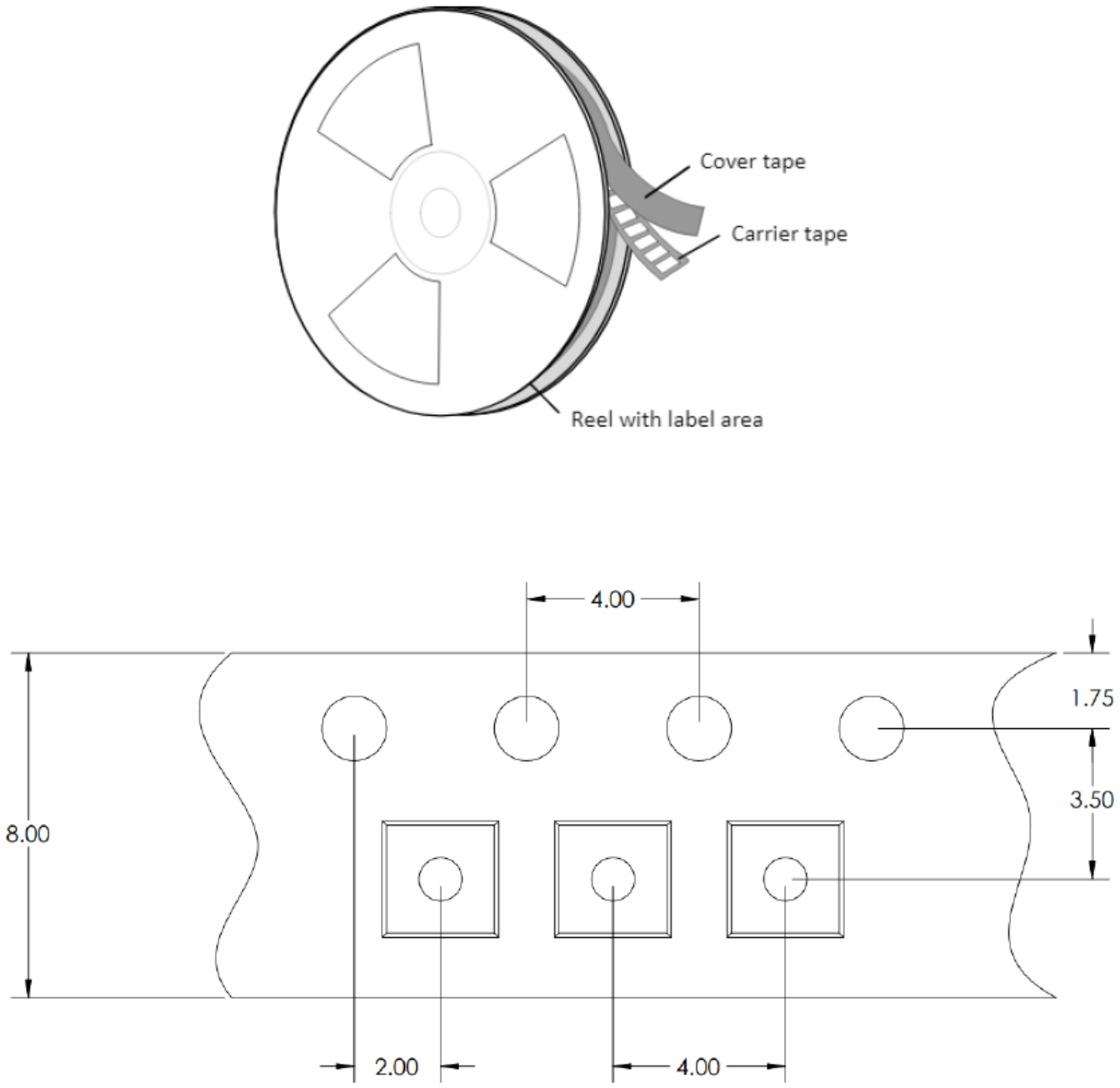


Figure 7: Tape and reel. All dimensions in mm, unless otherwise specified.

Tape Width	Component Pitch	Hole Pitch	Reel Diameter	Units per Reel
8 mm	4 mm	4 mm	180 mm (7”)	2500

11 Changelog

Revision Number	Revision Date	Description	Sections Changed
1.0	2024-05-23	Initial release	-
1.1	2025-05-28	Added information about derating for VIN < 0.8V	5
2.0	2026-08-19	Layout improvements and clarifications. Correction to equation 1	All

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