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IoT/RF Manufacturing: Fine-Pitch, Shielded, High-Density Modules at Scale

Fine-pitch, shielded, high-density IoT/RF modules fail when paste printing, placement stability, depaneling mechanics, and test coverage fight each other. INDIC tunes stencil design and Type 5 paste for 0.3 mm/01005, locks placement stability with frame support, fixes depaneling at the jig/bit level, and closes risk with Flying Probe Testing (FPT), boundary-scan JTAG, and a coverage matrix across ICT/FCT/EOL—all tied to MES traceability.

Fine-pitch IoT/RF manufacturing: stencil design + Type 5 paste for 0.3 mm and 01005

Fine-pitch boards with 0.3 mm parts, 01005 chips, dense BGAs, and shield step-ups demand controlled paste transfer. INDIC ran trials and standardized:

- Type 5 paste (vs. default Type 4) for consistent transfer on tight apertures.
- Stencil design iterations to balance release near shield step-ups and 3-mil chips.
- A dedicated support block to curb panel warpage during print.
- Aperture/rheology tweaks to cut clogging and solder balls around shield walls.

Result: stable, repeatable paste deposition in shielded zones on fine-pitch IoT/RF builds.

Shielded, high-density BGA modules: placement stability at frame level

High-density BGA layouts and shielded modules amplify micro-shifts. We stabilized placement by:

- Optimizing pick-and-place strategies per package.
- Selecting special nozzles and adding support bars to stiffen frames.
- Tightening jig tolerances to eliminate tilt and frame distortion.

Placement stability protects RF performance and holds yield on high-density assemblies.

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Depaneling high-density modules: router bits, jigs, and shield protection

Depaneling induced burrs and shield scratches until we re-engineered mechanics:

- Trialed router bits (0.8/1.5/1.6 mm) and matched diameter to module revisions.
- Built new jigs with tighter play and vibration damping.
- Added fixture support tape to control micro-movement during routing.

Mechanical fixes removed cosmetic/structural damage while protecting RF shields.

Test coverage for IoT/RF: Flying Probe Testing to 97.78% + boundary-scan JTAG & ICT/FCT/EOL

When access is scarce and specs are thin, we lift test coverage with complementary methods:

- FPT (Flying Probe Testing) for fixture-less access to components and hard-to-reach nodes.
- Boundary-scan JTAG to close BGA interconnects; pair with ICT where analog values matter.
- FCT/EOL with realistic stimuli; treat EOL as the shipping gate.
- MES traceability binds OBP version/checksum and all station results to the unit serial (no-pass/no-ship).

Case result: moving from outsourced MDA (~50% coverage) to FPT delivered 97.78% test coverage on a 4-board smart-city module, improved defect isolation, and raised product reliability.

Case evidence — fine-pitch, shielded, high-density modules in production

- Fine-pitch printing: Type 5 paste + stencil design iterations + support block removed shield-zone solder balls and under-deposit.
- Placement stability: package-level program tuning, nozzles, support bars, and jig tolerances locked BGA/shield alignment.
- Depaneling quality: revision-specific router bits + vibration damping + fixture tape eliminated burrs and shield scratches.

Together, these gated steps let the IoT customer scale complex modules with predictable yield.

What you provide; what INDIC returns

You provide: BOM/AVL, Gerbers or ODB++, stack-ups, netlists, shielding constraints, target RF tests, firmware image + checksum rules, acceptance criteria.
INDIC returns: stencil pack and print window, placement-stability plan (fixtures/nozzles/support), depaneling jig/bit matrix, a coverage matrix (FPT / JTAG / ICT/FCT/EOL), golden unit + guard-band limits, and the MES traceability schema with evidence pack.

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Quick checklist — IoT/RF fine-pitch, shielded, high-density modules

- Lock Type 5 paste and stencil design for fine-pitch 0.3 mm/01005.
- Verify placement stability (nozzles/support bars/jig tolerances) on shielded, high-density frames.
- Match router bits and jigs to revision; protect shields during depaneling.
- Use FPT to raise test coverage when access is scarce; add boundary-scan JTAG for BGAs.
- Publish the coverage matrix across ICT/FCT/EOL and bind results to serial in MES.

Bottom line

IoT/RF success hinges on controlling fine-pitch printing, shielded mechanics, high-density BGA placement, and end-to-end test coverage. INDIC fixes those at the process and fixture level, then proves it with FPT/JTAG + ICT/FCT/EOL and MES traceability—so complex modules scale without yield surprises.