■ Hardware

Leopard DPU

Egde Processing for Micro and Mini Satellites.
Leopard is a cutting-edge Data Processing Unit (DPU) designed for Micro and Mini Satellites in a compact PC-104 form factor, offering powerful on-board data analysis using Artificial Intelligence.

Now, instead of sending huge, unprocessed sets of data to ground stations, focus on the most important and valuable insights.
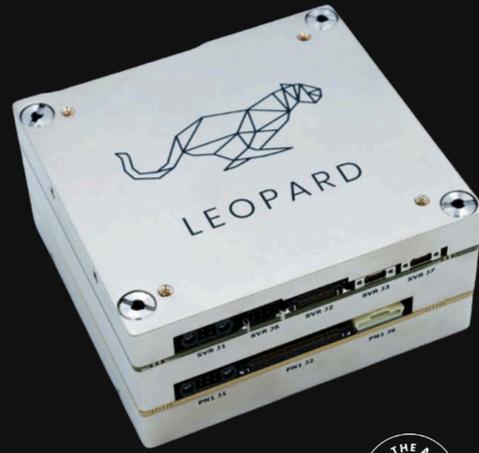
High-Performance Processing

Up to 3 Tera Operations Per Second (TOPS) for fast and efficient data processing.

AI-Driven

Utilizes deep learning algorithms directly in space, reducing the need and costs of data transfers to Earth.

Compact Design

CubeSat-compatible (<1U) with the ability to integrate seamlessly with various Micro and Mini satellite platforms.

Applications

Ideal for Earth Observation tasks such as image segmentation and object detection, as well as Space Situation Awareness (SSA) missions

■ Use Cases

LeopardISS (2024-2025)

LeopardISS is an experiment featuring KP Labs' Leopard Data Processing Unit (DPU), set to launch to the International Space Station (ISS) in early 2025 as part of the Polish Mission, in collaboration with the Poznan University of Technology (PUT). This project provides a unique platform for testing AI algorithms directly in space, allowing researchers and companies to gain valuable flight heritage for their technologies.

Intuition-1 (2023-2027)

Intuition-1 is a 6U KP Labs' hyperspectral satellite launched in November 2023, aiming to demonstrate onboard processing of hyperspectral data to minimize data transmission needs. KP Labs developed key payloads, including the 192-band hyperspectral sensor (HSI) and the Leopard Data Processing Unit (DPU). The satellite processes complex image data in orbit, enabling near-instant analysis of environmental conditions like vegetation health and soil composition.

Architecture	• Independent Supervisor (control, telemetry, software updates, FDIR)
	• 1-2 Processing node with Zynq SoC
Processing cores	AMD Zynq UltraScale+ ZU6EG | ZU9EG | ZU15EG
	• Quad ARM Cortex-A53 CPU 1.2 GHz
	• Dual ARM Cortex-R5 in lock-step
	• FPGA for custom function implementation
Memory	• 16 GiB DDR4 (with ECC)
	• 4 GiB SLC flash-based file system storage (with EDAC)
	• 2 x 240 GiB pSLC flash-based mass data storage
Interfaces	• Supervisor control I/F (TMTC): CAN bus
	• PL-connected LVDS and GPIOs
	• QuadGTH transceivers
Supply voltage and power consumption	• Supply voltage: 7 to 14 V
	• Power consumption: 7.5 W to 20 W - depending on workload and specified processing speed
Software ecosystem	• 64-bit Linux
	• Fully reconfigurable in orbit
	• Compatible with Vitis AI Deep learning accelerator
Redundancy	Possibility to introduce additional redundancy to each version
Form-factor	PC-104

■ Contact Us

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Mission Complete

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