Hardware

Leopard DPU

Edge Processing for Nano and Micro Satellites

Flight-proven Data Processing Unit supporting the full payload data handling chain on-board. **CPU + FPGA architecture** with redundant mass memory and industry-standard interfaces in a low SWaP solution. Off-the-shelf and custom Interface Boards enable **integration with various spacecraft platforms** and payload components.

Compute Power

High performance I/O and flexible CPU and FPGA

Algorithms

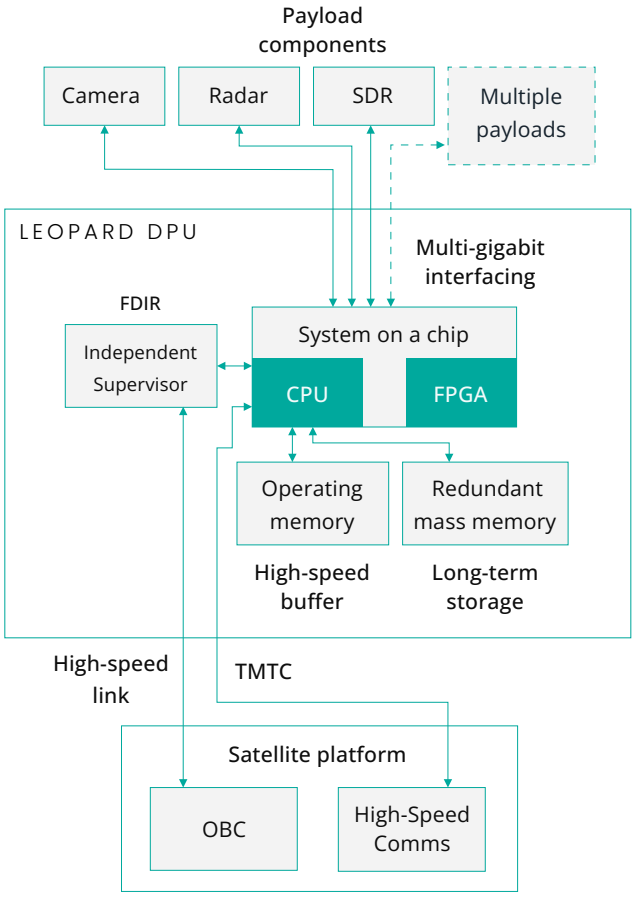
Supports classical and AI workloads directly on-board

Integration-Ready

PC/104 form factor with industry-standard interfaces

Architecture

Leopard DPU connects directly to payload components and the satellite platform - handling **acquisition, processing, and data storage in a single subsystem.**



Use cases

Supported missions

- Earth Observation
- Space Situational Awareness
- Autonomous Rendezvous & Docking
- Lunar Missions

On-board capabilities

- Payload acquisition & control
- Image pre-processing & AI inference
- Hardware-accelerated compression
- Mass memory storage

Processing algorithms & software

A library of **pre-integrated software, programmable logic components and algorithms** is available for payload interfacing (SpaceWire, PUS-C) and on-board data processing - including **image pre-processing, cloud screening and hyperspectral compression.** All listed solutions are available on request.

Architecture	• Supervisor – telemetry and control, FDIR, software recovery • Processing Node – processing and memory
Processing cores	AMD Zynq UltraScale+ MPSoC ZU6EG | ZU9EG | ZU15EG • Quad ARM Cortex-A53 CPU 1.2 GHz • Dual ARM Cortex-R5 (lock-step) • FPGA for custom function implementation
Memory	• 16 GiB PS-DDR4 (with ECC) • 64 MB Boot flash (NOR) with TMR • 4 GiB SLC NAND flash memory (with EDAC) • 2 x 240 GiB pSLC flash-based mass data storage (redundant)
Interfaces	• Supervisor TMTC interface: CAN with CSP, UART/RS422/485 • PL-connected LVDS, GPIOs and QuadGTH transceivers
Interface Extensions	• 3 x Gigabit Ethernet 1000BASE-T • 2 x SpaceWire • 2 x CAN bus • 2 x RS422/RS485/UART • 2 x PPS input • CameraLink Base/LVDS Other interfaces available upon request
Software Ecosystem	• SDK and Reference Designs for software and FPGA development • Compatible with Vitis AI Deep Learning Accelerator • 64-bit Linux (Yocto based) • Fully reconfigurable in-orbit
Environmental rating	• Qualified for launch and space environment at NASA GEVS levels • TID > 20 kRad (with enclosure) • Operating temperature: -25 °C to 75 °C
SWaP	• PC/104 form-factor with efficient thermal interface • Dimensions: 95.89 x 90.17 x 47.2 mm • Mass: 725 g • Supply voltage: 7 to 14 V • Power consumption: 5 W to 20 W – depending on workload

Test before flight

Smart Mission Lab is a platform that provides **remote access to Data Processing Units.** It enables testing before purchase and early verification of compatibility with mission requirements, algorithms, and planned workloads. This supports **hardware evaluation before integration.** Scan the QR code and test our solutions remotely.

sml.kplabs.space