

## Hardware

# Leopard DPU

## Edge Processing for Nano and Micro Satellites

**Flight-proven** Data Processing Unit supporting the full payload data handling chain on-board. **CPU + FPGA architecture** with redundant mass memory and industry-standard interfaces in a low SWaP solution. Off-the-shelf and custom Interface Boards enable **integration with various spacecraft platforms** and payload components.



### Compute Power

High performance I/O and flexible CPU and FPGA



### Algorithms

Supports classical and AI workloads directly on-board



### Integration-Ready

PC/104 form factor with industry-standard interfaces

## Architecture

Leopard DPU connects directly to payload components and the satellite platform - handling **acquisition, processing, and data storage** in a single subsystem.

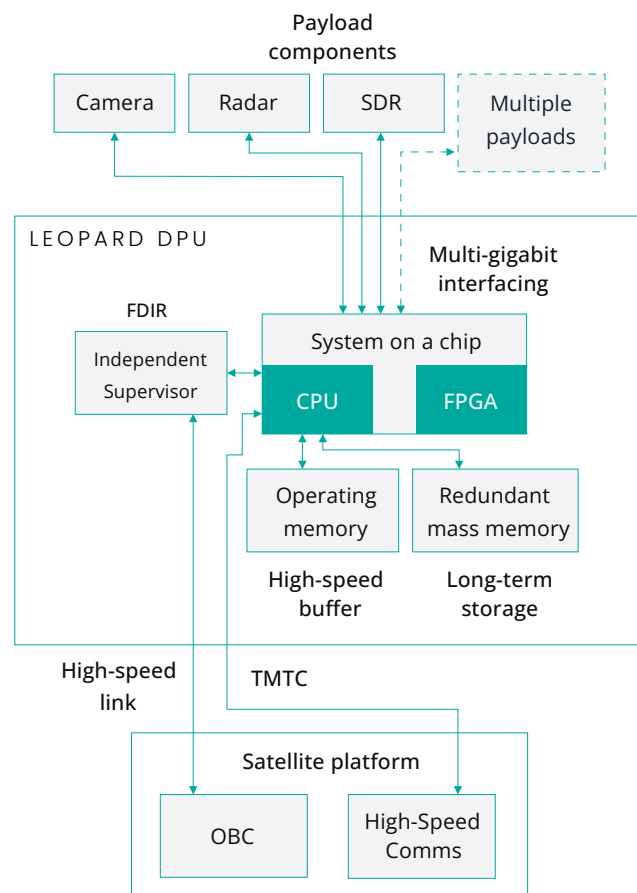
## Use cases

### Supported missions

- Earth Observation
- Space Situational Awareness
- Autonomous Rendezvous & Docking
- Lunar Missions

### On-board capabilities

- Payload acquisition & control
- Image pre-processing & AI inference
- Hardware-accelerated compression
- Mass memory storage



## Processing algorithms & software

A library of **pre-integrated software, programmable logic components and algorithms** is available for payload interfacing (SpaceWire, PUS-C) and on-board data processing - including **image pre-processing, cloud screening and hyperspectral compression**. All listed solutions are available on request.

## ■ Technical Sheet

Architecture	<ul style="list-style-type: none"><li>• Supervisor – telemetry and control, FDIR, software recovery</li><li>• Processing Node – processing and memory</li></ul>
Processing cores	<p>AMD Zynq UltraScale+ MPSoC ZU6EG   ZU9EG   ZU15EG</p> <ul style="list-style-type: none"><li>• Quad ARM Cortex-A53 CPU 1.2 GHz</li><li>• Dual ARM Cortex-R5 (lock-step)</li><li>• FPGA for custom function implementation</li></ul>
Memory	<ul style="list-style-type: none"><li>• 16 GiB PS-DDR4 (with ECC)</li><li>• 64 MB Boot flash (NOR) with TMR</li><li>• 4 GiB SLC NAND flash memory (with EDAC)</li><li>• 2 x 320 GB pSLC flash-based mass data storage (redundant)</li></ul>
Interfaces	<ul style="list-style-type: none"><li>• Supervisor TMTC interface: CAN with CSP, UART/RS422/485</li><li>• PL-connected LVDS, GPIOs and QuadGTH transceivers</li></ul>
Interface Extensions	<ul style="list-style-type: none"><li>• 3 x Gigabit Ethernet 1000BASE-T</li><li>• 2 x SpaceWire</li><li>• 2 x CAN bus</li><li>• 2 x RS422/RS485/UART</li><li>• 2 x PPS input</li><li>• CameraLink Base/LVDS</li></ul> <p>Other interfaces available upon request</p>
Software Ecosystem	<ul style="list-style-type: none"><li>• SDK and Reference Designs for software and FPGA development</li><li>• Compatible with Vitis AI Deep Learning Accelerator</li><li>• 64-bit Linux (Yocto based)</li><li>• Fully reconfigurable in-orbit</li></ul>
Environmental rating	<ul style="list-style-type: none"><li>• Qualified for launch and space environment at NASA GEVS levels</li><li>• TID &gt; 20 kRad (with enclosure)</li><li>• Operating temperature: -25 °C to 75 °C</li></ul>
SWaP	<ul style="list-style-type: none"><li>• PC/104 form-factor with efficient thermal interface</li><li>• Dimensions: 95.89 x 90.17 x 47.2 mm</li><li>• Mass: 725 g</li><li>• Supply voltage: 7 to 14 V</li><li>• Power consumption: 5 W to 20 W – depending on workload</li></ul>

## ■ Test before flight

Smart Mission Lab is a platform that provides **remote access to Data Processing Units**. It enables testing before purchase and early verification of compatibility with mission requirements, algorithms, and planned workloads. This supports **hardware evaluation before integration**. Scan the QR code and test our solutions remotely.



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