



SIM chip 380K

K2 TSS380A1

Product summary

Version 2.1

www.trasna.io

Upgrade your IoT future with Trasna

Trasna supports over 250 leading brands across 80+ countries with end-to-end IoT connectivity hardware and software solutions for SIM, eSIM, iSIM/SoC, cellular IoT modules, and device management.

Formed through the integration of several established specialist IoT players, Trasna delivers the full cellular IoT value chain from chip to cloud. This foundation gives us unmatched control, efficiency, and innovation across the stack. By partnering with us, clients gain maximum value and a strong competitive edge.



Chip design



(e)SIM



Device mgmt



Cellular IoT modules



Complete control

Enjoy end-to-end security. Everything starts and finishes with us, so you always have complete visibility and accountability at every stage



Complete efficiency

Our end-to-end solutions are designed to deliver optimal efficiency at every stage, reducing costs, time, and resources whilst ensuring fast, easy implementation



Complete innovation

We deliver cutting-edge, scalable technology, future-proofing your business with solutions that drive rapid growth and capitalise on emerging opportunities

Trasna in numbers



Top

05

in SIM

Excl. China



20_{bn}

**secure
connections**

without breach



250⁺

clients

in 80 countries



25⁺

years'

in cellular IoT





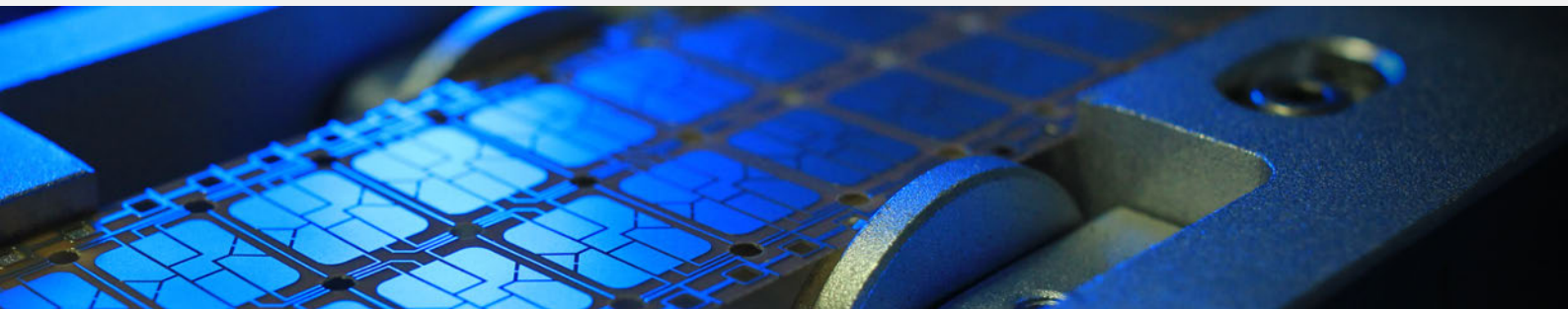
Secure SIM chip 380K: K2

Trasna introduces the **K2 TSS380A1**, a secure **SIM chip** engineered to meet the requirements of next-generation mobile communications. Designed for **4G and cost-optimized 5G deployments**, K2 addresses the needs of operators and IoT ecosystems seeking performance, security, and scalability without unnecessary complexity.

Built on a powerful **32-bit RISC architecture**, K2 leverages advanced **65 nm process technology**, **380 KB of optimized Flash memory**, and a **low-power design** to deliver high levels of security, reliable performance, and energy efficiency.

Highlights

- ✓ Optimised die size embedding 380 Kbytes flash
- ✓ Advanced embedded 65nm technology



Benefits

- **Cost-effective deployment:** Provides a highly cost-effective solution for mobile networks, making it well suited to future-proof cost-sensitive SIM card and IoT deployments while maintaining robust security and long-term reliability
- **Independent and competitive:** Delivers high-quality products, providing flexibility and competitive pricing for all players in the SIM ecosystem
- **Advanced technology:** Leveraging cutting-edge hardware architecture, ultra-low power embedded systems, and secure silicon sourcing, Trasna offers a future-proof solution
- **Scalable performance:** Optimised die size embedding with a flash density of 380 KB covering all applications, including Native, USIM Java Card, and LTE markets



Use cases

Trasna's secure SIM card chips cater to a wide range of applications, including:

- Mobile Network Operator (MNO) deployments
- Secure connectivity for IoT devices
- Machine-to-Machine (M2M) communication

Key features



High-performance architecture

A powerful 32-bit core with RISC instruction delivers exceptional processing capabilities with advanced embedded 65nm technology



Optimised power consumption

Advanced low-power modes ensure efficient operation and extended battery life for IoT devices



Secure flash memory

Fully flash-based design offers robust data retention for up to 10 years and a high erase/program cycle capability of 100 Kcycles



Unparalleled security

Secured memory data encryption and advanced algorithms safeguard against physical and logical attacks



Robustness

Operating temperature
-20°C to +85°C
Storage temperature
-40°C to +105°C



Development tools

A comprehensive development suite with an emulator and ETSI compliance simplifies integration and testing



Sustainability

Trasna integrates environmental considerations throughout its operations, from product design to supplier selection

Features overview

General

- 32-bit core CPU with RISC instruction
- Advanced low-power modes
- Internal clock at 28MHz
- ESD protection (Human Body Model):
 - Greater than 4KV 500V ESD CDM protection (Charged Device Model)
 - Class A, B and C operating voltages supported (5V, 3V and 1.8V)
- Supported standards:
 - ISO/IEC 7816-3
 - ETSI TS 102 221

CPU

- RISC processor
- High-performance 32-bit data
- 16/32-bit mixed instruction
- 2-stage single-issue pipeline
- Support big and little endian
- Performance: 0.6MIPS/MHz

Memories

FLASH

- | | |
|--|---------------------------|
| • Size: | 380KBytes |
| • Chip management area (not for user): | 12KBytes |
| • User Flash program/data area: | 380KBytes |
| • Page size: | 512Bytes |
| • Page erase speed: | 2ms |
| • Sector size: | 2KBytes |
| • Sector erase speed: | 2ms |
| • Word program speed (4 Bytes): | 25us |
| • Word read speed: | 30ns |
| • Sector endurance: | 100K Program/Erase cycles |
| • Data retention at 105°C/85°C: | 10/15 years |
| • Reliability for data retention and sector endurance tested according to JEDEC Standard JESD22-A117 | |

SRAM

- Size: 13KBytes

OTP

- Size: 512Bytes

Security

- MPU: memory protection unit
- RAM and FLASH data scrambling
- Data encryption
- Anti-attack mechanism against SPA and DPA
- Unique serial number per chip
- ISO7816 clock glitch filtering
- Environmental protection system: Voltage, HBM-ESD, CDM-ESD, X-Ray, Exposure, EMS
- Frequency and power supply monitor
- Shielding layer and test mode protect

Peripherals

- Smart card ISO7816 controller
- Support T=0/T=1 protocols
- Supported transmission speed F/D: 0x11 (372/1), 0x12 (372/2), 0x13 (372/4), 0x18 (372/12), 0x91 (512/1), 0x92 (512/2), 0x93 (512/4), 0x94 (512/8), 0x95 (512/16), 0x96 (512/32), 0x97 (512/64)
- Support clock stop
 - ISO7816 dedicated timer for 0x60 NULL byte
 - Conform to GSM power standard
- AES: ECB/CBC mode
- 16-bit CRC (based on ISO/IEC 13239 standard): $X^{16} + X^{12} + X^5 + 1$
- Timer
 - One TMR supports 16/32-bit counting
 - One ETU timer
- TRNG: True Random Number Generator to secure transactions

Operating and storage conditions

- Operating temperature min/max: -20°C/+85°C
- Storage temperature min/max: -40°C/+105°C
- Operating voltage min/max : 1.62V/5.5V

Development tools

- Emulator: Trasna provided FPGA hardware
- Development kit: compiler based on GNU GCC
- Embedder flash bootloader

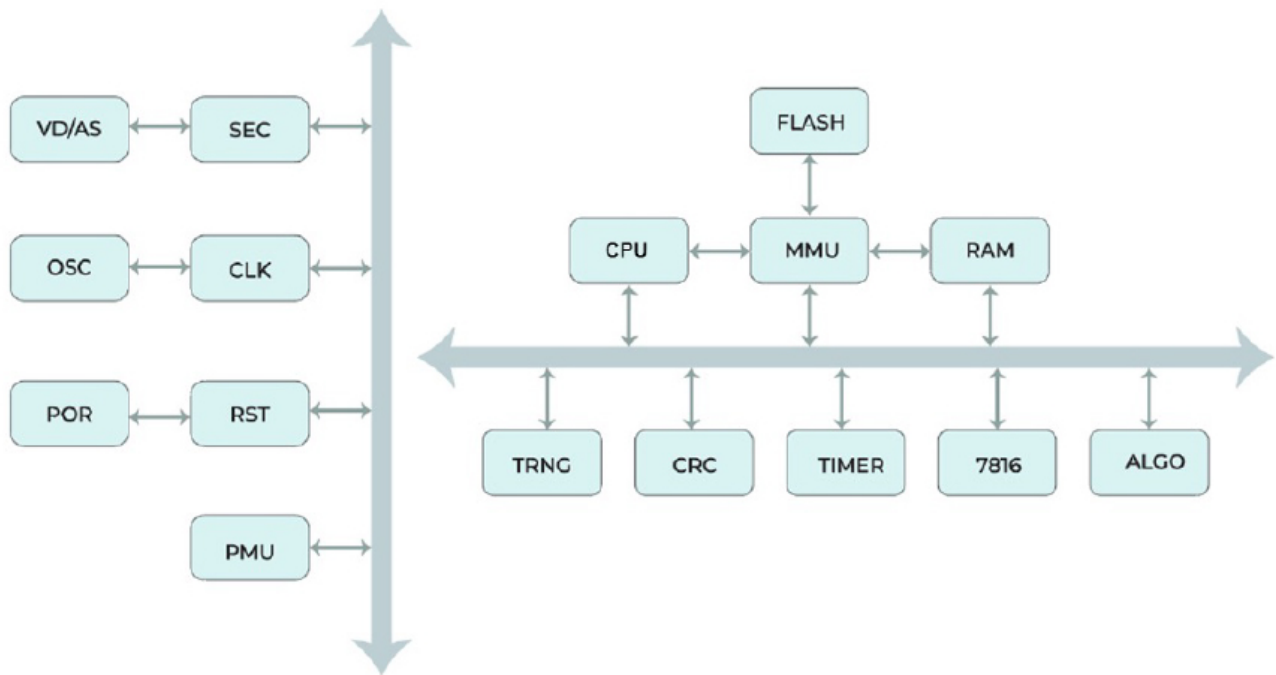
Chip PIN definition

Symbol	PIN name	Description
C1	VCC	Power supply from 1.62V to 5.5V
C2	RST	Reset input Active level effective With pull-down resistance inside
C3	CLK	Clock input Without pull-down resistance inside
C5	GND	Ground
C7	IO	Data input/output With pull-up resistance inside Default is data input when powered on

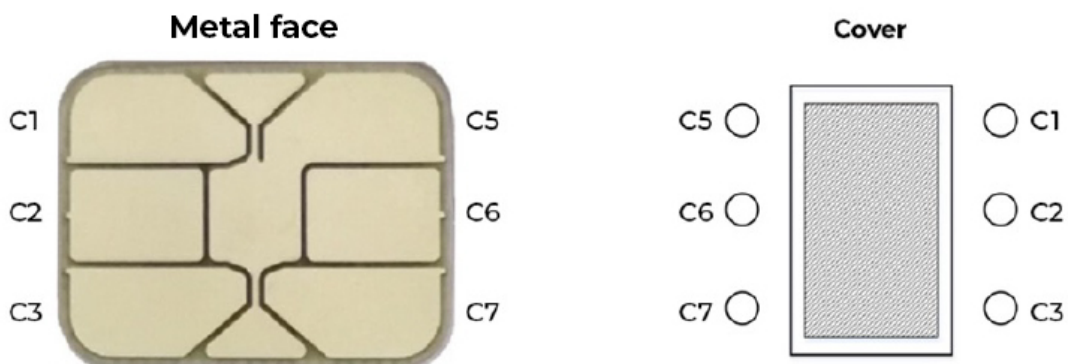
Technical parameters

Name	Symbol	VCC	Min	Typical	Max	Unit	JEDEC
Supply current	VCC	5v	-	-	10	mA	
		3v	-	-	6	mA	
		1.8V	-	-	4	mA	
Standby mode current	Isb	5v	-	-	200	uA	
		3v	-	-	100	uA	
		1.8V	-	-	100	uA	
Clock stop mode current	Isc	-	-	-	100	uA	
External frequency	Fex	-	1	-	10	MHz	
Internal frequency	Fin	-	10	-	30	MHz	
Flash endurance capacity	-	-	-	100,000	-	Cycles/sector	UA
Data retention @ 105°C	-	-	-	10	-	Years	RA
Data retention @ 85°C	-	-	-	15	-	Years	RC
Operating temperature			-20	+85		°C	TA
Storage temperature			-40	+105		°C	TS

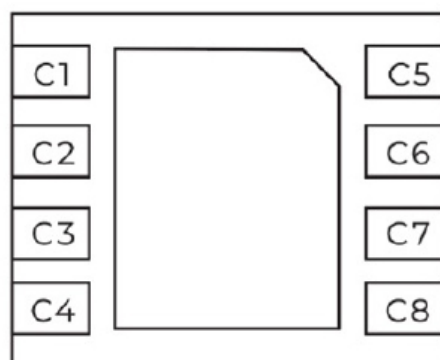
Chip block diagram



Carrier tape package information



DFN8 (5x6) package information



Learn more about Trasna's secure SIM chip 380K solution: K2 TSS380A1,
get in touch with a technical consultant today.

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