RT-HyperRAM-IPCore Reference Guide

Data Sheet for Radiation Tolerant HyperRAM AXI4-128 External Memory IP Intellectual Property Core

Rev 01252026

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DOCUMENT OVERVIEW

This document is designed to serve as a high level overview manual for CorDes Radiation Tolerant (RT) HyperRAM Memory Interface Intellectual Property [IP] Core. It includes the System Overview, the Hardware Interface Control Descriptions for external and major internal I/O, the Hardware Detail Design Descriptions [HDD] for all modules, and the Software Application Programming (API) Interface definitions.

The IP Core VHDL/Verilog, SystemC, and C++ files [source code form], detailed structural diagrams, module testbenches, and system level simulation environment are all provided with the IP core license. This also includes a full build environment for implementation (DCUltra, and Xilinx Vivado 2024.2) of the design for synthesis.

The IP Core has been successfully implemented in Ultrascale+ AMD-XILINX FPGAs and is silicon proven in GF 22FDx-SOI ASIC process.

IP CORE REFERENCE ARCHITECTURE HIGH LEVEL DESCRIPTION

SYSTEM OVERVIEW

The HyperRAM IP Core is a VHDL & Verilog implementation that provides a AXI4-128 Slave to 5x External 8-bit DDR400 HyperRAM memories. It provides inline complex interleaved Error Correction capable of correcting 4Bytes (or 4 random bits) per 64Byte Block along with 2-bit random correction per 16Byte subblock within the 64B cacheline. The design is optimized for 64B cacheline accesses consistent with most ARM and RISC-V Embedded CPU designs. Read Modify Write for non-aligned or partial cacheline access is supported and handled internally by the core.

Data Rate is dependent on implementation clock speed and the size of the data blocks fed to the core. Typical target implementation frequency is 100Mhz in mainstream Xilinx devices, and 400Mhz in <=22nm ASIC Process. At these clock rates the core is capable of up to 2GB/s operation in bursts.

Software (C/C++) Drivers are provided in the module mixed language testbench to interface with the IP core and verify operation. Minimal configuration is required before operational use of the core and is limited to setting the HyperRAM Memories to Fixed Latency operation and performing a self-initialization sequence to preset the ECC blocks in all the RAMs.

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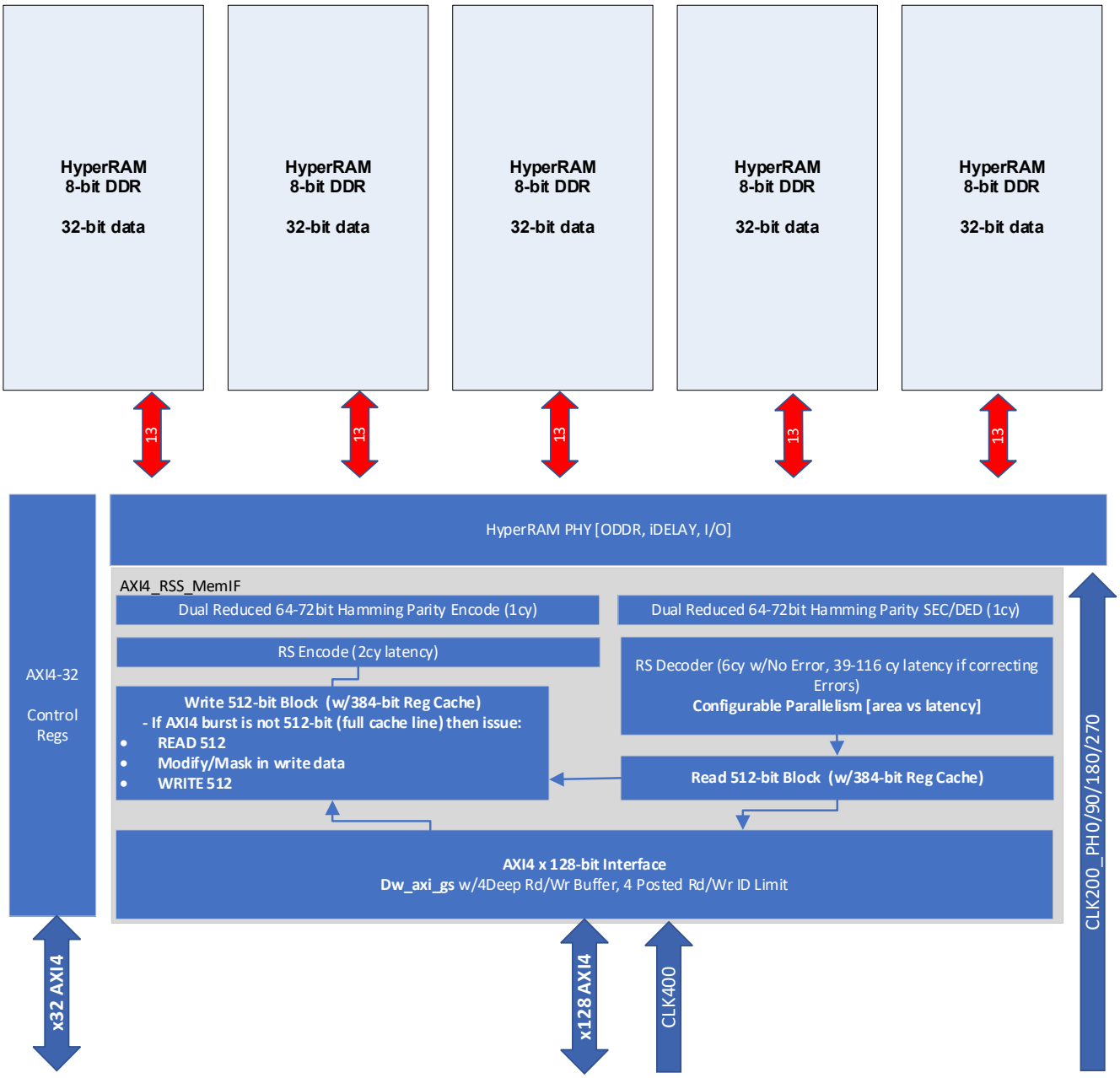
RS(72,64,8); n-k =8, 4Byte error correcting capability
Allows 4 Byte Correction per 64Byte Line. Dual 64-72b SEC-DEC allows 2-bit Random Error correction pre RS ECC per 16Byte sub-block



400Mhz @128-bit == 6.4GB/sec Interface Bandwidth. 5x DDR400 HyperRAM is limited to a theoretical max 2GB/sec bandwidth. Protocol overhead for HyperRAM random access and ECC overhead limit actual bandwidth to <2GB/sec.

~10-16cy latency on Cacheline Read/Write (with no RS Errors)
~latency penalty on RS Errors (detected with RS Syndrome check) varies based on RS Decoder Parallelism selection

Figure 1 RT-HyperRAM-Interface IP Core High Level Block Diagram

INTERNAL IP CORE ARCHITECTURE OVERVIEW

As shown in [Figure 2 Architecture Block Diagram of IP Core] the IP Core has a AXI4-32 configuration interface for setting control registers, and a AXI4-128 memory port interface to connect to a CPU or subsystem bus. The IP Core is designed to support 64B cacheline read/writes in bursts of single cachelines or up to 64x64B cachelines (4KB) depending on configured FIFO depths.

The IP Core on writes performs RS ECC and Reduced Hamming Parity encoding over each block, and supports read-modify/write operations for partial blocks. On reads the 64B Blocks with ECC are decoded and SECDED is performed over each 8Byte subblock within the cache line at no additional latency penalty (Dual SECDED per 144-bit line). If no additional errors are detected outside the SECDED capability then the block is fetched and responded to the memory bus (AXI4-128). If additional errors (up to 4Bytes, or 4-random bits with >9-bit separation) per 64B block are detected then the RS(72, 64, 8) ECC Decoder attempts to correct the errors. Uncorrectable errors signal a IRQ for use by the subsystem to allow system level handling of the event.

Internal shadow registers at the end of the memory region provide access to set the IP core to preset any or all 4KB regions in external memory, and to provide status counters for the total accumulated and last location of correctable and uncorrectable errors.

All code is synthesizable VHDL or Verilog, except the I/O, RAMs and Delay cells. The I/O, RAMs and Delay cells must be replaced with technology specific cells. Reference implementation for GF 22FDx-SOI and AMD-XILINX FPGAs are provided. All code is provided in source code (un-encrypted) format for ease of modification and integration into the users environment.

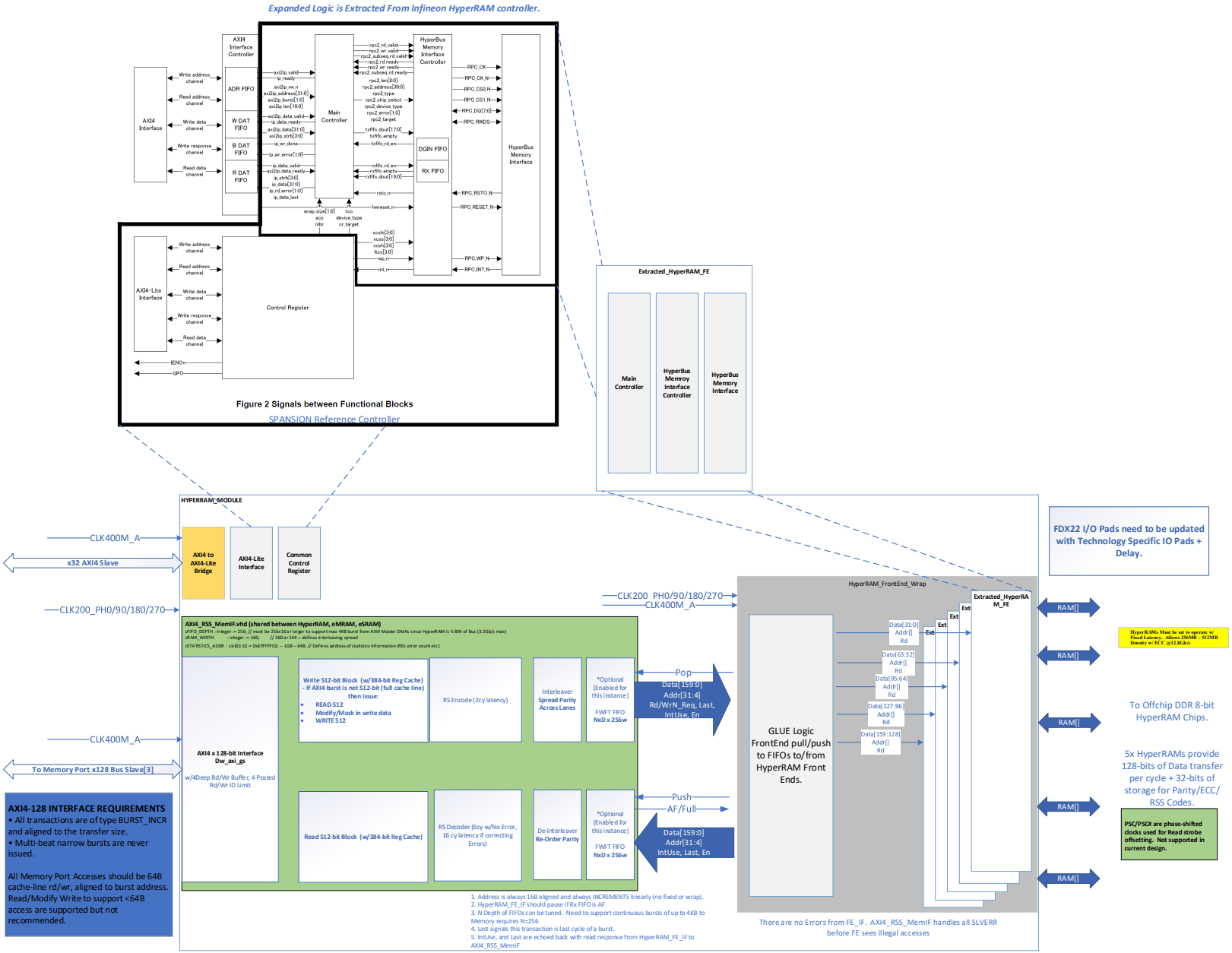


Figure 2 Architecture Block Diagram of IP Core

The AXI4_RSS_MemIF.vhd submodule performs the AXI4x128 interface and RSFEC Encode/Decode and interleaved dual SECDED to the backend. The AXI4 interface is selectable to be a Synopsys Designware AMBA Fabric component [if the user has a valid license] or a lightweight RTL version that is royalty-free but has less capability and performance.

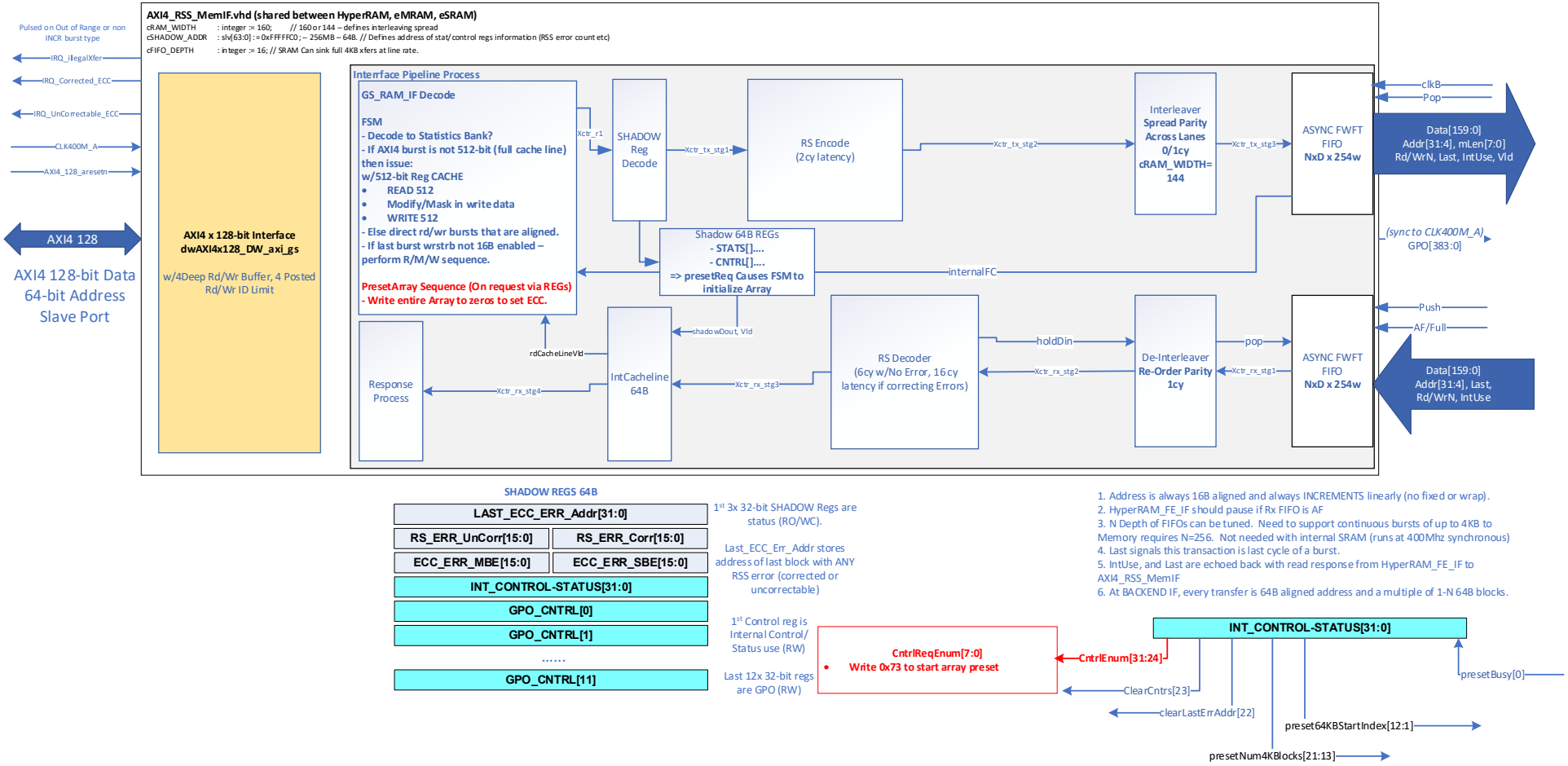


Figure 3 AXI4 RSS Memory Interface Block Diagram

As shown below the front end is designed to run at the AXI4 interface clock rate (clk400), and the front end runs at ½ that rate (clk200 phase-0). All data and configuration register transfers are handed off using asynchronous FIFOs between domains to remove any phase alignment requirements between the clk400 and clk200's.

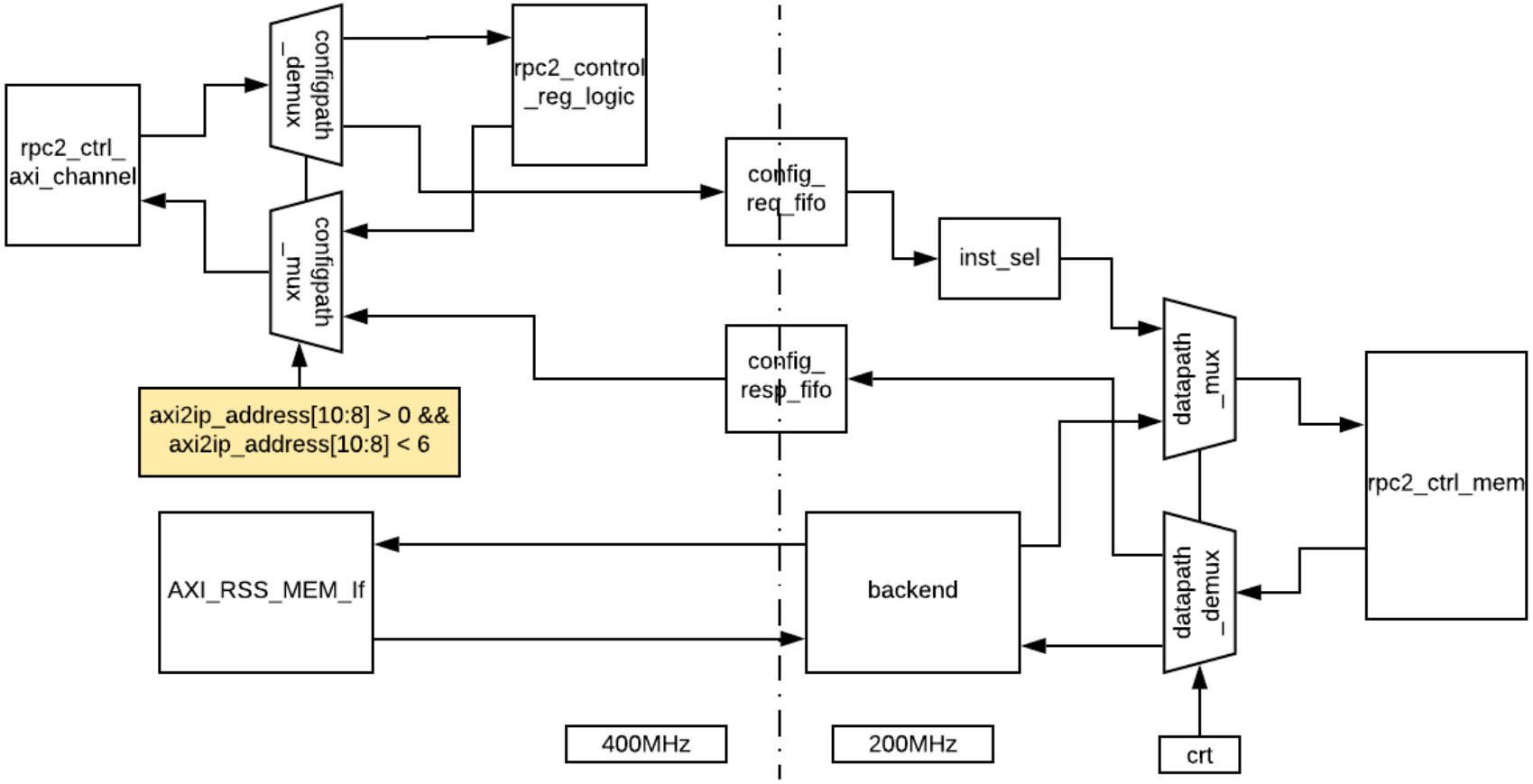


Figure 4 Front to Backend Clock Handoff

An example use of the IP Core in a Full embedded CPU Subsystem is shown below.

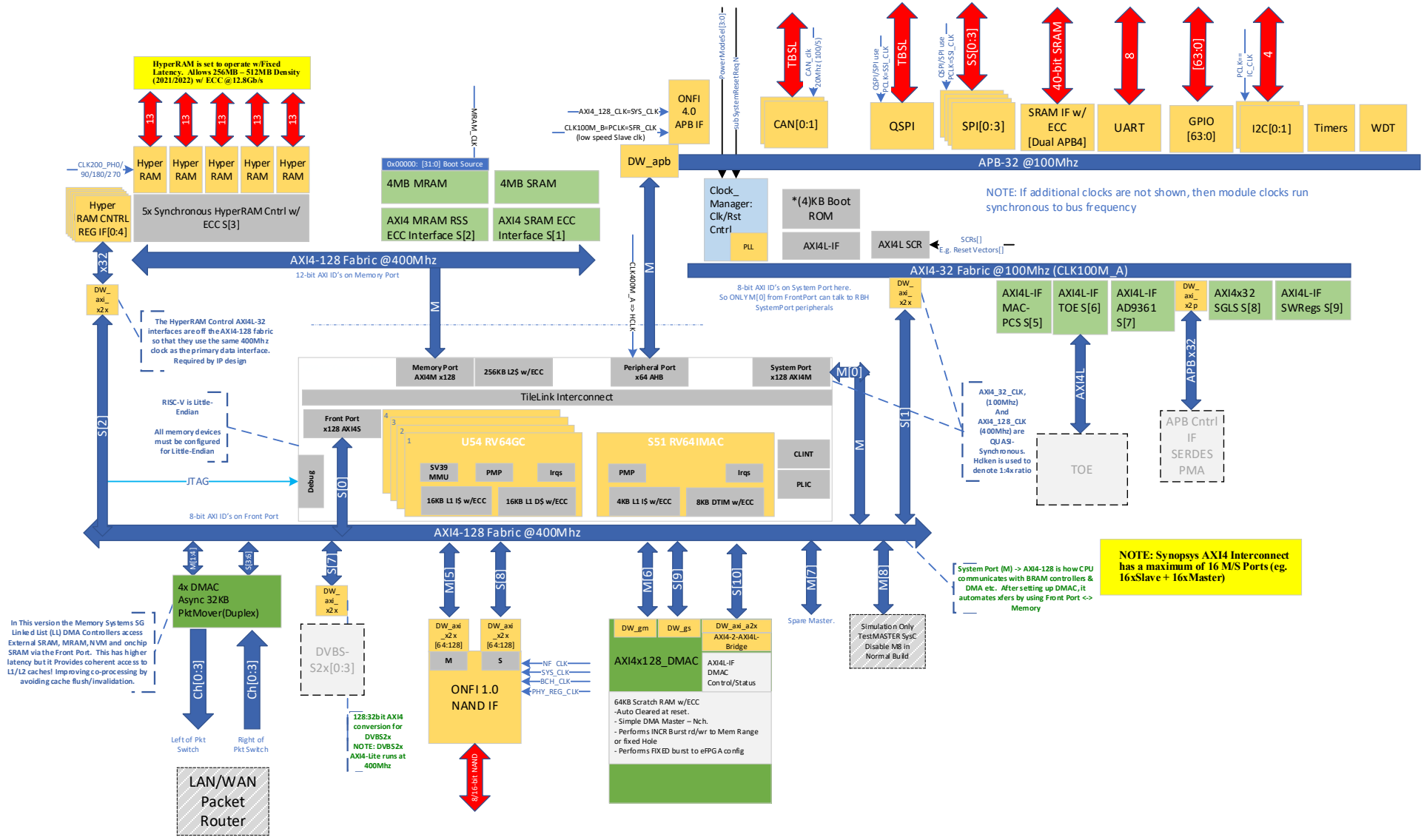


Figure 5 Example CPU Subsystem use of HyperRAM IP Core

Timing analysis of the HyperRAM I/O and board layout requirements are shown below:

For 400Mhz operation the timing analysis shows that a typical implementation budget has a Data Valid window of 1.267ns. In the HyperRAM PHY interface provided example ODDR and input IDelay modules are provided that perform alignment and programmable delay adjustment of the critical RWDS signal per the specification. The user design must provide 4x phase-aligned clocks at ½ the main AXI4-128 clock rate. E.g. for 400Mhz interface clock, the user must provide 200Mhz Phase[0, 90, 180, 270] input clocks. This can be from a PLL, DLL, or a divider output with fixed phase alignments. A reference clock manager that provides these phase aligned outputs is optionally available if needed.

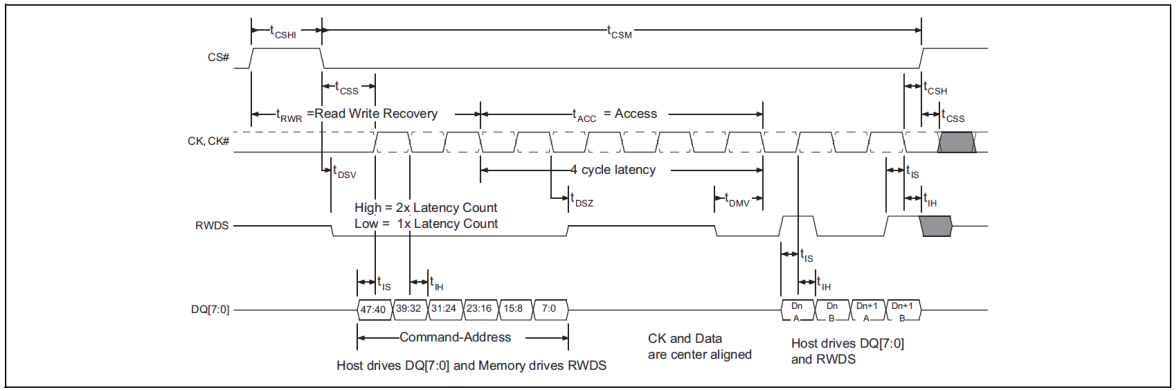


Figure 34 Write timing diagram — No additional latency

CK DDR Period = 2.35ns (Min with duty cycle distortion)

Jitter/Uncertainty on clock = 50ps
tIS = 500ps
tIH = 500ps

HyperRAM Layout guidelines recommend max skew of 33ps between DQ and CK on PWB.

Data valid window = 2.35ns – (50 + 500 + 500 + 33) == 1.267 ns

Figure 6 HyperRAM Clock period Timing for DQ/CK layout

Table 29 HYPERRAM™ specific read timing parameters

Parameter	Symbol	200 MHz		166 MHz		Unit
		Min	Max	Min	Max	
Chip select HIGH between transactions - 1.8 V	t_{CSHI}	6	–	6	–	ns
Chip select HIGH between transactions - 3.0 V		6	–	6	–	
HYPERRAM™ read-write recovery time - 1.8 V	t_{RWR}	35	–	36	–	
HYPERRAM™ read-write recovery time - 3.0 V		35	–	36	–	
Chip select setup to next CK rising edge	t_{CSS}	4.0	–	3	–	
Data strobe valid - 1.8 V	t_{DSV}	–	5.0	–	12	
Data strobe valid - 3.0 V		–	6.5	–	12	
Input setup - 1.8 V	t_{IS}	0.5	–	0.6	–	
Input setup - 3.0 V		0.5	–	0.6	–	
Input hold - 1.8 V	t_{IH}	0.5	–	0.6	–	
Input hold - 3.0 V		0.5	–	0.6	–	
HYPERRAM™ read initial access time - 1.8 V	t_{ACC}	35	–	36	–	
HYPERRAM™ read initial access time- 3.0 V		35	–	36	–	
Clock to DQs low Z	t_{DQLZ}	0	–	0	–	
CK transition to DQ valid - 1.8 V	t_{CKD}	1	5.0	1	5.5	
CK transition to DQ valid - 3.0 V		1	6.5	1	7	
CK transition to DQ invalid - 1.8 V	t_{CKDI}	0	4.2	0	4.6	
CK transition to DQ invalid - 3.0 V		0.5	5.7	0.5	5.6	
Data valid (t_{DV} min = The lesser of: t_{CKHP} min - t_{CKD} max + t_{CKDI} max) or (t_{CKHP} min - t_{CKD} min + t_{CKDI} min) - 1.8 V	t_{DV}[65, 66]	1.45	–	1.8	–	
Data valid (t_{DV} min = The lesser of: t_{CKHP} min - t_{CKD} max + t_{CKDI} max) or (t_{CKHP} min - t_{CKD} min + t_{CKDI} min) - 3.0 V		1.45	–	1.3	–	
CK transition to RWDS valid - 1.8 V	t_{CKDS}	–	5.0	1	5.5	
CK transition to RWDS valid - 3.0 V		–	6.5	1	7	
RWDS transition to DQ valid - 1.8 V	t_{DSS}	-0.4	+0.4	-0.45	+0.45	
RWDS transition to DQ valid - 3.0 V		-0.4	+0.4	-0.45	+0.45	
RWDS transition to DQ invalid - 1.8 V	t_{DSH}	-0.4	+0.4	-0.45	+0.45	
RWDS transition to DQ invalid - 3.0 V		-0.4	+0.4	-0.45	+0.45	
Chip select hold after CK falling edge	t_{CSH}	0	–	0	–	
Chip select inactive to RWDS HIGH-Z - 1.8 V	t_{DSZ}	–	5.0	–	6	
Chip select inactive to RWDS HIGH-Z - 3.0 V		–	6.5	–	7	

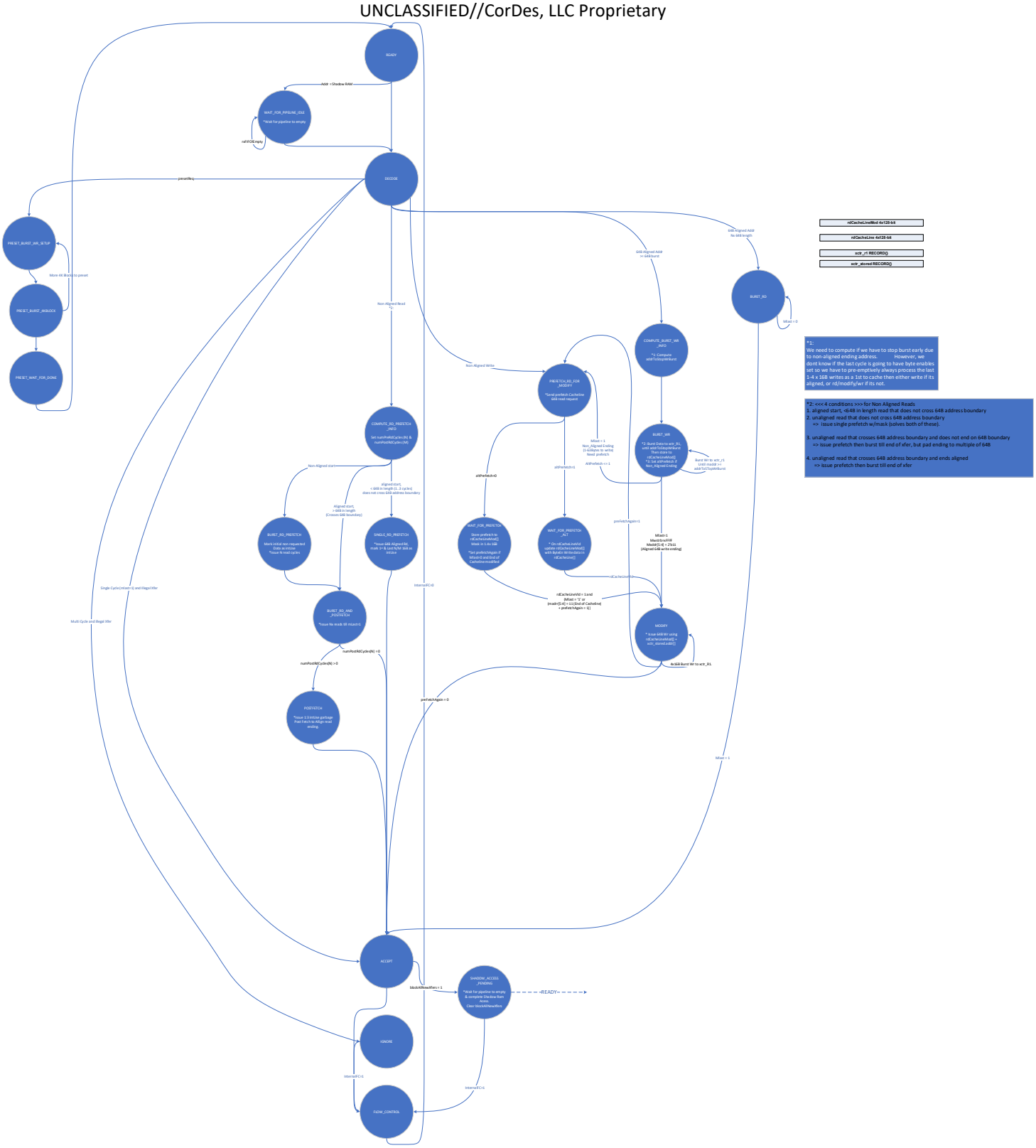
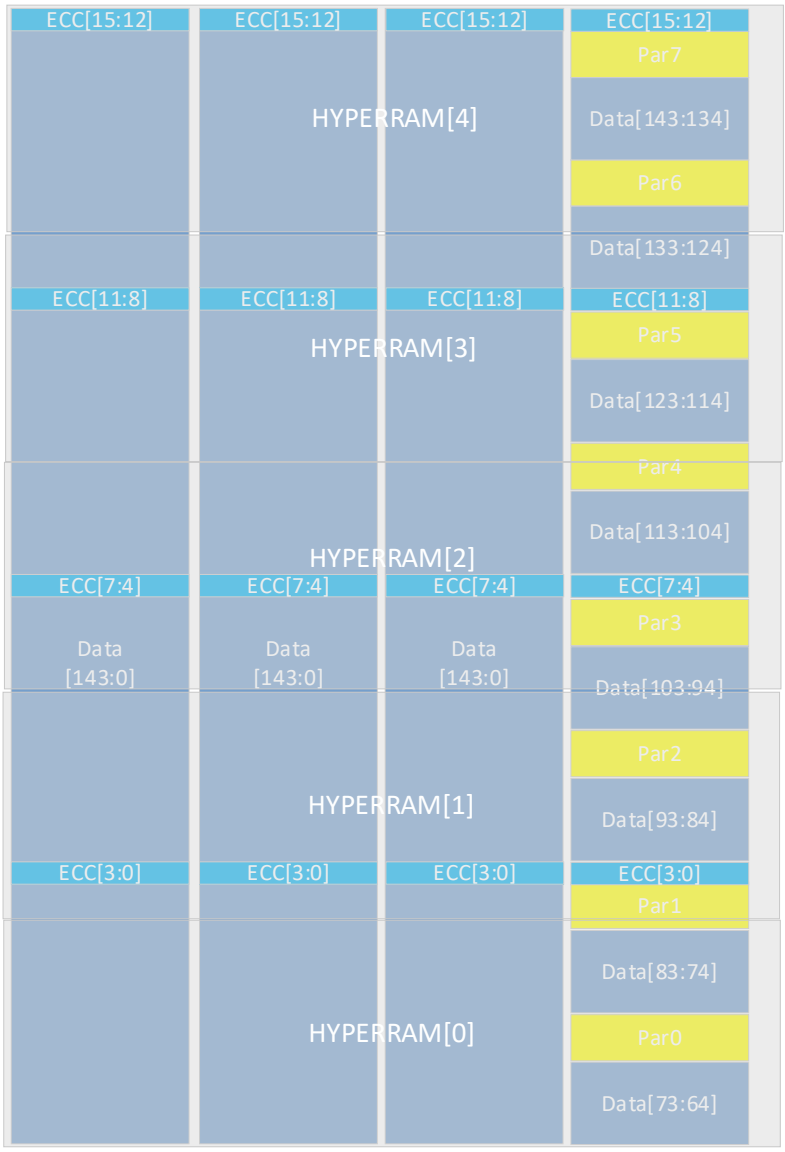


Figure 7 FSM Architecture of RSS CacheLine Access w/FEC control

For reference the Finite State Machine of the RS-FEC AXI4-128 64B cacheline Access controller is shown above.

REED SOLOMON & REDUCED HAMMING INTERLEAVING

The RS(72, 64, 8) FEC along with Dual Reduced 64-72-bit Single Event Correct, Double Event Detect (SECDED) parity is encoded and interleaved for each 64Byte Cacheline block before sending to memory in the format as shown:



NOTE: dual 64/72 (128->144) ECC adds 16-bits parity. There is not enough bits spare to cover entire 144-bits of RSS output.

Instead we selectively take 128-bits out of the RSS output and add ECC. This way on receive from RAM you have all the data + ECC needed concurrently in each cycle to perform reverse.

Figure 8 RS/ECC Interleaved Format

AXI4 32-BIT INTERFACE AND INITIALIZATION

All configuration registers in the reference design use the AXI4 32-bit Interface internally bridged to a AXI4-Lite register set. Only 32-bit reads and writes are supported – byte accesses are prohibited and will not function correctly (perform read/modify writes if required). All AXI4Lite slave interfaces are synchronous to the datapath clocks. Refer to [AMBA AXI Protocol Specification for AXI4 and AXI4-Lite] for details on the AXI4 and AXI4-Lite peripheral interface.

The External HyperRAM memories require some initial configuration before supporting pseudo-synchronous operation from the RT-HyperRAM controller. This is achieved via AXI4-32 register writes to the internal controller – a steering register selects which external Memory DIE is targeted – then the configuration write is sent to the external memory via the shared I/O. The software initialization driver uses this path to set the external memories into fixed latency operation, adjust the timing parameters (if needed), and se the Master Clock Type in CR1 to Differential.

After initializing the registers in each external Memory the driver uses the AXI4_RSS_Mem_IF controller to preset all 4KB blocks with valid computed ECC. This is done via accessing the shadow registers which are mapped to the last 64B block at the end of the 256MB region. Once preset is complete the memory is available for the system/CPU to use it for normal 64B read/write cacheline operations.

IP CORE TOP LEVEL I/O

The following parameters are configurable for the core at the top level:

Table 1 IP Core Top Level Generics

Name	Type	Description
CORR_PARALLELISM	Integer	[1,2,4,32] Selects RS Decoder internal Parallelism – lower reduces AREA but increase latency when errors are detected and require RS correction. Latency increases from nominal 6cy w/out errors to: Parallelism 1 == 116 cy latency 4 == 62 cy latency 32 [Full parallel] == 39 cy latency on correct.
cFIFO_DEPTH	Integer	Default is 256. Sets Depth of AXI4_RSS_MemIF FIFOs. Width internally is 254bits. Depth should be set to the largest outstanding burst length of xfers supported on the AXI4-128 interface.
cRAM_BASE_ADDR	64-bit SLV	Base address of transactions to decode. Must be 64B aligned.
cRAM_END_ADDR	64-bit SLV	End address of transactions to decode. Must be 64B aligned. Must include 64B address of SHADOW Regs. Should be larger than actual memory range used by external memory devices to support shadow regs.
cSHADOW_ADDR	64-bit SLV	Base address of memory to map to internal shadow registers. Must be 64B Aligned.

Table 2 IP Core Top Level I/O w/Example I/O from 22FDX Design

GROUP	PinName	IO Macro Name	IO Type	IO DIR	IO VDD (V)	Frequency	Driving current capacity	Output Load	Impedance	Tolerance (+/-%)	Inductance nH	Max Skew Limit	CrossTalk Limit
HYPERRAM 2.0 200Mhz DDRw/ECC Expansion Memory Interface	HYPER_CSN[0]	DWC_GPIO18_INLINE_OUT_H	LVCMOS	O	1.8	200Mhz	4ma	3pf	500hm	20%			
	HYPER_CK[0]	DWC_GPIO18_INLINE_OUT_H	LVCMOS	O	1.8	200Mhz	4ma	3pf	100Ohm Diff Pair	10%			-26db
	HYPER_CKN[0]												-26db
	HYPER_PSC[0]	DWC_GPIO18_INLINE_OUT_H	LVCMOS	O	1.8	200Mhz	4ma	3pf	100Ohm Diff Pair	10%			
	HYPER_PSCN[0]												
	HYPER_RWDS[0]	DWC_GPIO18_INLINE_BDFS_H	LVCMOS	IO	1.8	200Mhz	4ma	3pf	500hm	20%			
	HYPER_RSTN[0]	DWC_GPIO18_INLINE_OUT_H	LVCMOS	O	1.8	200Mhz	4ma	3pf	500hm	20%			
	HYPER_DQ[0]	DWC_GPIO18_INLINE_BDFS_H	LVCMOS	IO	1.8	200Mhz	4ma	3pf	500hm	20%		120 ps	
	HYPER_DQ[1]	DWC_GPIO18_INLINE_BDFS_H	LVCMOS	IO	1.8	200Mhz	4ma	3pf	500hm	20%			
	HYPER_DQ[2]	DWC_GPIO18_INLINE_BDFS_H	LVCMOS	IO	1.8	200Mhz	4ma	3pf	500hm	20%			
	HYPER_DQ[3]	DWC_GPIO18_INLINE_BDFS_H	LVCMOS	IO	1.8	200Mhz	4ma	3pf	500hm	20%			
	HYPER_DQ[4]	DWC_GPIO18_INLINE_BDFS_H	LVCMOS	IO	1.8	200Mhz	4ma	3pf	500hm	20%			
	HYPER_DQ[5]	DWC_GPIO18_INLINE_BDFS_H	LVCMOS	IO	1.8	200Mhz	4ma	3pf	500hm	20%			
	HYPER_DQ[6]	DWC_GPIO18_INLINE_BDFS_H	LVCMOS	IO	1.8	200Mhz	4ma	3pf	500hm	20%			
	HYPER_DQ[7]	DWC_GPIO18_INLINE_BDFS_H	LVCMOS	IO	1.8	200Mhz	4ma	3pf	500hm	20%			
	HYPER_CSN[1]	DWC_GPIO18_INLINE_OUT_H	LVCMOS	O	1.8	200Mhz	4ma	3pf	500hm	20%			
	HYPER_CK[1]	DWC_GPIO18_INLINE_OUT_H	LVCMOS	O	1.8	200Mhz	4ma	3pf	100Ohm Diff Pair	10%			-26db
	HYPER_CKN[1]												-26db
	HYPER_PSC[1]	DWC_GPIO18_INLINE_OUT_H	LVCMOS	O	1.8	200Mhz	4ma	3pf	100Ohm Diff Pair	10%			
	HYPER_PSCN[1]												
	HYPER_RWDS[1]	DWC_GPIO18_INLINE_BDFS_H	LVCMOS	IO	1.8	200Mhz	4ma	3pf	500hm	20%			
	HYPER_RSTN[1]	DWC_GPIO18_INLINE_OUT_H	LVCMOS	O	1.8	200Mhz	4ma	3pf	500hm	20%			
	HYPER_DQ[8]	DWC_GPIO18_INLINE_BDFS_H	LVCMOS	IO	1.8	200Mhz	4ma	3pf	500hm	20%		120 ps	
	HYPER_DQ[9]	DWC_GPIO18_INLINE_BDFS_H	LVCMOS	IO	1.8	200Mhz	4ma	3pf	500hm	20%			
	HYPER_DQ[10]	DWC_GPIO18_INLINE_BDFS_H	LVCMOS	IO	1.8	200Mhz	4ma	3pf	500hm	20%			
	HYPER_DQ[11]	DWC_GPIO18_INLINE_BDFS_H	LVCMOS	IO	1.8	200Mhz	4ma	3pf	500hm	20%			
	HYPER_DQ[12]	DWC_GPIO18_INLINE_BDFS_H	LVCMOS	IO	1.8	200Mhz	4ma	3pf	500hm	20%			
	HYPER_DQ[13]	DWC_GPIO18_INLINE_BDFS_H	LVCMOS	IO	1.8	200Mhz	4ma	3pf	500hm	20%			
	HYPER_DQ[14]	DWC_GPIO18_INLINE_BDFS_H	LVCMOS	IO	1.8	200Mhz	4ma	3pf	500hm	20%			
	HYPER_DQ[15]	DWC_GPIO18_INLINE_BDFS_H	LVCMOS	IO	1.8	200Mhz	4ma	3pf	500hm	20%			
	HYPER_CSN[2]	DWC_GPIO18_INLINE_OUT_H	LVCMOS	O	1.8	200Mhz	4ma	3pf	500hm	20%			
	HYPER_CK[2]	DWC_GPIO18_INLINE_OUT_H	LVCMOS	O	1.8	200Mhz	4ma	3pf	100Ohm Diff Pair	10%			-26db
	HYPER_CKN[2]												-26db
	HYPER_PSC[2]	DWC_GPIO18_INLINE_OUT_H	LVCMOS	O	1.8	200Mhz	4ma	3pf	100Ohm Diff Pair	10%			
	HYPER_PSCN[2]												
	HYPER_RWDS[2]	DWC_GPIO18_INLINE_BDFS_H	LVCMOS	IO	1.8	200Mhz	4ma	3pf	500hm	20%			
	HYPER_RSTN[2]	DWC_GPIO18_INLINE_OUT_H	LVCMOS	O	1.8	200Mhz	4ma	3pf	500hm	20%			
	HYPER_DQ[16]	DWC_GPIO18_INLINE_BDFS_H	LVCMOS	IO	1.8	200Mhz	4ma	3pf	500hm	20%		120 ps	
	HYPER_DQ[17]	DWC_GPIO18_INLINE_BDFS_H	LVCMOS	IO	1.8	200Mhz	4ma	3pf	500hm	20%			
	HYPER_DQ[18]	DWC_GPIO18_INLINE_BDFS_H	LVCMOS	IO	1.8	200Mhz	4ma	3pf	500hm	20%			
	HYPER_DQ[19]	DWC_GPIO18_INLINE_BDFS_H	LVCMOS	IO	1.8	200Mhz	4ma	3pf	500hm	20%			
	HYPER_DQ[20]	DWC_GPIO18_INLINE_BDFS_H	LVCMOS	IO	1.8	200Mhz	4ma	3pf	500hm	20%			
	HYPER_DQ[21]	DWC_GPIO18_INLINE_BDFS_H	LVCMOS	IO	1.8	200Mhz	4ma	3pf	500hm	20%			
	HYPER_DQ[22]	DWC_GPIO18_INLINE_BDFS_H	LVCMOS	IO	1.8	200Mhz	4ma	3pf	500hm	20%			
	HYPER_DQ[23]	DWC_GPIO18_INLINE_BDFS_H	LVCMOS	IO	1.8	200Mhz	4ma	3pf	500hm	20%			
	HYPER_CSN[3]	DWC_GPIO18_INLINE_OUT_H	LVCMOS	O	1.8	200Mhz	4ma	3pf	500hm	20%			
	HYPER_CK[3]	DWC_GPIO18_INLINE_OUT_H	LVCMOS	O	1.8	200Mhz	4ma	3pf	100Ohm Diff Pair	10%			
	HYPER_CKN[3]												-26db
	HYPER_PSC[3]	DWC_GPIO18_INLINE_OUT_H	LVCMOS	O	1.8	200Mhz	4ma	3pf	100Ohm Diff Pair	10%			
	HYPER_PSCN[3]												
	HYPER_RWDS[3]	DWC_GPIO18_INLINE_BDFS_H	LVCMOS	IO	1.8	200Mhz	4ma	3pf	500hm	20%			
	HYPER_RSTN[3]	DWC_GPIO18_INLINE_OUT_H	LVCMOS	O	1.8	200Mhz	4ma	3pf	500hm	20%			
	HYPER_DQ[24]	DWC_GPIO18_INLINE_BDFS_H	LVCMOS	IO	1.8	200Mhz	4ma	3pf	500hm	20%		120 ps	
	HYPER_DQ[25]	DWC_GPIO18_INLINE_BDFS_H	LVCMOS	IO	1.8	200Mhz	4ma	3pf	500hm	20%			
	HYPER_DQ[26]	DWC_GPIO18_INLINE_BDFS_H	LVCMOS	IO	1.8	200Mhz	4ma	3pf	500hm	20%			
	HYPER_DQ[27]	DWC_GPIO18_INLINE_BDFS_H	LVCMOS	IO	1.8	200Mhz	4ma	3pf	500hm	20%			
	HYPER_DQ[28]	DWC_GPIO18_INLINE_BDFS_H	LVCMOS	IO	1.8	200Mhz	4ma	3pf	500hm	20%			
	HYPER_DQ[29]	DWC_GPIO18_INLINE_BDFS_H	LVCMOS	IO	1.8	200Mhz	4ma	3pf	500hm	20%			
	HYPER_DQ[30]	DWC_GPIO18_INLINE_BDFS_H	LVCMOS	IO	1.8	200Mhz	4ma	3pf	500hm	20%			
	HYPER_DQ[31]	DWC_GPIO18_INLINE_BDFS_H	LVCMOS	IO	1.8	200Mhz	4ma	3pf	500hm	20%			
	HYPER_CSN[4]	DWC_GPIO18_INLINE_OUT_H	LVCMOS	O	1.8	200Mhz	4ma	3pf	500hm	20%			
	HYPER_CK[4]	DWC_GPIO18_INLINE_OUT_H	LVCMOS	O	1.8	200Mhz	4ma	3pf	100Ohm Diff Pair	10%			-26db
	HYPER_CKN[4]												-26db
	HYPER_RWDS[4]	DWC_GPIO18_INLINE_OUT_H	LVCMOS	O	1.8	200Mhz	4ma	3pf	100Ohm Diff Pair	10%			
	HYPER_RSTN[4]												
	HYPER_PSC[4]	DWC_GPIO18_INLINE_OUT_H	LVCMOS	O	1.8	200Mhz	4ma	3pf	500hm	20%			
	HYPER_PSCN[4]	DWC_GPIO18_INLINE_OUT_H	LVCMOS	O	1.8	200Mhz	4ma	3pf	500hm	20%			
	HYPER_DQ[32]	DWC_GPIO18_INLINE_BDFS_H	LVCMOS	IO	1.8	200Mhz	4ma	3pf	500hm	20%		120 ps	
	HYPER_DQ[33]	DWC_GPIO18_INLINE_BDFS_H	LVCMOS	IO	1.8	200Mhz	4ma	3pf	500hm	20%			
	HYPER_DQ[34]	DWC_GPIO18_INLINE_BDFS_H	LVCMOS	IO	1.8	200Mhz	4ma	3pf	500hm	20%			
	HYPER_DQ[35]	DWC_GPIO18_INLINE_BDFS_H	LVCMOS	IO	1.8	200Mhz	4ma	3pf	500hm	20%			
	HYPER_DQ[36]	DWC_GPIO18_INLINE_BDFS_H	LVCMOS	IO	1.8	200Mhz	4ma	3pf	500hm	20%			
	HYPER_DQ[37]	DWC_GPIO18_INLINE_BDFS_H	LVCMOS	IO	1.8	200Mhz	4ma	3pf	500hm	20%			
	HYPER_DQ[38]	DWC_GPIO18_INLINE_BDFS_H	LVCMOS	IO	1.8	200Mhz	4ma	3pf	500hm	20%			
	HYPER_DQ[39]	DWC_GPIO18_INLINE_BDFS_H	LVCMOS	IO	1.8	200Mhz	4ma	3pf	500hm	20%			

The External I/O are shown in the table above for the connections to the external memory (5x) HyperRAM devices from the IP Core front end PHY.

SIMULATION ENVIRONMENT

ENVIRONMENT VARIABLES

All component directories contain a local ./simulation directory containing a **makefile** and one or more **testbenches**. Testbenches use a _tb.vhd postfix. Each makefile is a linux gnu compatible make file that contains rules to rebuild the testbench's associated libraries, module files and testbench itself. The makefiles are setup by default to use Questa-sim [>=2022.02] and inherit parameters from a global shared makefile.inc file.

Each makefile requires the following user/system environment variables to be set:

1. ${PROJECTS} – This is typically the directory one up from the source and is the root of all the IP.
2. ${RTHYPERRAMIP} – This is the base address of the IP Core e.g. ${PROJECTS}/RTHyperRAMIPCore/

MODULE LEVEL SIMULATION

Each module directory has a local simulation testbench available. To run individual module level simulation regressions perform the following:

1. > cd <module-dir>/simulation
2. (Only required one time at project setup) > make clean_all
3. > make clean REGRESSION
4. This will build, run and report the pass/fail status of the complete regression suite.

TOP LEVEL SIMULATION

The top level IP Core has a directed test sequence and constrained random sequence test environment. The outputs of the IP core are dynamically checked using a SystemC (C++ Core) CPU Model that exercises the AXI4 Bus.

1. > cd <top-level-dir>/simulation
2. (Only required one time at project setup) > make clean_all
3. > make clean REGRESSION
4. This will build, run and report the pass/fail status of the complete regression suite.

IMPLEMENTATION

SYNTHESIS SCRIPTS

Example DC Ultra synthesis scripts and SDC timing scripts are provided with the IP.

IMPLEMENTATION RESOURCE ESTIMATES

The complete IP Core has been Synthesized, Placed and Routed, static timing analyzed, and processed using Xilinx Vivado 2024.2 tool suite for emulation.

The summary of the per module, and total resource utilization is provided below:

- Target FPGA is set to XCKU3P-FFVA676-2-E
- Clock Constraints are set to 100Mhz
- The RS FEC Decoder is configurable to trade latency for performance during error correction. The Area of the Decoder varies significantly based on this setting [12K to 39K LUTs]
- In 22FDX-SOI the Full Design is approximately 1.2mm^2
    - Actual silicon area will vary significantly based upon FIFO Memory Type, Depth, Decoder Parallelism, Frequency, and DFT options.

[UPDATE TO BE PROVIDED FOR EMULATION COMPILE in US+ FPGA]

Figure 9 IP Core Resource Utilization in AMD-XILINX Ultrascale+ Emulation FPGA

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