Technical Rationale

Modifications to PRC-006-NPCC-2 (Automatic Underfrequency Load Shedding Operating Time Tolerances) | March 2025

PRC-006-NPCC-3 – Automatic Underfrequency Load Shedding

Introduction:
This document explains the technical rationale and justification for the proposed Reliability Standard PRC-006-NPCC-3. It provides stakeholders within the Regional Entity with an understanding of the technical limitations necessary to consider for practical implementation of Regional Standard requirements.

Changes were made to the tolerances identified for Automatic Underfrequency Load Shedding (UFLS) scheme nominal operating times to respond to issues raised by NPCC Task Force on System Protection (TFSP), specifying that:

> The drafting team must reconsider adding the +/- 50ms tolerance back into Footnote 1 for the UFLS blocks that operate in 300ms and in addition, consider a reasonable tolerance for the 10s anti-stall stage.

Subsequent modifications were made consistent with the five-year review of the standard per the Regional Standards Processes Manual requirement.

Background:
Lack of incorporating of the +/- 50 ms tolerance for UFLS nominal operating time previously provided in NPCC Regional Reliability Reference Directory # 12[1] led to confusion regarding differing interpretations and expectations during the NPCC audits of PRC-006-NPCC-2. The omission implies that the nominal time listed for each UFLS stage is design criteria and systems must operate exactly at the specified time. Since the operation of the UFLS program contains various vintages of relays and interrupting devices, it is not realistic to specify an exact operate time without providing for tolerances on that nominal operate time.

It has been disclosed that Planning applications study the UFLS plan performance utilizing fixed assumptions based on the nominal quantities. That is, studies simulate interruption of current at precisely 0.30 seconds for Stages 1-4 and 10.0 seconds for Stage 5. Additionally, the MW quantities studied precisely follow the survey results provided by the individual entities. While some real-world deviation is assumed, only these assumptions are studied due to the wide range of other parameters under study.

However, specifying overly stringent ranges for both the load shed quantity and nominal operating time for the actual UFLS plan adversely affects the implementation of the scheme when faced with real-world complications.

[1] NPCC Regional Reliability Reference Directory # 12 was retired effective October 1, 2021, to coincide with the enforcement of NPCC Regional Reliability Standard PRC-006-NPCC-2 in all jurisdictions.

To increase the likelihood of the response assumed by planning studies and system operators to occur in real life scenarios, the following ranges were modified to:

- Re-establish +/- 50 ms Tolerance for Nominal 300 ms UFLS Stages in Appendix C Tables 1-3
- Establish +/- 350 ms Tolerance for UFLS Stage 5 in Appendix C Table 1
- Remove Upper Margin for Cumulative Load Shed Requirement in Appendix C Table 1
- Redefine Breaker Interrupting Time

Rationale:

Rationale for Re-establishing +/- 50 ms Tolerance for UFLS Stages 1-4:
The +/- 50 ms range previously specified in NPCC Regional Reliability Reference Directory # 12 (D12) is restored. The original criteria were established by a special studies group within NPCC charged with establishing the basic criteria for the design of the UFLS programs to ensure declining frequency is arrested and recovered in accordance with established NPCC performance requirements to prevent system collapse due to a load-generation imbalance.

The +/-50 ms tolerance additionally compliments use of the term “nominal” as exceeding these thresholds would result in a value other than 300 milliseconds based on the rules of rounding and significant figures.

Rationale for Establishing +/- 350 ms Tolerance for UFLS Stage 5:
The tolerance for the anti-stall stage is approached differently as 50ms does not provide sufficient leeway due to variation of relay response for the applicable frequencies for performing anti-stall function and the frequency ramp rate prescribed for test purposes.

For relays which operate in seconds, the 10 second nominal operating time setting target can be predictably achieved by deducting the breaker timing and relay pickup delay. Relays with underfrequency element delay based in cycles may determine time differently depending on the nature of the underfrequency event. As frequency decays, each cycle represents more time as measured in seconds. This introduces negligible difference in operating times for 300 ms stages but has significant impact for the anti-stall stage. For example, 600 cycles represent 10 seconds at 60Hz, but 10.35 seconds at 58 Hz. A relay set in cycles to perfectly achieve 10 second interruption for a stall condition with system frequency held constant at 59.5 Hz cannot simultaneously achieve 10 second tripping when evaluated by the continuous decay state prescribed by the ramp test rate within Attachment C. The time difference between these two valid conditions exceeds 50 ms, therefore a wider tolerance is necessary for Stage 5 than the previous stages.

An appropriate tolerance range for the anti-stall stage was derived from rigorous mathematical evaluation of several constant frequencies, the linear ramp rate test of -0.2 Hz/second, and the minimum underfrequency criteria provided by Figure 1. Further details are provided in Attachment 1 of this document.

The results of the evaluation indicate that any reasonable interpretation for setting a relay in cycles to achieve a nominal 10 second operating time could yield a range of results from 9.667 seconds to 10.345 seconds, when evaluated under other various frequency criteria.

Thus, establishing a +/- 350 ms tolerance to allow for nominal operating times between 9.65 and 10.35 seconds permits entities to make reasonable interpretations for calculating ten seconds under various valid frequency conditions.

The drafting team considered ensuring the ten second timing requirements coordinated with the generator tripping requirements provided by Figure 2, however ultimately determined that Figure 1 specifies the UFLS scheme requirements and inherently coordinates with the generator assumptions of Figure 2. This assumption can be crudely validated by considering that Figure 2 specifies that generator tripping is only permitted at 58.0 Hz after 30 seconds, providing approximately 20 seconds of margin from an anti-stall trip.

Additional consideration was given for specifying a +/- 500 ms tolerance. In the same way that +/-50 ms tolerance compliments use of the term “nominal” for 300 milliseconds, a +/- 500 ms tolerance compliments “nominal” ten seconds based on the rules of rounding and significant figures.
However, the fact that planning simulations target 10 seconds exactly led to the conclusion that a tighter band should be pursued to provide clarity that entities should directly target 10 seconds.

The drafting team requested the SS-38 Working Group on Inter-Area Dynamic Analysis assess UFLS operating times with a tolerance of +/- 500 ms rather than the proposed +/- 350 ms range. The intent of this was to firmly identify +/- 350 ms as a technically sound limitation, with ample margin. Having studied the UFLS performance at +/-500 ms with passing results, there is increased confidence that approaching the limits of +/-350 ms in real world applications will not risk system stability.

The drafting team agreed to pursue +/- 350 ms tolerance for UFLS Stage 5 to establish technically sound and achievable limitations.

Rationale for Removal of Upper Margin for Cumulative Load Shed:
For entities with load greater than 100MW, the proposed changes and the nature of the individual stage requirements assures an upper boundary of 33% at Stage 5 compared to previous 31.5% for Table 1, assuming compensatory load shed is implemented appropriately. The additional flexibility of 1.5% over five UFLS Stages is proposed to alleviate an inequitable and impractical restriction placed on entities with load greater than 100 MW. The individual stage margin is stringent enough and enforcing an upper range of the cumulative requirement only compounded this, providing the same minimal leeway for the summation of all stages.

The capacity deficiency events in the last decade suggest there is risk of insufficient actualized load shed versus planned load shed which can result in insufficient frequency recovery. Therefore, greater focus should be allotted towards ensuring the minimum cumulative range is met than capping the upper cumulative range. While there is risk to automatic UFLS overshedding resulting in an overfrequency condition and further generation tripping, the 1.5% additional tolerance spread over several stages is unlikely to be the sole source of such an overcorrection.

It is worth noting that this change only impacts Table 1 associated with entities with load greater than 100 MW. Mathematically, the previous upper range for Table 2 and Table 3 are guaranteed by the individual stage ranges. Table 3 only has a single stage while the individual

range for Table 2 is 14-25% with the cumulative requirement for Stage 2 at 28-50%, simply two times the upper and lower limit.

Reevaluating the tight cumulative tolerance is merited based on further considering the differences between the UFLS program requirements for entities of different sizes. The nature of the UFLS requirements for smaller entities inherently inflates the total UFLS program response at 59.5Hz and 59.1Hz, with no impact to UFLS program responses at 59.3Hz, 58.9Hz, or for anti-stall purposes.
Entities smaller than 25MW are entitled not to shed load at all, entities between 25 and 50 MW shed load at 59.5Hz only, and entities between 50 and 100 MW contain stages impacting 59.5Hz and 59.1Hz.

The percentage targets for entities applicable to Tables 2-3 both generate a MW range of 5.5-11 MW to satisfy an individual stage. As entities exceed 100MW, the MW range by stage becomes significantly more unforgiving. For an entity supplying 100MW, the 6.5-7.5% range offers only 1 MW of leeway within any particular stage. At this point, a single feeder can easily represent more than the entire tolerance range.

The main purpose of the legacy cumulative load shed requirement for Table 1 was to align the UFLS program with the planning and operational organization assumptions of ideal 7% load blocks for UFLS Stages 1-4 and a load block of 2% for Stage 5. While this makes intuitive sense, enforcing rounding convention to idealized percentage values presents more significant implementation challenges when faced with technical realities. Enforcing this stringent range already places a more restrictive requirement on larger entities, and further enforcing the upper cumulative range further complicates actualization. It is inconsistent for the standard to enforce 1 MW tolerance on the net effect of five stages for larger entities while permitting smaller entities to shed additional load at only two particular stages with wider tolerance.

While ensuring that entities do not specify the minimum 6.5% for multiple stages makes sense, enforcing the same limitation for the upper bound of 7.5% practically ensures entities will require yearly changes to the program, which may detriment other conflicting goals such as minimalizing the impact to critical facilities and optimizing the overlap between underfrequency load shed and manual load shed. It is not reasonable to assume sufficient variability of feeder size exists to cover the need to continuously manipulate the UFLS plan in a manner that does not compromise a separate goal of the combined load shed philosophy. Additional issues including DER masking and different individual feeder peaks during the various load cycles make it difficult to maintain such precision from year to year.

With the removal of the upper margin, larger entities are provided more freedom to target stable 7% load blocks and align with qualitative considerations such as the exemption of critical facilities and optimization with manual load shed programs, while still ensuring a reliable lower limit very near to the 7% target.

Rationale for Defining Breaker Interrupting Time:
The previous iteration of this Regional Standard focused heavily on the impacts of underfrequency and auxiliary relay operating times and communication delays but specified rated breaker operating time. Rated breaker operating time is defined conservatively and does not reflect the effects of aging or maintenance efforts. Entities with more sophisticated testing methods are now free to treat the breaker operating time with the same precision as

estimations given for relay operating times and communication delays, in order to more precisely target nominal operating times consistent with Attachment C requirements. In the event such data is not available, the rated operating time is still permissible to consider, as is a combination of the two values in the spirit of achieving operating times consistent with Attachment C.

Attachment 1

A mathematical evaluation of reasonable interpretations for reflecting the 10 second nominal time to cycles was performed. This explores impacts of underfrequency conditions on relay operating times for relays that measure time in cycles.

First, the integrals of time-frequency plots for several frequency conditions were evaluated from zero to 10 seconds. This yields the decayed-frequency cycles experienced during the selected conditions at the ten second mark, where time zero is defined as the moment when frequency passes 59.5 Hz.

After this, each experienced cycle count was evaluated using each of the alternate frequency conditions. This yields the possible time ranges in seconds which may be experienced for each count of cycles when evaluated under different frequency assumptions.

Determining Cycles Experienced at 10 Seconds:

Normal System Frequency of 60 Hz:

Use of flat 60 Hz is technically unsound due to the nature of frequency decay; however, this represents the typical philosophy for other relay elements under normal system conditions.

$$\int_0^{10} (60.0)\, dt = 600\ cyc$$

Stage 1 Pickup of 59.5 Hz:

Use of flat 59.5 Hz is representative of a true anti-stall application, where UFLS Stage 1 sufficiently arrests the frequency decline, but is not sufficient to promote frequency recovery. This philosophy was previously recommended as best practice for PRC-006-NPCC-2 compliance.

$$\int_0^{10} (59.5)\, dt = 595\ cyc$$

Stage 4 Pickup of 58.9 Hz:

Flat 58 Hz Use of flat 58.9 Hz is representative of an anti-stall application after UFLS Stages 1-4 have already actuated.

$$\int_0^{10} (58.9)\, dt = 589\ cyc$$

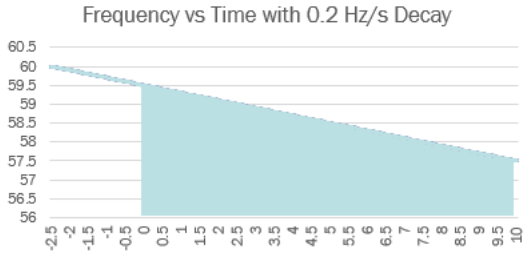
Linear -0.2 Hz/sec Ramp Rate Test:

The -0.2 Hz per second decline specified in Footnote 1 is the official testing criteria for UFLS operating times. Time is measured from the time when frequency passes the frequency threshold setpoint, 59.5 Hz in the case of Stage 5.

(t=0 when 59.5 Hz pickup is passed)

(10 real seconds) ← $\int_0^{10} (59.5 - 0.2x)\, dx$ → (Decayed cycles experienced at 10 seconds)

(start time of 'nominal') ←



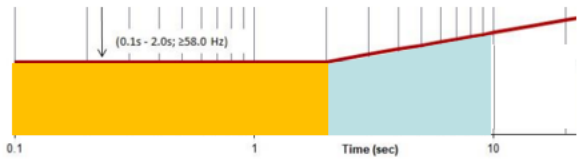
$$\int_0^{10} (59.5 - 0.2x)\, dx$$

$$[59.5x - 0.1x^2]_0^{10} = 585\ cyc$$

Minimum Acceptable UFLS Criteria:

The UFLS Performance Characteristics from PRC-006-NPCC-2 Figure 1 represent the most extreme permissible underfrequency conditions for which UFLS schemes are designed.

For the sake of analysis, a high rate of frequency change is assumed such that the frequency drops through 59.5 Hz to 58 Hz instantaneously. The Underfrequency Performance Characteristic Curve remains at constant 58.0 Hz for two seconds before recovering at a logarithmic rate described with frequency equaling 0.575 log(t) + 57.83 Hz.



Underfrequency Requirements	
t ≤ 2 s	f = 58.0 Hz
2 s < t ≤ 30 s	f = 0.575log(t) + 57.83 Hz
t > 30 s	f = 59.5 Hz

$$\int \log_a x\, dx = x \log_a x - \frac{x}{\ln a} = \frac{x}{\ln a}(\ln x - 1)$$

$$\int_0^2 (58.0)\, dt$$

$$[58.0t]_0^2$$

$$[58.0 * (2 - 0)]$$

$$116\ cycles$$

$+$

$$\int_2^{10} (0.575 * \log(t) + 57.83)\, dt$$

$$0.575 * \left[t * (\log(t) - \frac{t}{\ln(10)}) + \frac{57.83}{0.575} t\right]_2^{10}$$

$$0.575 * \left[10 * (\log(10) - \frac{10}{\ln(10)} - \left(2 * \log(2) - \frac{2}{\ln(10)}\right) + 100.574\ (10 - 2)\right]$$

$$0.575 * [(10 - 4.3429) - (0.6021 - 0.8686) + 804.592]$$

$$0.575 * [\ (5.6571 - (-0.2665) + 804.592]$$

$$466.05\ cycles$$

$$116\ cycles + 466.05\ cycles = 582\ cycles$$

Constant 58 Hz Beyond Acceptable UFLS Criteria:

Using a flat frequency of 58 Hz offers a more extreme case, as Figure 1 requires frequency to be above 58 Hz after the first two seconds based on the equations given by PRC-006-NPCC-2 Figure 1. Using constant 58 Hz yields sufficiently close results with less complicated math.

$$\int_0^{10} (58.0)\, dt = 580\ cyc$$

Summary of Experienced Cycles at 10s for Various Underfrequency Conditions:

$\int_0^{10} (58.0)\, dt$

$580\ cycles$

Constant 58 Hz – Beyond Design Criteria

$600\ cycles$

At Nominal 60 Hz

$\int_0^{2} (58.0)\, dt\ +$

$\int_2^{10} (0.575 * \log(t) + 57.83)\, dt$

$582\ cycles$

Minimum UFLS Performance Characteristics from PRC-006-NPCC-2 Figure 1

$\int_0^{10} (58.9)\, dt$

$589\ cycles$

$\int_0^{10} (59.5)\, dt$

$595\ cycles$

Constant 58.9 Hz (Stage 4) – Constant 59.5 Hz (Stage 1)

$\int_0^{10} (59.5 - 0.2x)\, dx$

$585\ cycles$

-0.2 Hz/sec Ramp Test Result

Impact of Timing in Seconds Under Various Frequency Assumptions:
These values for the cycles experienced at the ten second mark were then evaluated against each of the alternative frequency assumptions.

For each of the constant frequencies, the timing in seconds is derived by taking the number of cycles and dividing by the frequency under evaluation.

For the two more complicated equations, the count of seconds is defined by evaluating the indefinite integral of the equations, then solving for the count of seconds given the count of cycles.

Ramp Rate Test:

$$\int_0^{second} (59.5 - 0.2x)\, dx = cycle$$

$$[59.5x - 0.1x^2]_0^{sec} = cycle$$
$$[59.5sec - 0.1sec^2] = cycle$$

$$0.1sec^2 - 59.5sec + cycle = 0$$

The above equation is evaluated using the Quadratic Formula for each of the cycle options.

Minimum UFLS Performance Curve:

$$2\ seconds\ at\ 58\ Hz = 116\ cycles$$

$\int_2^{fsec} (0.575 * \log(t) + 57.83)\, dt$ = cycles - 116

$$0.575 * \left[t * (\log(t) - \frac{t}{\ln(10)}) + \frac{57.83}{0.575}\, t\right]_2^{fsec}$$

$$0.575 * \left[fsec * (\log(fsec) - \frac{fsec}{\ln(10)} - \left(2 * \log(2) - \frac{2}{\ln(10)}\right) + 100.574\ (fsec - 2)\right]$$

$$0.575 * \left[fsec * (\log(fsec) - \frac{fsec}{\ln(10)} - (-0.2665) + 100.574\ (fsec - 2)\right]$$

$$cycle = 116 + 0.575 * \left[fsec * (\log(fsec) - \frac{fsec}{\ln(10)} - (-0.2665) + 100.574\ (fsec - 2)\right]$$

$$cycle = 116 + 0.575 * [fsec * (\log(fsec) - 0.4343 fsec - (-0.2665) + 100.574\ fsec - 201.148]$$

For the minimum UFLS characteristic, manually calculated charts evaluated the continuum, and the appropriate cycle/second pairings were selected. This avoided complicated integration involving logarithms.

Result Matrix:

	Results (sec) by Evaluation Criteria					
'10s' Cycle Count	58.0 Hz	Min Criteria	Ramp Test	58.9 Hz	59.5 Hz	60.0 Hz
600 *cycles*	10.345	10.307	10.261	10.187	10.084	10.000
595 *cycles*	10.259	10.222	10.174	10.102	10.000	9.917
589 *cycles*	10.155	10.119	10.070	10.000	9.899	9.817
585 *cycles*	10.086	10.051	10.000	9.932	9.832	9.750
582 *cycles*	10.034	10.000	9.948	9.881	9.782	9.700
580 *cycles*	10.000	9.965	9.913	9.847	9.748	9.667