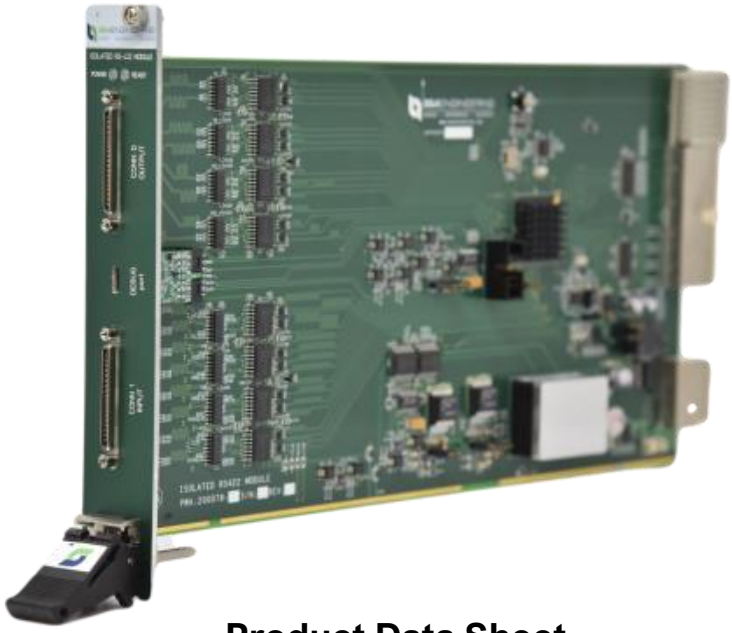
# Isolated Single-Ended Module



**Product Data Sheet**
B&A Document 110022_B

Part No.
200103

B&A ENGINEERING
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## INTRODUCTION

This document contains technical specifications for the Isolated Single-Ended Module (B&A Part No. 200103). Specifications are shown at 25 °C temperature, unless otherwise noted. The main features of the module are listed below:

- Separate 32 Transmit and 32 Receive Single-Ended (LVTTL, TTL, CMOS, Open Drain) channels(1)
- Configurable grounding
- On-board Isolated voltage regulation
- Internal House Keeping / Health Monitoring
- User-controlled Flight interface power on/off
- Built-in LabVIEW FPGA Debugging Port
- Safe to connect to Flight hardware, FMEA approved
- LabVIEW drivers

## SAFETY

The following items must be considered for safety:

- Using the Isolated Single-Ended Module in a manner not described within this document may impair the protection of the Isolated Single-Ended Module provides.
- The SLSC-12001 chassis and the SLSC Modules **do not support** hot plug-in. The entire chassis must be powered down when a module is installed.
- Sense lines **do not support** reverse polarity.
- Always follow ESD procedures for handling.
- If cleaning is required, wipe with dry and clean towel.
- Installation of the Isolated Single-Ended Module must be performed in accordance with "B&A SLSC Module User Manual" (Document No. 140040).

## INTERFACES

| | |
|---|---|
| Front panel Connectors | 2 x VHDCI (Page 6 & 7) |
| Backplane Connectors | 3 x SLSC (Page 8 & 9) |
| Power Up State | Drivers and receivers disabled |
| I/O Compatibility | Single-Ended Signaling [LVTTL, TTL, CMOS, Open Drain] |
| Number of on-card Temperature Sensors | 4 |
| LabVIEW FPGA Debug Interface | Micro-USB |
| Grounding Configuration | See Page 4 |

## SPECIFICATIONS(3)

| | |
|---|---|
| Channels Per Connector(2) | 32 |
| Number Of Single-ended Channels | 32 |
| Termination Impedance | Optional 4.7 kΩ Pull-Up and Pull-Down Resistors |
| In-Line Series Resistance | 25 Ω nominal |
| Properties | See Page 10 |
| Register Mapping | See Page 11 |
| Configuration Option | See Page 12 (Tables 1 & 2) |

**Note:**

(1) All 32 channels (TX and RX) are length-matched and have the same delay on the board.

(2) For further specification details, please contact support@baengineering.com



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## STANDARD CONFIGURATIONS SPECIFICATIONS

| Available Part No. | Physical Protocol | Isolated Domain Voltage | Drive Series Resistance | Receiver Series Resistance | Receiver Pull-up Resistance | Receiver Pull-down Resistance | Ground Scheme |
|---|---|---|---|---|---|---|---|
| 200103-00 | LVTTL | 3.3 V | 25 Ω | 25 Ω | Open | Open | 2.2 MΩ II 100 nF |
| 200103-01 | Open Collector/Drain | 3.3 V | 100 Ω | 25 Ω | 10 kΩ | Open | 2.2 MΩ II 100 nF |
| 200103-02 | TTL | 5.0 V | 25 Ω | 25 Ω | Open | Open | 2.2 MΩ II 100 nF |
| 200103-XX | Customizable based on customer requests. (See the last page for ordering instructions) | | | | | | |

| Standard Configurations Specifications | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Physical Protocol | LVTTL | | Open drain | | TTL | | LVCMOS | | CMOS | | | |
| Isolated Domain Voltage (V) | 3.3 | | 3.3 | | 5.0 | | 3.3 | | 3.3 | | 5 | |
| | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max |
| Operational Voltage Range (V) | 18 | 40 | 18 | 40 | 18 | 40 | 18 | 40 | 18 | 40 | 18 | 40 |
| TX HL Propagation Delay (ns) | 8.1 | 22.5 | 14.7 | 26.4 | 8.1 | 22.5 | 8.1 | 22.5 | 8.1 | 22.5 | 8.1 | 22.5 |
| TX LH Propagation Delay (ns) | 8.1 | 22.5 | 27.7 | 39.4 | 8.1 | 22.5 | 8.1 | 22.5 | 8.1 | 22.5 | 8.1 | 22.5 |
| RX HL Propagation Delay (ns) | 8.1 | 22.5 | 8.1 | 22.5 | 8.1 | 22.5 | 8.1 | 22.5 | 8.1 | 22.5 | 8.1 | 22.5 |
| RX LH Propagation Delay (ns) | 8.1 | 22.5 | 8.1 | 22.5 | 8.1 | 22.5 | 8.1 | 22.5 | 8.1 | 22.5 | 8.1 | 22.5 |
| Output High Voltage (V) | 3.2 | 3.3 | N/A | | 4.9 | 5 | 3.2 | 3.3 | 3.2 | 3.3 | 4.9 | 5 |
| Output Low Voltage (V) | 0 | 0.1 | 100 Ω pull to ground | | 0 | 0.1 | 0 | 0.1 | 0 | 0.1 | 0 | 0.1 |
| Maximum Nominal Data Rate of TX and RX Channels (MHz) | 40 | | 40 | | 40 | | 40 | | 40 | | 40 | |
| Input Voltage (V) | 5.5 | | 5.5 | | 5.5 | | 5.5 | | 5.5 | | 5.5 | |
| Input High Voltage (mV) | 2 | | 2 | | 3.5 | | 2 | | 2 | | 3.5 | |
| Input Low Voltage (mV) | 0.8 | | 0.8 | | 1.5 | | 0.8 | | 0.8 | | 1.5 | |
| High Output Current (mA) | -24 | | N/A | | -32 | | -24 | | -24 | | -32 | |
| Low Output Current (mA) | 24 | | 2 | | 32 | | 24 | | 24 | | 32 | |
| Input Capacitance (pF) | 3.5 | | 3.5 | | 3.5 | | 3.5 | | 3.5 | | 3.5 | |
| Rise Time (ns) | 33 | | 10 | | 25 | | 33 | | 33 | | 25 | |
| Fall Time (ns) | 33 | | 8 | | 25 | | 33 | | 33 | | 25 | |



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## NON-STANDARD CONFIGURATIONS SPECIFICATIONS

| Available Part No. | Physical Protocol | Isolated Domain Voltage | Drive Series Resistance | Receiver Series Resistance | Receiver Pull-up Resistance | Receiver Pull-down Resistance | Ground Scheme |
|---|---|---|---|---|---|---|---|
| 200103-03 | LVTTL / Open Drain | 3.3 V | 25 Ω | 25 Ω | Open | Open | 2.2 MΩ II 100 nF |
| 200103-XX | Customizable based on customer requests. (See the last page for ordering instructions) | | | | | | |

| Non-Standard Configurations Specifications | | | | |
|---|---|---|---|---|
| Part Number | 200103-03 | | | |
| Physical Protocol | Channels 0 – 29 LVTTL | | Channels 30 - 31 Open Drain | |
| Isolated Domain Voltage (V) | 3.3 | | 3.3 | |
| | Min | Max | Min | Max |
| Operational Voltage Range (V) | 18 | 40 | 18 | 40 |
| TX HL Propagation Delay (ns) | 8.1 | 22.5 | 14.7 | 26.4 |
| TX LH Propagation Delay (ns) | 8.1 | 22.5 | 27.7 | 39.4 |
| RX HL Propagation Delay (ns) | 8.1 | 22.5 | 8.1 | 22.5 |
| RX LH Propagation Delay (ns) | 8.1 | 22.5 | 8.1 | 22.5 |
| Output High Voltage (V) | 3.2 | 3.3 | N/A | |
| Output Low Voltage (V) | 0 | 0.1 | 100 Ω pull to ground | |
| Maximum Nominal Data Rate of TX and RX Channels (MHz) | 40 | | 40 | |
| Input Voltage (V) | 5.5 | | 5.5 | |
| Input High Voltage (mV) | 2 | | 2 | |
| Input Low Voltage (mV) | 0.8 | | 0.8 | |
| High Output Current (mA) | -24 | | N/A | |
| Low Output Current (mA) | 24 | | 2 | |
| Input Capacitance (pF) | 3.5 | | 3.5 | |
| Rise Time (ns) | 33 | | 10 | |
| Fall Time (ns) | 33 | | 8 | |



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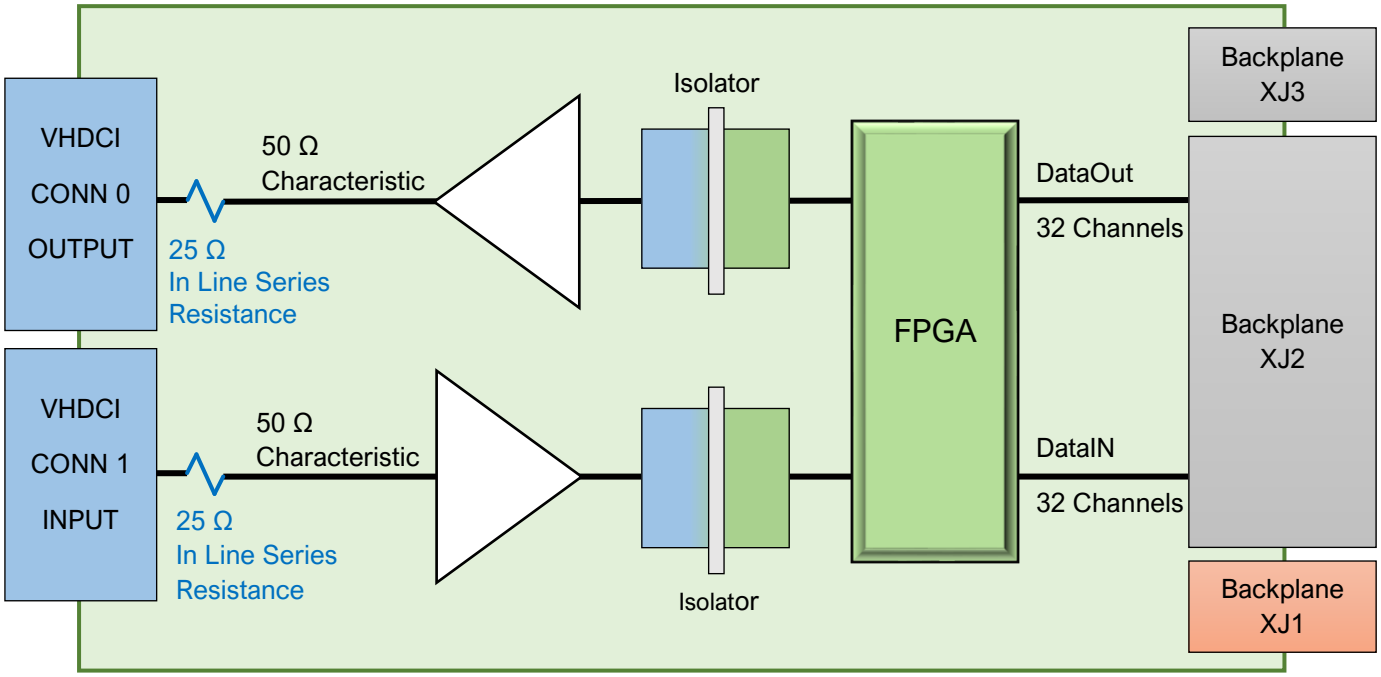
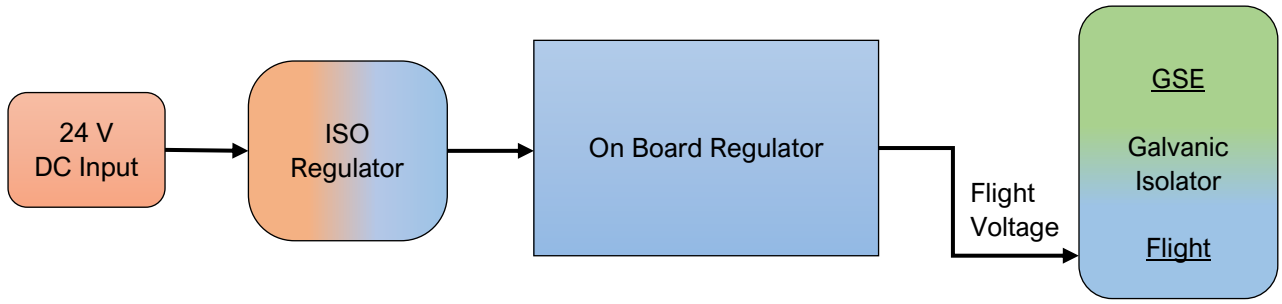
## FUNCTIONAL BLOCK DIAGRAM

The functional block diagram is shown below:




## ISOLATED VOLTAGE REGULATION

The Isolated Voltage Regulation block diagram is shown below:



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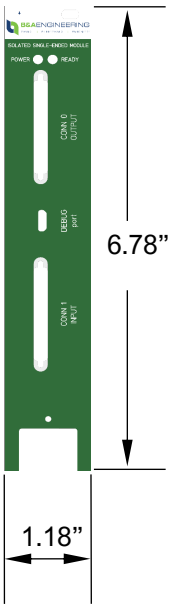
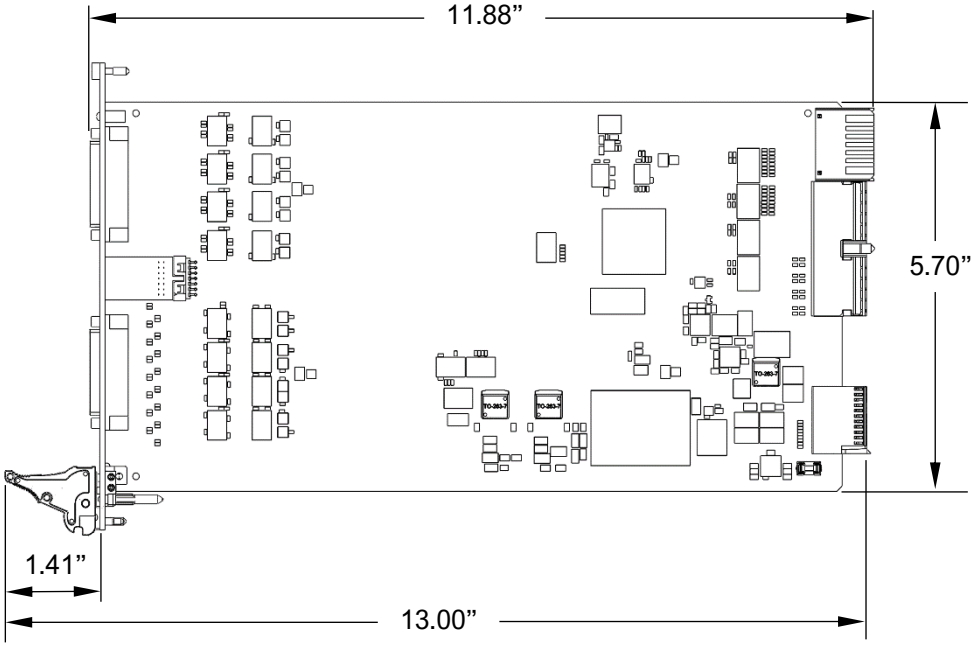
## PHYSICAL DIMENSIONS




**Front Panel View**

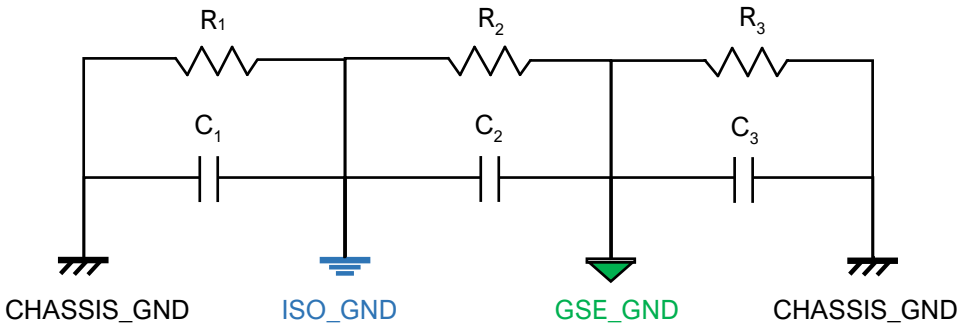



**Top View**

## CONFIGURABLE GROUNDING

Three different groundings are provided: **Chassis Ground**, **ISO Ground**, and **GSE Ground**.

- The module allows customizable grounding schemes by shorting the on-board resistors; $R_1$, $R_2$, and $R_3$.
- Capacitors $C_1$, $C_2$, and $C_3$ are used to implement RC filters.
- Isolated resistors and capacitors are installed on the module by default. ($R_1$= $R_2$ = $R_3$= 2.2 MΩ, $C_1$ = $C_2$=$C_3$=100 nF)
- Resistor and capacitor values can be configured based on users’ requirements upon order. Online customization tools are available on the B&A website.



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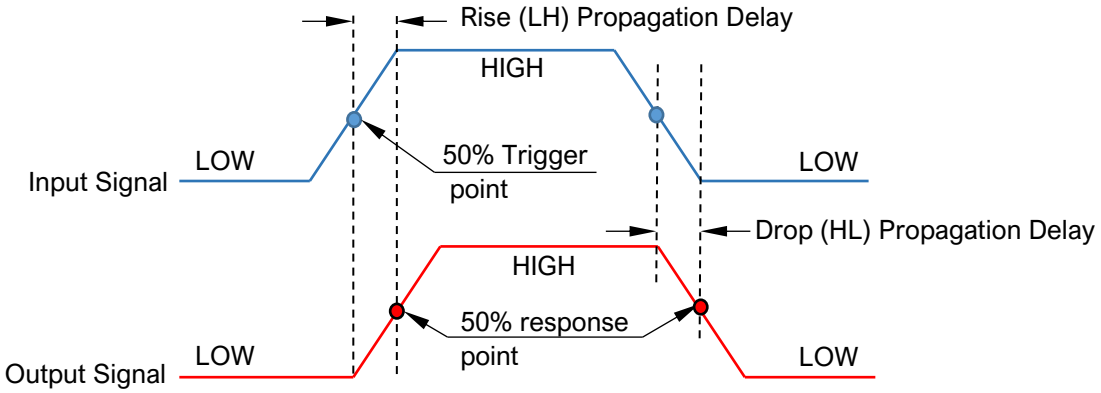
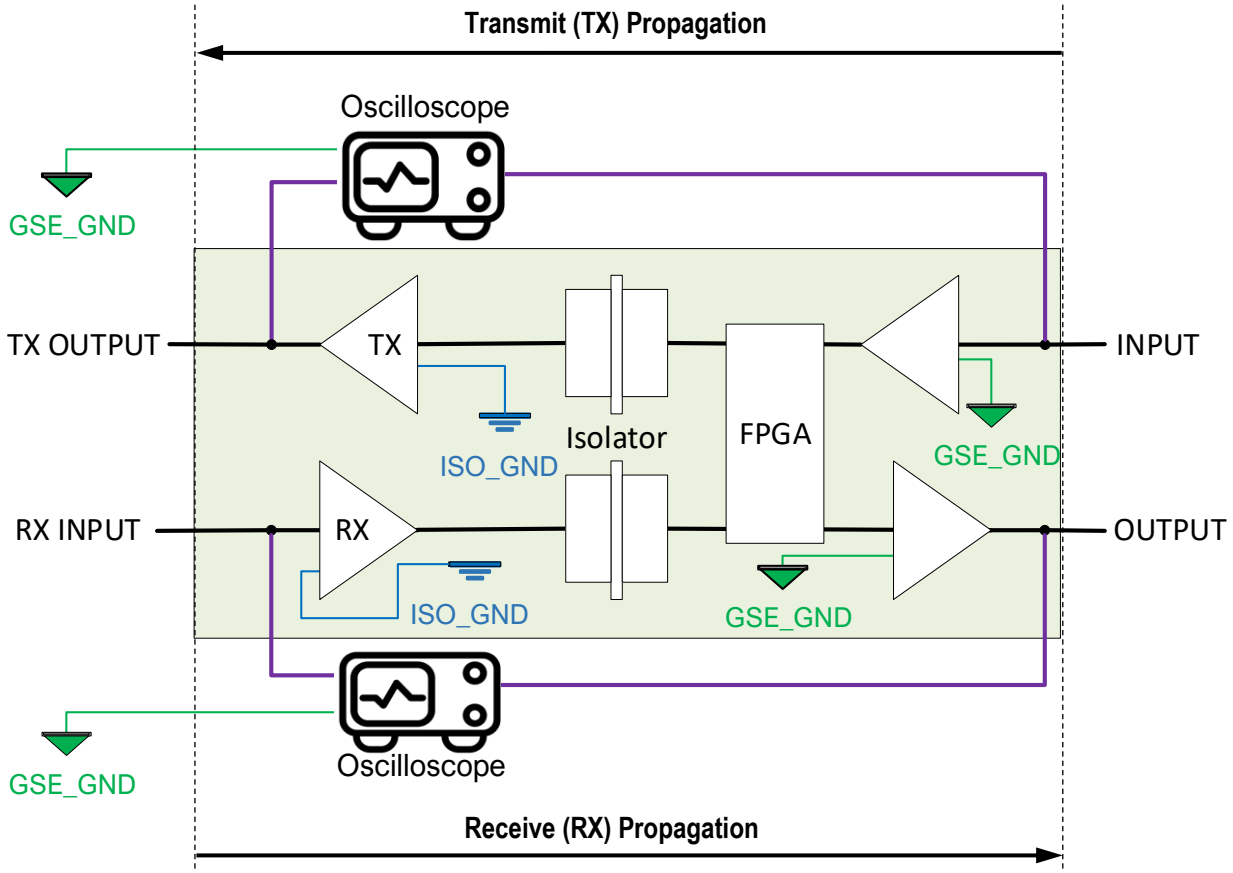
## PROPAGATION DELAY

The propagation delay is defined as the delay between the 50% trigger point and the 50% response point. The figure below illustrates two different propagation delays: The LOW to HIGH signal rise phase (LH) and HIGH to LOW signal Drop phase (HL). The signal rise and drop measurement is performed bi-directional for the TX and RX propagation direction. An Oscilloscope is required to perform testing. The signal data is measured with the oscilloscope at the board INPUT, TX output, RX input, and board OUTPUT. For delay measurements, ISO_GND and GSE_GND are connected.





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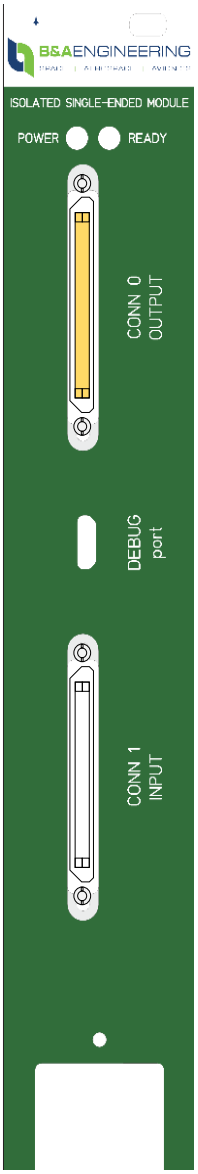
## FRONT CONNECTOR 0 PINOUT

| | | | |
|---|---|---|---|
| ISO_GND | 68 | 34 | ISO_GND |
| TX_31 | 67 | 33 | TX_15 |
| ISO_GND | 66 | 32 | ISO_GND |
| TX_30 | 65 | 31 | TX_14 |
| ISO_GND | 64 | 30 | ISO_GND |
| TX_29 | 63 | 29 | TX_13 |
| ISO_GND | 62 | 28 | ISO_GND |
| TX_28 | 61 | 27 | TX_12 |
| ISO_GND | 60 | 26 | ISO_GND |
| ISO_GND | 59 | 25 | ISO_GND |
| TX_27 | 58 | 24 | TX_11 |
| ISO_GND | 57 | 23 | ISO_GND |
| TX_26 | 56 | 22 | TX_10 |
| ISO_GND | 55 | 21 | ISO_GND |
| TX_25 | 54 | 20 | TX_9 |
| ISO_GND | 53 | 19 | ISO_GND |
| TX_24 | 52 | 18 | TX_8 |
| ISO_GND | 51 | 17 | ISO_GND |
| TX_23 | 50 | 16 | TX_7 |
| ISO_GND | 49 | 15 | ISO_GND |
| TX_22 | 48 | 14 | TX_6 |
| ISO_GND | 47 | 13 | ISO_GND |
| TX_21 | 46 | 12 | TX_5 |
| ISO_GND | 45 | 11 | ISO_GND |
| TX_20 | 44 | 10 | TX_4 |
| ISO_GND | 43 | 9 | ISO_GND |
| ISO_GND | 42 | 8 | ISO_GND |
| TX_19 | 41 | 7 | TX_3 |
| ISO_GND | 40 | 6 | ISO_GND |
| TX_18 | 39 | 5 | TX_2 |
| ISO_GND | 38 | 4 | ISO_GND |
| TX_17 | 37 | 3 | TX_1 |
| ISO_GND | 36 | 2 | ISO_GND |
| TX_16 | 35 | 1 | TX_0 |



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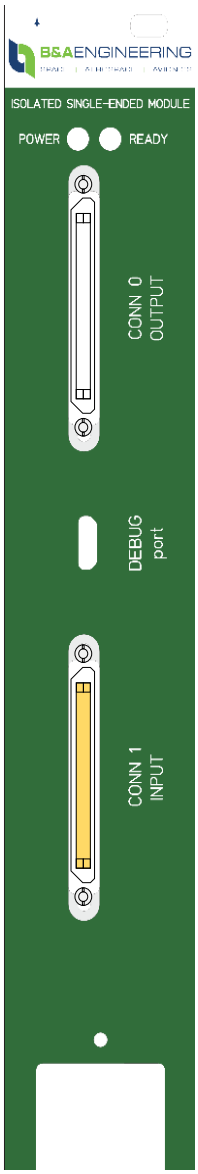
## FRONT CONNECTOR 1 PINOUT

| | | | |
|---|---|---|---|
| ISO_GND | 68 | 34 | ISO_GND |
| RX_31 | 67 | 33 | RX_15 |
| ISO_GND | 66 | 32 | ISO_GND |
| RX_30 | 65 | 31 | RX_14 |
| ISO_GND | 64 | 30 | ISO_GND |
| RX_29 | 63 | 29 | RX_13 |
| ISO_GND | 62 | 28 | ISO_GND |
| RX_28 | 61 | 27 | RX_12 |
| ISO_GND | 60 | 26 | ISO_GND |
| ISO_GND | 59 | 25 | ISO_GND |
| RX_27 | 58 | 24 | RX_11 |
| ISO_GND | 57 | 23 | ISO_GND |
| RX_26 | 56 | 22 | RX_10 |
| ISO_GND | 55 | 21 | ISO_GND |
| RX_25 | 54 | 20 | RX_9 |
| ISO_GND | 53 | 19 | ISO_GND |
| RX_24 | 52 | 18 | RX_8 |
| ISO_GND | 51 | 17 | ISO_GND |
| RX_23 | 50 | 16 | RX_7 |
| ISO_GND | 49 | 15 | ISO_GND |
| RX_22 | 48 | 14 | RX_6 |
| ISO_GND | 47 | 13 | ISO_GND |
| RX_21 | 46 | 12 | RX_5 |
| ISO_GND | 45 | 11 | ISO_GND |
| RX_20 | 44 | 10 | RX_4 |
| ISO_GND | 43 | 9 | ISO_GND |
| ISO_GND | 42 | 8 | ISO_GND |
| RX_19 | 41 | 7 | RX_3 |
| ISO_GND | 40 | 6 | ISO_GND |
| RX_18 | 39 | 5 | RX_2 |
| ISO_GND | 38 | 4 | ISO_GND |
| RX_17 | 37 | 3 | RX_1 |
| ISO_GND | 36 | 2 | ISO_GND |
| RX_16 | 35 | 1 | RX_0 |



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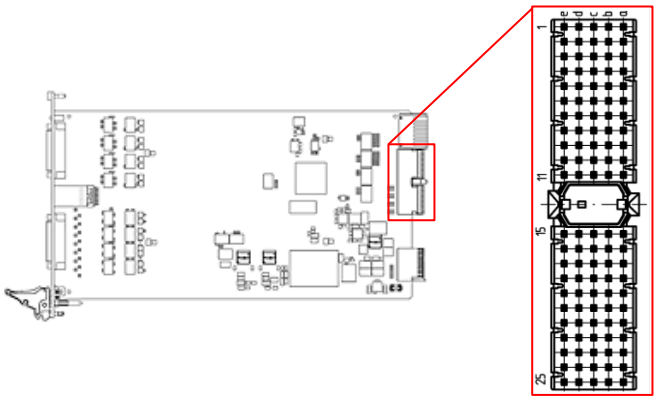
## BACKPLANE 110P XJ2 CONNECTOR PINOUT



| | e | d | c | b | a |
|---|---|---|---|---|---|
| 1 | OUT_3 | OUT_2 | N/C | OUT_1 | OUT_0 |
| 2 | OUT_7 | OUT_6 | N/C | OUT_5 | OUT_4 |
| 3 | GSE_GND | GSE_GND | GSE_GND | GSE_GND | GSE_GND |
| 4 | OUT_11 | OUT_10 | N/C | OUT_9 | OUT_8 |
| 5 | OUT_15 | OUT_14 | N/C | OUT_13 | OUT_12 |
| 6 | GSE_GND | GSE_GND | GSE_GND | GSE_GND | GSE_GND |
| 7 | OUT_19 | OUT_18 | N/C | OUT_17 | OUT_16 |
| 8 | OUT_23 | OUT_22 | N/C | OUT_21 | OUT_20 |
| 9 | GSE_GND | GSE_GND | GSE_GND | GSE_GND | GSE_GND |
| 10 | OUT_27 | OUT_26 | N/C | OUT_25 | OUT_24 |
| 11 | OUT_31 | OUT_30 | N/C | OUT_29 | OUT_28 |
| 12 | GSE_GND | GSE_GND | GSE_GND | GSE_GND | GSE_GND |
| 13 | N/C | N/C | N/C | N/C | N/C |
| 14 | N/C | N/C | N/C | N/C | N/C |
| 15 | IN_3 | IN_2 | N/C | IN_1 | IN_0 |
| 16 | IN_7 | IN_6 | N/C | IN_5 | IN_4 |
| 17 | GSE_GND | GSE_GND | GSE_GND | GSE_GND | GSE_GND |
| 18 | IN_11 | IN_10 | N/C | IN_9 | IN_8 |
| 19 | IN_15 | IN_14 | N/C | IN_13 | IN_12 |
| 20 | GSE_GND | GSE_GND | GSE_GND | GSE_GND | GSE_GND |
| 21 | IN_19 | IN_18 | N/C | IN_17 | IN_16 |
| 22 | IN_23 | IN_22 | N/C | IN_21 | IN_20 |
| 23 | GSE_GND | GSE_GND | GSE_GND | GSE_GND | GSE_GND |
| 24 | IN_27 | IN_26 | N/C | IN_25 | IN_24 |
| 25 | IN_31 | IN_30 | N/C | IN_29 | IN_28 |



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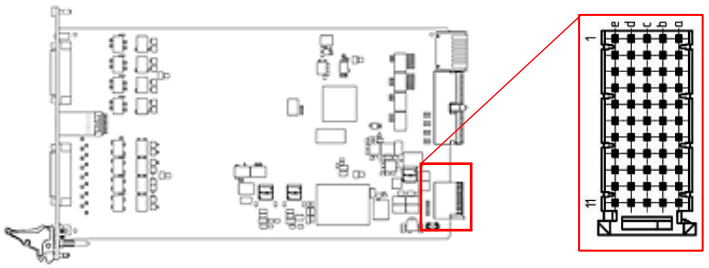
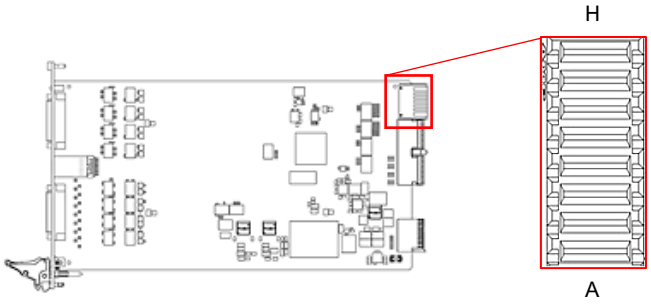
## BACKPLANE 55P XJ1 CONNECTOR PINOUT



| | e | d | c | b | a |
|---|---|---|---|---|---|
| 1 | N/C | N/C | N/C | N/C | N/C |
| 2 | N/C | N/C | N/C | N/C | N/C |
| 3 | N/C | N/C | N/C | N/C | N/C |
| 4 | N/C | N/C | N/C | N/C | N/C |
| 5 | N/C | N/C | N/C | N/C | N/C |
| 6 | N/C | N/C | N/C | N/C | N/C |
| 7 | GSE_GND | N/C | GSE_GND | N/C | GSE_GND |
| 8 | SLSC_SpiMOSI | GSE_GND | SLSC_SpiCLK | GSE_GND | SLSC_IntIn# |
| 9 | GSE_GND | SLSC_Trig_To_Mod | GSE_GND | SLSC_Trig_From_Mod | GSE_GND |
| 10 | N/C | GSE_GND | SLSC_SpiMISO | GSE_GND | SLSC_ED_SS# |
| 11 | 24 V | SLSC_Rdy/Rst# | 3.3 V | SLSC_ID_SS# | 24 V |

## BACKPLANE XJ3 CONNECTOR PINOUT




| | |
|---|---|
| H | ISO_GND |
| G | ISO_GND |
| F | EXT_CLK_IN |
| E | EXT_CLK_OUT |
| D | CHASSIS_GND |
| C | CHASSIS_GND |
| B | GSE_GND |
| A | GSE_GND |



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**PROPERTIES TABLE**
For use with NI SLSC VI package

| Signal Name | Description | Documentation | RW |
|---|---|---|---|
| BA.Isolated_Power_Supply_Switch | Output of the Isolated power supply | Lets you control the output of the Isolated power supply | RW |
| BA.DebugPort_Switch | Output of the Isolated power supply | Lets you control the output of the Isolated power supply | RW |
| BA.Discrete_Enable | Discrete Mode | Lets you control the Discrete Mode | RW |
| BA.Discrete_Inputs | Discrete Inputs | Read the Discrete Inputs | R |
| BA.Discrete_Outputs | Discrete Outputs | Read/Write the Discrete Outputs | RW |
| BA.ModuleControllerVersion | Module Controller Version | The version is the timestamp, in hexadecimal format, of the time the Module Controller was compiled | R |
| BA.Isolated_Power_Supply_Stage_2_Voltage | Isolated Power Supply Stage 2 Voltage | Reads Isolated power supply stage two's voltage | R |
| BA.Isolated_Power_Supply_Stage_2_Current | Isolated Power Supply Stage 2 Current | Reads Isolated power supply stage two's Current | R |
| BA.Isolated_Power_Supply_Stage_2_Temperature | Isolated Power Supply Stage 2 Temperature | Reads Isolated power supply stage two's temperature | R |
| BA.Isolated_Power_Supply_Stage_3_Voltage | Isolated Power Supply Stage 3 Voltage | Reads Isolated power supply stage three's voltage | R |
| BA.Isolated_Power_Supply_Stage_3_Current | Isolated Power Supply Stage 3 Current | Reads Isolated power supply stage three's Current | R |
| BA.Isolated_Power_Supply_Stage_3_Temperature | Isolated Power Supply Stage 3 Temperature | Reads Isolated power supply stage three's temperature | R |
| BA.SLSC_3p3_Voltage | Voltage of 3.3V line of SLSC Chassis | Reads the voltage of 3.3V line of SLSC Chassis | R |
| BA.SLSC_24V_Voltage | Voltage of 24V line of SLSC Chassis | Reads the voltage of 24V line of SLSC Chassis | R |
| BA.SLSC_24V_Current | Current of 24V line of SLSC Chassis | Reads the current of 24V line of SLSC Chassis | R |
| BA.GSE_3p3V_Voltage | Voltage of 3.3V line of GSE | Reads the voltage of 3.3V line of GSE | R |
| BA.GSE_3p3V_Current | Current of 3.3V line of GSE | Reads the current of 3.3V line of GSE | R |
| BA.GSE_1p5V_Voltage | Voltage of 1.5V line of GSE | Reads the voltage of 1.5V line of GSE | R |
| BA.GSE_1p5V_Current | Current of 1.5V line of GSE | Reads the current of 1.5V line of GSE | R |
| BA.GSE_Temperature_Sensor_1 | Temperature Sensor 1 | Reads the temperature reported by temperature sensor 1 | R |
| BA.GSE_Temperature_Sensor_2 | Temperature Sensor 2 | Reads the temperature reported by temperature sensor 2 | R |
| BA.GSE_Temperature_Sensor_3 | Temperature Sensor 3 | Reads the temperature reported by temperature sensor 3 | R |
| BA.GSE_Temperature_Sensor_4 | Temperature Sensor 4 | Reads the temperature reported by temperature sensor 4 | R |



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## REGISTER MAPPING TABLE

For developing custom SLSC drivers

| Signal Name | Addr (x16) | RW | Length | Reset Value | Bits | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| General Register | 0025 | RW | 8 | 0 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | | | X | X | X | Discrete Mode | Discrete Enable | X | DebugPort Switch | Isolated Power Supply Switch |
| iDis Register (Input State) | 0026 | R | 32 | | 31 | 30 | 29 | ... | ... | 2 | 1 | 0 |
| | | | | | Channel 31 | Channel 30 | Channel 29 | Channel n | Channel n | Channel 2 | Channel 1 | Channel 0 |
| oDis Register (Output State) | 0027 | RW | 32 | 0 | 31 | 30 | 29 | ... | ... | 2 | 1 | 0 |
| | | | | | Channel 31 | Channel 30 | Channel 29 | Channel n | Channel n | Channel 2 | Channel 1 | Channel 0 |
| oDis En Register (Discrete Enable) | 0028 | RW | 32 | 0 | 31 | 30 | 29 | ... | ... | 2 | 1 | 0 |
| | | | | | Channel 31 | Channel 30 | Channel 29 | Channel n | Channel n | Channel 2 | Channel 1 | Channel 0 |
| Miscellaneous | 0004 | RW | 8 | 0 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | | | X | X | X | X | X | X | X | Flash Write Protect |
| Version | 0000 | R | 32 | | 31 | 30 | 29 | ... | ... | 2 | 1 | 0 |
| | | | | | Timestamp | | | | | | | |
| Isolated Power Supply Stage_2 Voltage | 0015 | R | 32 | | 31 | 30 | 29 | ... | ... | 2 | 1 | 0 |
| | | | | | Voltage | | | | | | | |
| Isolated Power Supply Stage_2 Current | 001F | R | 32 | | 31 | 30 | 29 | ... | ... | 2 | 1 | 0 |
| | | | | | Current | | | | | | | |
| Isolated Power Supply Stage_2 Temperature | 001D | R | 32 | | 31 | 30 | 29 | ... | ... | 2 | 1 | 0 |
| | | | | | Temperature | | | | | | | |
| Isolated Power Supply Stage_3 Voltage | 001B | R | 32 | | 31 | 30 | 29 | ... | ... | 2 | 1 | 0 |
| | | | | | Voltage | | | | | | | |
| Isolated Power Supply Stage_3 Temperature | 0017 | R | 32 | | 31 | 30 | 29 | ... | ... | 2 | 1 | 0 |
| | | | | | Temperature | | | | | | | |
| Isolated Power Supply Stage_3 Current | 0019 | R | 32 | | 31 | 30 | 29 | ... | ... | 2 | 1 | 0 |
| | | | | | Current | | | | | | | |
| SLSC 24V Voltage | 0005 | R | 32 | | 31 | 30 | 29 | ... | ... | 2 | 1 | 0 |
| | | | | | Voltage | | | | | | | |
| SLSC 24V Current | 000D | R | 32 | | 31 | 30 | 29 | ... | ... | 2 | 1 | 0 |
| | | | | | Current | | | | | | | |
| SLSC 3p3V Voltage | 0007 | R | 32 | | 31 | 30 | 29 | ... | ... | 2 | 1 | 0 |
| | | | | | Voltage | | | | | | | |
| GSE 3p3V Voltage | 0009 | R | 32 | | 31 | 30 | 29 | ... | ... | 2 | 1 | 0 |
| | | | | | Voltage | | | | | | | |
| GSE 3p3V Current | 000E | R | 32 | | 31 | 30 | 29 | ... | ... | 2 | 1 | 0 |
| | | | | | Current | | | | | | | |
| GSE 1p5V Voltage | 000B | R | 32 | | 31 | 30 | 29 | ... | ... | 2 | 1 | 0 |
| | | | | | Voltage | | | | | | | |
| GSE 1p5V Current | 000F | R | 32 | | 31 | 30 | 29 | ... | ... | 2 | 1 | 0 |
| | | | | | Current | | | | | | | |
| GSE Temperature Sensor_1 | 0011 | R | 32 | | 31 | 30 | 29 | ... | ... | 2 | 1 | 0 |
| | | | | | Temperature | | | | | | | |
| GSE Temperature Sensor_2 | 0012 | R | 32 | | 31 | 30 | 29 | ... | ... | 2 | 1 | 0 |
| | | | | | Temperature | | | | | | | |
| GSE Temperature Sensor_3 | 0013 | R | 32 | | 31 | 30 | 29 | ... | ... | 2 | 1 | 0 |
| | | | | | Temperature | | | | | | | |
| GSE Temperature Sensor_4 | 0014 | R | 32 | | 31 | 30 | 29 | ... | ... | 2 | 1 | 0 |
| | | | | | Temperature | | | | | | | |



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## HOW TO ORDER

Table 1 shows the available configurations for immediate ordering.

**Table 1. Available Configurations for Ordering**

| PWA | Physical Protocol | Isolated Domain Voltage | Drive Series Resistance | Receiver Series Resistance | Receiver Pull-up Resistance | Receiver Pull-down Resistance | Ground Scheme |
|---|---|---|---|---|---|---|---|
| 200103-00 | LVTTL | 3.3 V | 25 Ω | 25 Ω | Open | Open | 2.2 MΩ II 100 nF |
| 200103-01 | Open Collector/Drain | 3.3 V | 100 Ω | 25 Ω | 10 kΩ | Open | 2.2 MΩ II 100 nF |
| 200103-02 | TTL | 5.0 V | 25 Ω | 25 Ω | Open | Open | 2.2 MΩ II 100 nF |
| 200103-03 | LVTTL / Open Drain | 3.3 V | 25 Ω | 25 Ω | Open | Open | 2.2 MΩ II 100 nF |
| 200103-XX | Customizable based on customer requests. | | | | | | |

For the customized Isolated Single-Ended Module (200103-XX), please provide the parameters below utilizing Table 2. A dash number will be associated with the requested configuration.

1) Physical Protocol
2) Isolated Domain Supply Voltage
3) Driver Series Resistance
4) Receiver Termination Resistance
5) Receiver Termination Capacitance
6) Receiver Series Resistance
7) Ground Scheme

**Table 2. Configurable Isolated Single-Ended Module Parameters for Ordering**

| Isolated Single-Ended Module | | | | | | | |
|---|---|---|---|---|---|---|---|
| PWA | Physical Protocol | Isolated Domain Voltage | Drive Series Resistance | Receiver Series Resistance | Receiver Pull-up Resistance | Receiver Pull-down Resistance | Ground Scheme |
| 200103 | LVTTL | 3.3 V | 0 Ω | 0 Ω | Open | Open | 2.2 MΩ ||100 nF All Legs |
| | TTL | 5.0 V | 25 Ω | 25 Ω | 1 kΩ | 1 kΩ | Open All Legs |
| | Open Collector / Drain | | 50 Ω | 50 Ω | 2 kΩ | 2 kΩ | 0 Ω Iso to Chassis,<br>2.2 MΩ \|\| 100 nF others |
| | LVCMOS | | 100 Ω | 100 Ω | 4.7 kΩ | 4.7 kΩ | 0 Ω GSE to Chassis,<br>2.2 MΩ \|\| 100 nF others |
| | CMOS | | 500 Ω | 500 Ω | 10 kΩ | 10 kΩ | 0 Ω Iso to GSE,<br>2.2 MΩ \|\| 100 nF others |
| | | | 1 kΩ | 1 kΩ | XX kΩ | XX kΩ | 0 Ω All Legs |
| | | | 2 kΩ | 2 kΩ | | | |
| | | | 4.7 kΩ | 4.7 kΩ | | | |
| | | | 10 kΩ | 10 kΩ | | | |



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