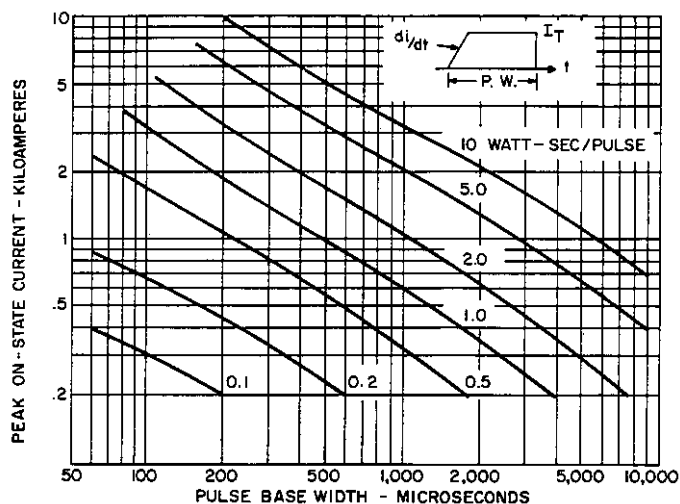


CHARACTERISTICS

TEST	SYMBOL	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
Peak Off-State and Reverse Currents	I_{DRM} and I_{RRM}	—	10	15	mA	$T_J = +25^\circ\text{C}$, $V = V_{DRM} = V_{RRM}$
Peak Off-State and Reverse Currents	I_{DRM} and I_{RRM}	—	45	60	mA	$T_J = +125^\circ\text{C}$, $V = V_{DRM} = V_{RRM}$
Effective Thermal Resistance Junction-to-Case, $R_{\theta JC}$	DC	—	—	.045	$^\circ\text{C}/\text{watt}$	Double-Side Cooled
Critical Linear Rate-of-Rise of Forward Blocking Voltage (Higher values may cause device switching)	dv/dt	200	—	—	$\text{V}/\mu\text{sec}$	$T_J = +125^\circ\text{C}$, $V_{DRM} = .80$ Rated, Gate Open ¹
Delay Time	t_d	—	1.5	3.0	μsec	Switching from 1000 Volts, 20 Volt, 10 Ohm Gate $0.5 \mu\text{sec}$ Rise Time, $T_J = 25^\circ\text{C}$
Gate Pulse Width Necessary to Trigger		—	—	10	μsec	See Figure 7.
Gate Trigger Current (See Figure 11)	I_{GT}	—	120	150	mA _{dc}	$T_C = 25^\circ\text{C}$, $V_D = 10 \text{ Vdc}$, $R_L = 3 \text{ Ohms}$
		5.0	30	—		$T_C = +125^\circ\text{C}$, $V_D = .5 \times \text{Rated}$, $R_L = 1000 \text{ Ohms}$
Gate Trigger Voltage (See Figure 11)	V_{GT}	—	3.0	5.0	V _{dc}	$T_C = 25^\circ\text{C}$, $V_D = 10 \text{ Vdc}$, $R_L = 3 \text{ Ohms}$
		.3	—	—		$T_C = 125^\circ\text{C}$, $V_D = .5 \times \text{Rated}$, $R_L = 1000 \text{ Ohms}$
Peak On-State Voltage	V_{TM}	—	—	2.21	Volts	$T_C = +125^\circ\text{C}$, $I_T = 2000 \text{ Amps}$. Peak Duty Cycle $\leq 0.01\%$
Conventional Circuit Commutated Turn-Off Time ⁽¹⁾ (With Reverse Voltage)	t_q —	—	55	60	μsec	(1) $T_C = +125^\circ\text{C}$ (2) $I_T = 500 \text{ Amps}$. (3) $V_R \geq 50 \text{ Volts}$ (4) Rate-of-Rise of Forward Blocking Voltage = $200 \text{ V}/\mu\text{sec}$ to 80% of V_{DRM} or $400 \text{ V}/\mu\text{sec}$ to 70% of V_{DRM} (5) Gate Bias = Open During Turn-Off Interval = 0 Volts , 100 Ohms (6) Duty Cycle $\leq 0.01\%$
Conventional Circuit Commutated Turn-Off Time ⁽¹⁾ (With Feedback Diode)	t_q	—	60	65	μsec	(1) $T_C = +125^\circ\text{C}$ (2) $I_T = 500 \text{ Amps}$. (3) $V_R = 5 \text{ Volts Min.}$ (4) Rate-of-Rise of Forward Blocking Voltage = $400 \text{ V}/\mu\text{sec}$ to 70% of V_{DRM} (5) Gate Bias = Open During Turn-Off Interval (6) Duty Cycle $\leq 0.01\%$

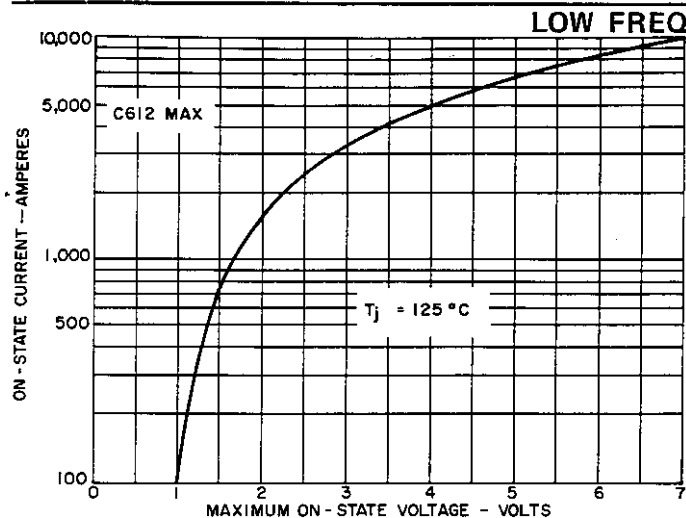
(1) Turn-off times are measured on a go/no-go basis using LEM test equipment. Experimental determination of critical t_q may lead to device degradation.



6. ENERGY PER PULSE FOR TRAPEZOIDAL
CURRENT WAVEFORMS FOR
100 A/ μ SEC RISING DI/DT

NOTES:

1. Switching voltage range: $V_D = 15V - 0.8 V_{DRM}$.
2. Peak snubber discharge current $\leq 50A$. $RC \leq 10\mu sec$.
3. High gate drive: 20V/10 Ohms, 0.5 μsec . rise time.
4. Reverse voltage $\leq 50V$.

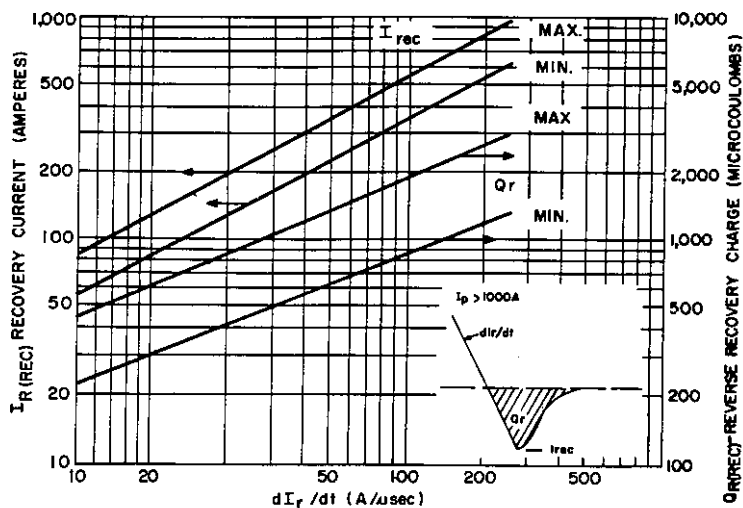


7. FORWARD CONDUCTION
CHARACTERISTIC ON-STATE

VOLTAGE (Volts) CURRENT (Amps)

NOTES:

1.040	100
1.153	200
1.232	300
1.300	400
1.363	500
1.422	600
1.480	700
1.537	800
1.594	900
1.650	1000
1.706	1100
1.762	1200
1.818	1300
1.873	1400
1.929	1500
2.210	2000
2.781	3000
3.363	4000
3.954	5000
4.552	6000
5.157	7000
5.767	8000
6.382	9000
7.000	10000

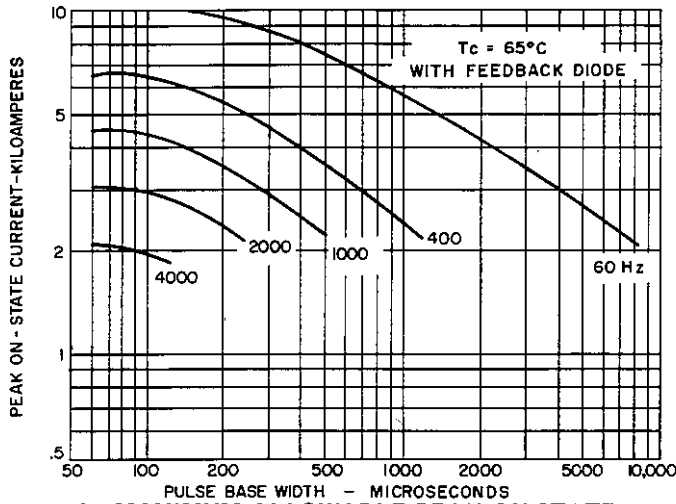


8. REVERSE RECOVERY CHARACTERISTICS
(125°C)

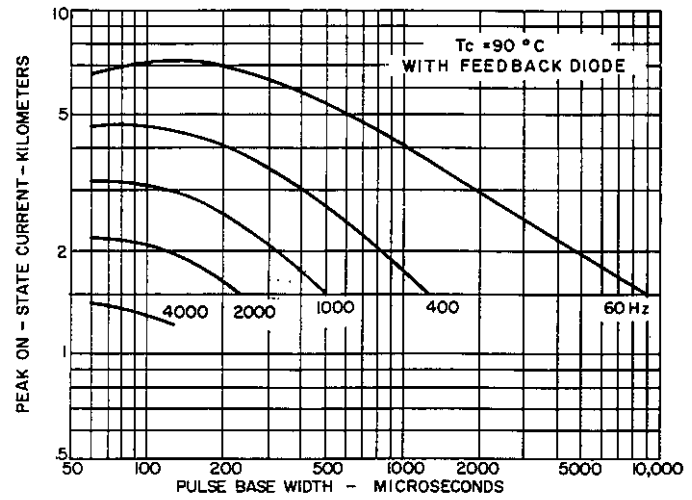
NOTES:

Curves are based upon production tests of I_{rec} . Q_r is a close approximation based upon calculation using appropriate value of I_{rec} and an empirical formula.

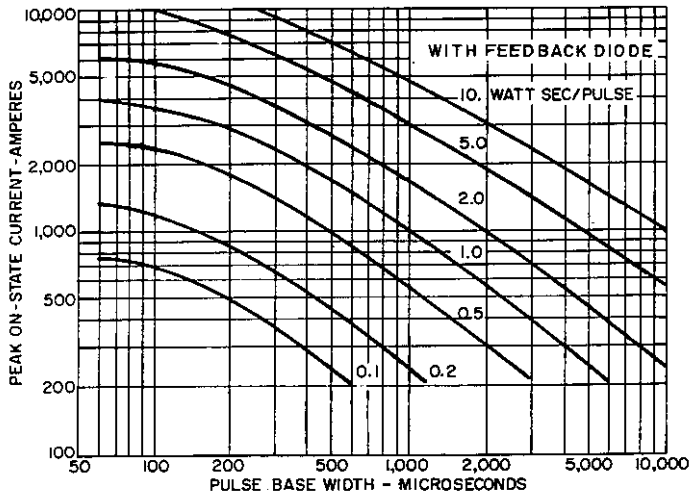
SINE WAVE DATA



1. MAXIMUM ALLOWABLE PEAK ON-STATE CURRENT VS. PULSE WIDTH ($T_c = 65^\circ\text{C}$)



2. MAXIMUM ALLOWABLE PEAK ON-STATE CURRENT VS. PULSE WIDTH ($T_c = 90^\circ\text{C}$)

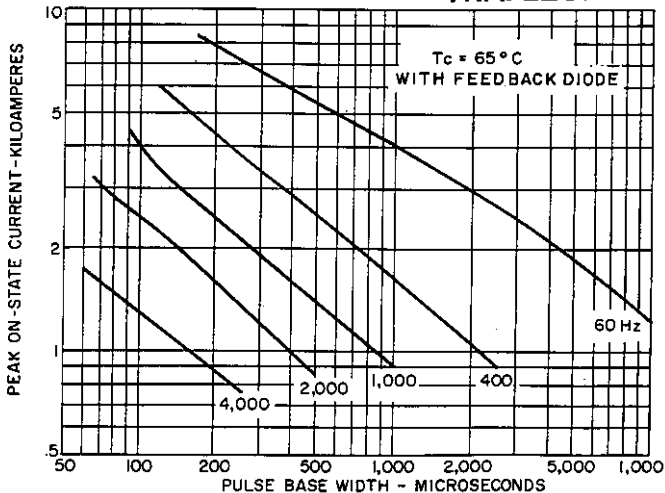


3. ENERGY PER PULSE FOR SINUSOIDAL PULSES

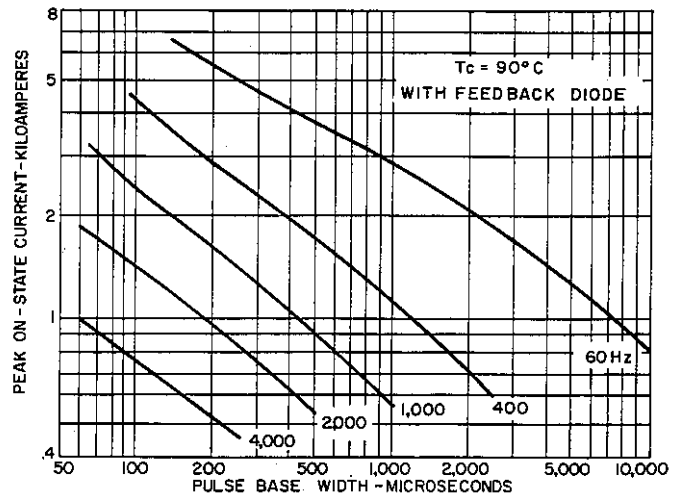
NOTES:

1. Switching voltage range: $V_D = 15\text{V} - 0.8 V_{\text{DRM}}$.
2. Peak snubber discharge current $\leq 50\text{A}$, $RC \leq 10\mu\text{sec}$.
3. High gate drive: $20\text{V}/10\text{ Ohms}$, $0.5\mu\text{sec}$ rise time.
4. Reverse voltage $< 50\text{V}$. If no bypass diode is used, recovery switching losses must be added.

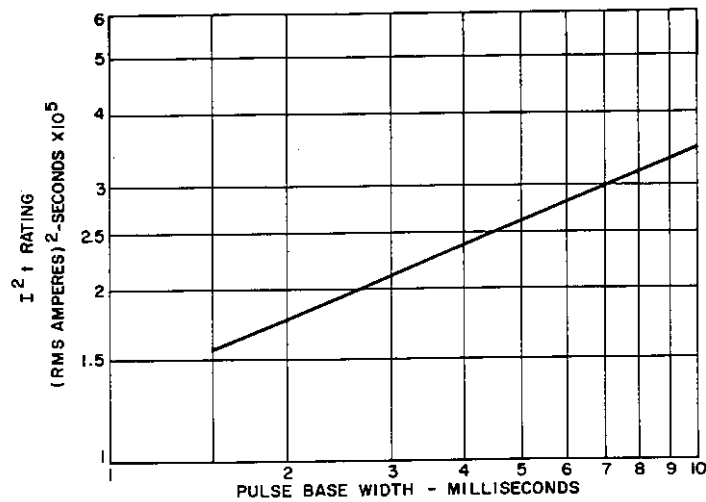
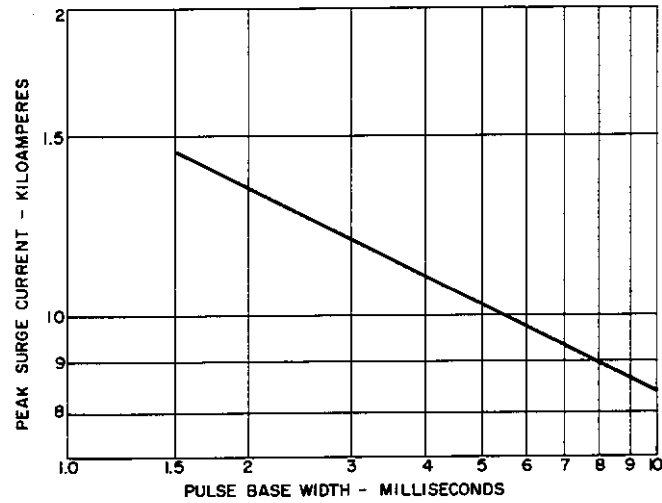
TRAPEZOIDAL WAVEFORM DATA



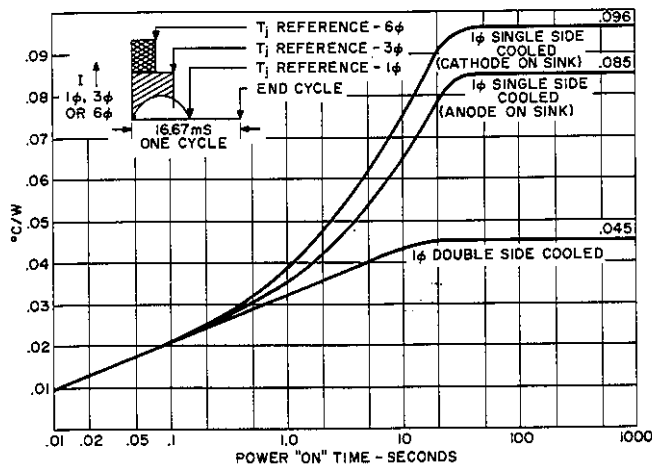
4. MAXIMUM ALLOWABLE PEAK ON-STATE CURRENT FOR RISING $DI/DT = 100\text{ A}/\mu\text{SEC}$ ($T_c = 65^\circ\text{C}$)



5. MAXIMUM ALLOWABLE PEAK ON-STATE CURRENT FOR RISING $DI/DT = 100\text{ A}/\mu\text{SEC}$ ($T_c = 90^\circ\text{C}$)



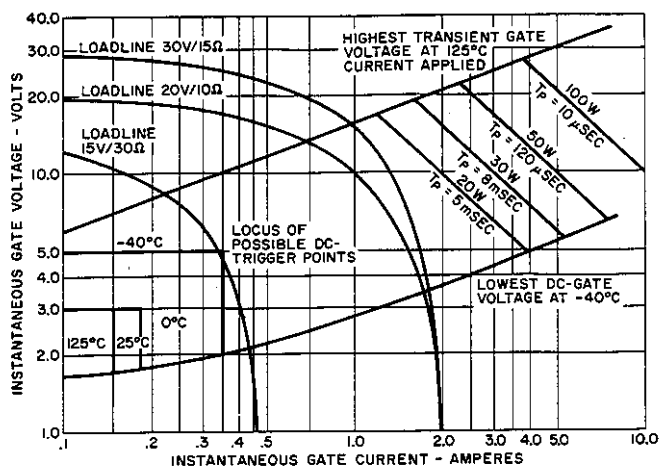
9. SUB-CYCLE SURGE AND I^2t RATING FOLLOWING RATED LOAD CONDITIONS (Sinusoidal Waveform)



NOTES:

- For 3 ϕ thermal resistance add .0037°C/W along entire curve length.
- For 6 ϕ thermal resistance add .001°C/W along entire curve length.
- For DC thermal resistance subtract .005°C/W along entire curve length.

10. TRANSIENT THERMAL IMPEDANCE - JUNCTION-TO-CASE



NOTES:

1. Maximum allowable gate dissipation = 3 watts.
2. The locus of possible DC-trigger points lies outside the boundaries shown at various junction temperatures.
3. Loadlines 30V/15 Ω , 20V/10 Ω and similar are recommended as minimum gate drives for most inverter application: rise time $\leq 0.5 \mu\text{sec}$; $T_p \geq 10 \mu\text{sec}$.
4. Loadline 15V/30 Ω is the minimum usable gate drive. Snubber resistances must be $> 30 \Omega$ when turning on from $\geq 800\text{V}$ bias. Delay-time may be increased. di/dt rating $\leq 100\text{A}/\mu\text{sec}$.

**11. MAXIMUM ALLOWABLE PEAK GATE POWER
VS. GATE PULSE WIDTH**