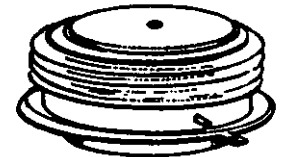


## Operation to 3 kHz



The C712 Reverse Blocking Thyristor has proven performance in forced commutation circuits operating to 3KHZ. It is recommended for use with an anti-parallel soft recovery diode as utilized in most PWM inverters.

The C712 internal gate structure has an involute, interdigitated gate pattern needed to enhance the initially turned on area for high di/dt capability.



THYRISTOR (SCR) PRESSPAK

### FEATURES:

- o Proven mature design.
- o Low switching loss at high frequency.
- o 60 us maximum turn-off time with feedback diode.
- o Involute, interdigitate gate.
- o Narrow pulse capability for PWM inverter commutation socket.

### MAXIMUM ALLOWABLE RATINGS

| TYPE   | $V_{DRM}/V_{RRM}^1$<br>REPETITIVE<br>$T_J = -40^\circ\text{C to } +125^\circ\text{C}$ | $V_{DRM}/V_{RRM}^1$<br>REPETITIVE<br>$T_J = 0^\circ\text{C to } +125^\circ\text{C}$ | TRANSIENT PEAK REVERSE<br>VOLTAGE, $V_{RSM}^1$<br>$T_J = -40^\circ\text{C to } +125^\circ\text{C}$ |
|--------|---------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------|
| C712L  | 2000 Volts                                                                            | 2100 Volts                                                                          | 2100 Volts                                                                                         |
| C712PT | 1900                                                                                  | 2000                                                                                | 2000                                                                                               |
| C712PN | 1800                                                                                  | 1900                                                                                | 1900                                                                                               |
| C712PS | 1700                                                                                  | 1800                                                                                | 1800                                                                                               |
| C712PM | 1600                                                                                  | 1700                                                                                | 1700                                                                                               |
| C712PE | 1500                                                                                  | 1600                                                                                | 1600                                                                                               |

Consult factory for lower rated voltage devices.

|                                                                                    |                                                 |
|------------------------------------------------------------------------------------|-------------------------------------------------|
| Peak One-Cycle Surge On-State Current, $I_{TSM}$ (8.3 msec)                        | 20,000 Amperes                                  |
| Maximum Rate-of-Rise of Anode Current Turn-On Interval (Switching From 1200 Volts) | 800 A/ $\mu\text{sec}$                          |
| Repetitive di/dt Rating <sup>2</sup>                                               | 200 A/ $\mu\text{sec}$                          |
| $I^2t$ (for fusing) (at 8.3 milliseconds)                                          | 1,660,000 Ampere <sup>2</sup> Seconds           |
| Peak Gate Power Dissipation, $P_{GM}$                                              | 100 Watts                                       |
| Average Gate Power Dissipation, $P_{G(AV)}$                                        | 5 Watts                                         |
| Peak Reverse Gate Voltage, $V_{GRM}$                                               | 20 Volts                                        |
| Storage and Operating Temperature, $T_{STG}$ and $T_J$                             | Refer Above                                     |
| Mounting Force Required                                                            | 5000 Lb. + 1000 - 0 Lb.<br>22.2 KN + 4.4 - 0 KN |

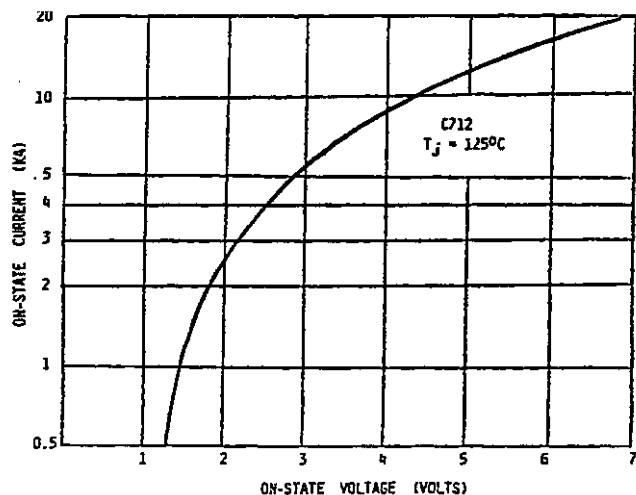
### NOTES:

<sup>1</sup> 10 msec voltage sinewave.

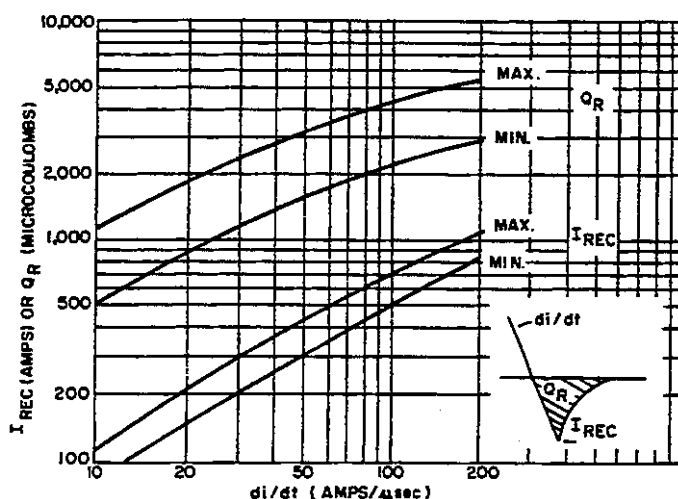
<sup>2</sup> di/dt rating established in accordance with EIA-NEMA Standard RS-397, Section 5.2.2. This di/dt is in addition to the discharge of a 0.25  $\mu\text{f}$ , 20 ohm snubber circuit in parallel with the DUT.

## CHARACTERISTICS

| TEST                                                                                                | SYMBOL                  | MIN. | TYP. | MAX. | UNITS                    | TEST CONDITIONS                                                                                                                                                                                                                                                                                                |
|-----------------------------------------------------------------------------------------------------|-------------------------|------|------|------|--------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Peak Reverse and On-State Blocking Current                                                          | $I_{DRM}$ and $I_{RRM}$ | —    | 20   | 60   | mA                       | $T_J = +125^\circ\text{C}$ , $V = V_{DRM} = V_{RRM}$                                                                                                                                                                                                                                                           |
| Effective Thermal Resistance, Junction-to-Case                                                      | $R_{\theta JC}$         | —    | —    | .023 | $^\circ\text{C/Watt}$    | Double-Side Cooled (DC)                                                                                                                                                                                                                                                                                        |
| Critical Linear Rate-of-Rise of Forward Blocking Voltage (Higher values may cause device switching) | $dv/dt$                 | 500  | —    | —    | $\text{V}/\mu\text{sec}$ | $T_J = +125^\circ\text{C}$ , $V_{DRM} = .80$ Rated $V_{RRM}$<br>Gate Open.                                                                                                                                                                                                                                     |
| Delay Time                                                                                          | $t_d$                   | —    | 1.5  | —    | $\mu\text{sec}$          | Switching from 140 Volts, 20 Volt, 10 Ohm<br>Gate: $0.5 \mu\text{sec}$ Rise Time, $T_J = 25^\circ\text{C}$                                                                                                                                                                                                     |
| Gate Pulse Width Necessary To Trigger                                                               |                         | —    | —    | 10   | $\mu\text{sec}$          | $T_J = 25^\circ\text{C}$                                                                                                                                                                                                                                                                                       |
| Gate Trigger Current (not for operational use)                                                      | $I_{GT}$                | —    | 120  | —    | mA dc                    | $T_C = 25^\circ\text{C}$ , $V_D = 10 \text{ Vdc}$ , $R_L = 3 \text{ Ohms}$                                                                                                                                                                                                                                     |
|                                                                                                     |                         | 5.0  | 30   | —    |                          | $T_C = +125^\circ\text{C}$ , $V_D = .5 \times \text{Rated}$ , $R_L = 1000 \text{ Ohms}$                                                                                                                                                                                                                        |
| Gate Trigger Voltage (not for operational use)                                                      | $V_{GT}$                | —    | 3.0  | —    | Vdc                      | $T_C = 0^\circ\text{C}$ to $+125^\circ\text{C}$ , $V_D = 10 \text{ Vdc}$ , $R_L = 3 \text{ Ohms}$                                                                                                                                                                                                              |
| Peak On-State Voltage                                                                               | $V_{TM}$                | —    | —    | 1.45 | Volts                    | $T_C = +125^\circ\text{C}$ , $I_T = 1000 \text{ Amps}$ . Peak<br>Duty Cycle $\leq 0.01\%$                                                                                                                                                                                                                      |
| Conventional Circuit Commutated Turn-Off Time (With Reverse Voltage)                                | $t_q$                   | —    | —    | 55   | $\mu\text{sec}$          | (1) $T_C = +125^\circ\text{C}$<br>(2) $I_T = 1000\text{A}$<br>(3) $V_R \geq 50 \text{ Volts}$<br>(4) $80\% V_{DRM}$ Reapplied<br>(5) Rate-of-Rise of Forward Blocking Voltage = $400\text{V}/\mu\text{s}$<br>(6) Gate Bias = Open During Turn-Off Interval = 0 Volts, 100 Ohms<br>(7) Duty Cycle $\leq 0.01\%$ |
| Conventional Circuit Commutated Turn-Off Time (With Feedback Diode)                                 | $t_q$                   | —    | 55   | 60   | $\mu\text{sec}$          | (1) $T_C = +125^\circ\text{C}$<br>(2) $I_T = 1000\text{A}$<br>(3) $V_R = 2 \text{ Volts Min.}$<br>(4) $80\% V_{DRM}$ Reapplied<br>(5) Rate-of-Rise of Forward Blocking Voltage = $400\text{V}/\mu\text{s}$<br>(6) Gate Bias = Open During Turn-Off Interval<br>(7) Duty Cycle $\leq 0.01\%$                    |

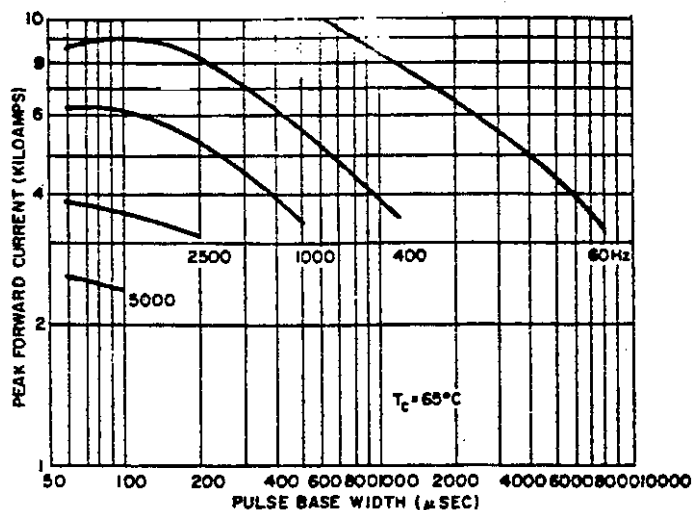


FORWARD CONDUCTION CHARACTERISTIC  
ON-STATE

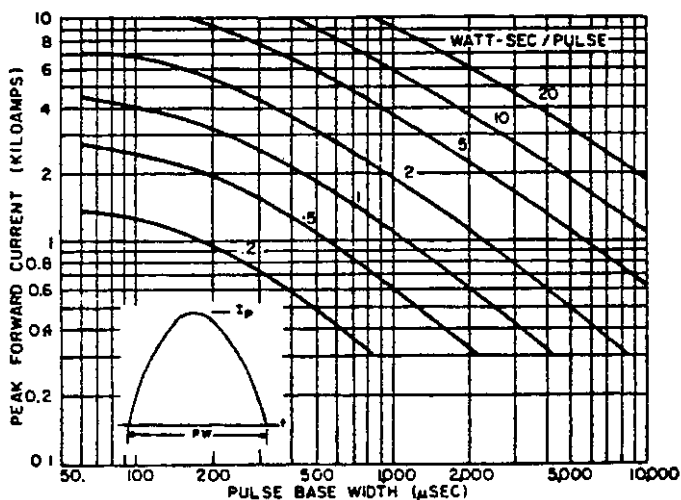


RECOVERED CHARGE (125°C)

## SINUSOIDAL CURRENT WAVEFORMS

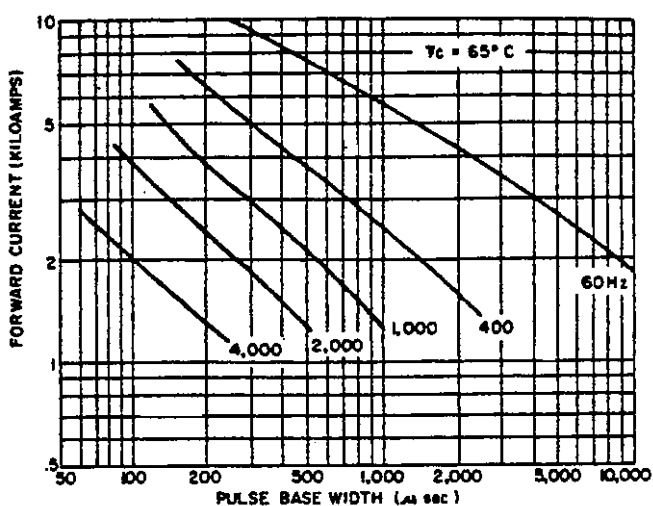


MAXIMUM ALLOWABLE PEAK ON-STATE CURRENT VS. PULSE WIDTH ( $T_c = 65^\circ\text{C}$ )

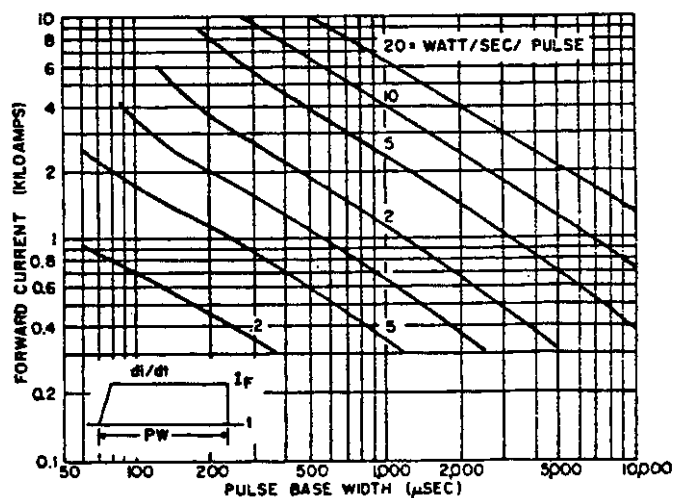


ENERGY PER PULSE FOR SINUSOIDAL PULSES

## TRAPEZOIDAL CURRENT WAVEFORMS



MAXIMUM ALLOWABLE PEAK ON-STATE CURRENT FOR TRAPEZOIDAL CURRENT WAVEFORMS FOR ( $T_c = 65^\circ\text{C}$ ) ( $di/dt = 100\text{A/us}$ )



ENERGY PER PULSE FOR TRAPEZOIDAL CURRENT WAVEFORMS

| $\frac{di_R}{dt}$ (A/us) | $\frac{dv_R}{dt}$ (V/us) |      |      |      |      |
|--------------------------|--------------------------|------|------|------|------|
|                          | 100                      | 300  | 500  | 700  | 1000 |
| 10                       | .166                     | .481 | .654 | .743 | .816 |
| 30                       | .167                     | .501 | .774 | .935 | 1.07 |
| 50                       | .168                     | .503 | .812 | 1.02 | 1.2  |
| 70                       | .168                     | .504 | .829 | 1.07 | 1.29 |
| 100                      | .168                     | .505 | .839 | 1.11 | 1.37 |
| 300                      | .169                     | .508 | .846 | 1.18 | 1.60 |

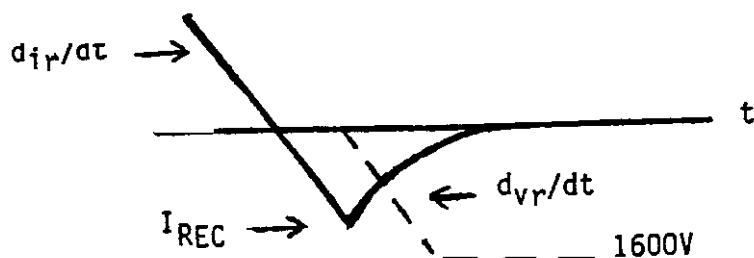
MAXIMUM RECOVERY ENERGY (JOULES)

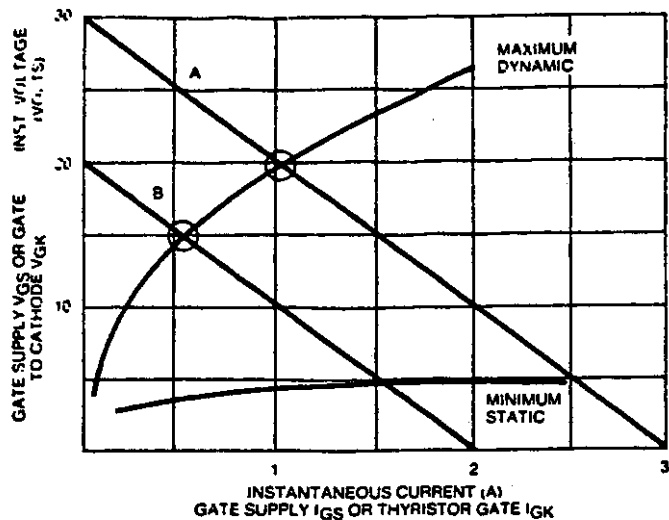
NOTES: 1- On-state ratings and energies do not include reverse recovery as a bypass diode is anticipated. A snubber discharge of 50A is included.

2- If no bypass diode is used with this thyristor, the additional switching energy can be significant. Refer to the table on the left.

3- The full cycle average power dissipation is the sum of the on-state and recovery energies times the operating frequency, accordingly

$$P_{AV} = (S_F + S_R) \cdot f$$





#### THYRISTOR GATE IMPEDANCE

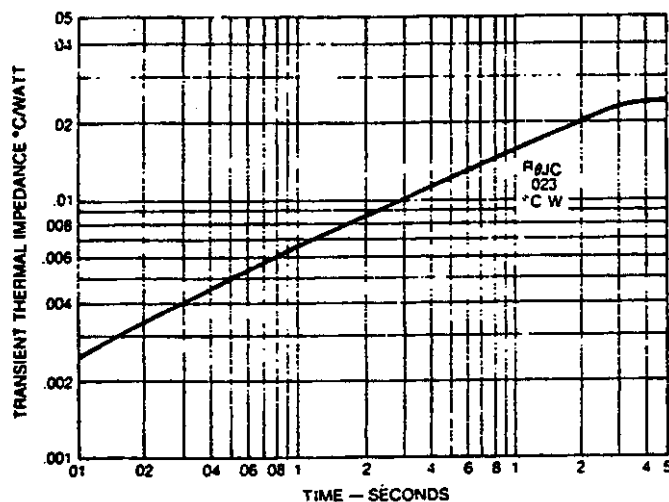
...This is enhanced by fast rising gate voltage, increasing anode bias and temperature.  
 ...It is shown at a minimum for dc voltage, zero bias and low temperature.  
 ...It is shown at a maximum for operating bias and recommended gate drive.

#### GATE SUPPLY

...Load lines (A) and (B) are operational, however, (A) is recommended to achieve maximum life at full di/dt rating and snubber discharge. The short circuit current rise time should be approximately 0.5us and the duration longer than the expected delay time.

#### MINIMUM ACCEPTABLE GATE CURRENT

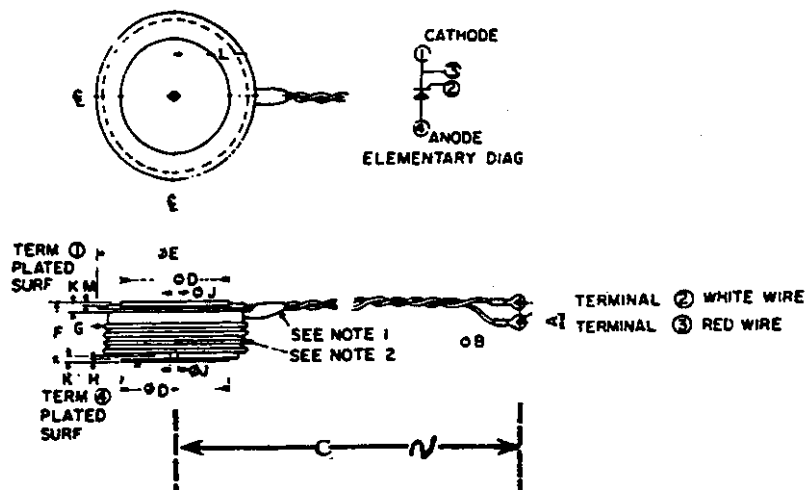
...The intersection of the load line and the gate characteristic (encircled) indicates the desired value of gate current needed to flow into the thyristor.



#### NOTES:

1. Add .006°C W to account for both case to dissipator interfaces when properly mounted: e.g.,  $R_{\theta JS} = .029^\circ\text{C W}$ . See Mounting Instructions.
2. DC Thermal Impedance is based on average full cycle junction temperature. Instantaneous junction temperature may be calculated using the following modifications:
  - end of conducting portion of cycle
    - 120° sq. wave add .0025°C W along entire curve
    - 180° sq. wave add .0018°C W along entire curve
    - 180° sine wave add .0010°C W along entire curve
  - end of cycle
    - any wave, subtract .001°C along entire curve.
3. Ask for general mounting instructions.

#### OUTLINE DRAWING



4. Anode-Cathode Pole Faces ① ① Nickel Plated Copper.
5. Mating Surface Requirement TIR  $\leq .0005$  inch Finish 32.
6. Mounting Force, 5000-6000 Lb., 22.4-26.7 KN.
7. Electrical Insulation, Glazed Ceramic, Creepage 1 in. (25.4mm). Strike  $\frac{1}{8}$  in. (15.9mm)
8. Gate Leads ② ③ 18 in. #22 Terminated with #8 Ring Terminal, Cathode Wire-Red, Gate Wire-White.

| Symbol   | Inches |        | Millimeters |        | Notes |
|----------|--------|--------|-------------|--------|-------|
|          | Min.   | Max.   | Min.        | Max.   |       |
| A        | 0.200  | 0.240  | 5.08        | 6.10   | 1     |
| $\phi B$ | 0.140  | —      | 3.56        | —      |       |
| C        | 16.000 | 20.000 | 406.40      | 508.00 |       |
| $\phi D$ | 1.700  | 1.900  | 43.18       | 48.26  |       |
| $\phi E$ | —      | 2.960  | —           | 75.18  |       |
| F        | 1.000  | 1.070  | 25.40       | 27.18  |       |
| G        | —      | —      | —           | —      | 2     |
| H        | .005   | .067   | 0.13        | 1.70   |       |
| $\phi J$ | 0.136  | 0.146  | 3.45        | 3.71   |       |
| K        | .070   | .100   | 1.78        | 2.54   |       |
| L        | —      | 2.500  | —           | 63.50  |       |
| M        | .030   | —      | 0.76        | —      |       |

#### NOTES:

1. Contour and orientation of term lugs is undefined.
2. Glazed ceramic insulator with 1.00 inch (25.40 mm) surface creepage, min.