# CFP MSA Management Interface Specification

100/40 Gigabit Transceiver Package Multi-Source Agreement

**Version 1.4**

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# 1 REVISION HISTORY

| *Revision* | *Date* | *Objective* | *By* |
|---|---|---|---|
| *External NDA Draft 0.1* | *12/23/2008* | *Initial release, work in progress* | *Jiashu Chen* |
| *External NDA Draft 0.2* | *01/26/2009* | *2nd release for review* | *Jiashu Chen* |
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| *Publication Draft 1.0* | *04/13/2009* | *First full draft for releasing to public.* | *Jiashu Chen* |
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| *Publication Version 1.4 (r5)* | *6/22/2010* | *Publication release* | *Jiashu Chen* |

# REFERENCES

1. IEEE Standard 802.3-2008
2. IEEE Standard P802.3ba, Draft 2.0
3. INF-8074i, XENPAK MSA Issue 3.0
4. INF-8077i, XFP Specification Rev. 4.5
5. CFP MSA Hardware Specification Draft 1.4

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# 1 DOCUMENT SUMMARY

## 1.1 Background

This technical document, CFP MSA Management Interface Specification, has been created by the CFP MSA group as a basis for a technical agreement between CFP module users and vendors, together with its companion document *CFP MSA Hardware Specification*.

This document is not a warranted document. Each CFP module supplier will have their own datasheet. If the users wish to find a warranted document, they should consult the datasheet of the chosen module vendor.

The CFP MSA group reserves the rights at any time to add, amend, or withdraw technical data contained in this document.

## 1.2 CFP Management Interface

*CFP MSA Hardware Specification* specifies the use of Management Data Input/Output (MDIO) as the management interface between a Host and a CFP module. While the hardware specification defines the hardware aspects of the MDIO interface such as its electrical characteristics and timing requirements, this document defines a set of MDIO registers suitable for CFP module applications following MDIO interface definition in IEEE 802.3 Clause 45.

## 1.3 Content of this document

Section 1 is the summary of this document. Section 2 provides an overview of the CFP management interface, including a sample block diagram, MDIO command frame, and the CFP register set. Section 3 layouts the overview of the CFP register set. Section 4 presents detailed discussions of the Host/Module control and signaling theory. Finally Section 5 gives a series of tables describing the details of all CFP registers.

## 1.4 Notations

### 1.4.1 Hardware Signal Name

Signals transmitted over CFP module connector pins are considered as hardware signals. Hardware signals names are directly quoted from the CFP MSA Hardware Specification, formed with all upper case letters and numbers with the exception of a lower case letter as the post script for some cases. Examples are MOD_LOPWR and MOD_RSTn.

### 1.4.2 Soft (MDIO) Signal Name

Signals transmitted over CFP Management Interface are considered as “Soft” signals or MDIO signals. They are represented by CFP Registers or register bits. Soft signals have their names denoted by one or more words or acronyms connected with or without underscores. If the name consists of multiple words each word shall have its first character

capitalized. Examples are Soft GLB_ALRM Test, Soft Module Reset, etc. Some Soft signals used as the defaults for programmable hardware pins are denoted in the manner of Hardware Signal names, such as GLB_ALRM, HIPWR_ON, and MOD_READY.

### 1.4.3 CFP Register Name and Address

The names of CFP registers are formed with one or more English words, with each word's first character capitalized and space in between. Each register address is a 16-bit hex number. When a particular bit in a register is addressed its address is denoted by x.y where the x is the register address and y is the bit address, a decimal number ranging from 0 to 15. When several bits in a register are addressed the address format is x.y~z, where y and z are boundary bits. The sign "~" is used to represent all the bits in between.

### 1.4.4 Numbers

Hex numbers are post-fixed by a lower case letter "h", for example, A000h. Binary numbers are post-fixed by a lower case letter such as 11b and 1101b. Decimal numbers have neither prefix nor postfix. With this notation, an example of bit 15 at register A001 (hex) has the format of A001h.15.

### 1.4.5 Special Characters

Whenever possible, the special characters are avoided. For example, the symbol of micrometer is designated as "um" or micro-meter instead of "μm" to prevent format loss in the editing process.

## 1.5 Glossary

The often used nomenclatures in this document are listed in the following glossary table for reference.

*Table 1 Glossary*

| Terminology | Description |
|---|---|
| APD | Avalanche Photodiode |
| BOL | Beginning Of Life |
| IEEE 802.3 | IEEE Standard 802.3-2008 |
| CFP MSA Specifications | CFP MSA Specifications define a hot-pluggable optical transceiver form factor to enable 40Gbps and 100Gbps applications, including next-generation High Speed Ethernet (40GbE and 100GbE).<br><br>CFP MSA Specifications consist of two major documents: CFP MSA Hardware Specification and CFP MSA Management Interface Specification (this document). |
| CFP module | A transceiver compliant to CFP MSA. The term "module" refers to CFP module unless otherwise specified. |
| CFP register(s) | A CFP register collects certain related management information in a basic form of a 16-bit word, occupying one MDIO register address. The term "register" |

| Terminology | Description |
|---|---|
| | refers to CFP register unless otherwise specified. |
| CMU | Clock Multiplier Circuit. |
| Control | It refers to the Host control functions to the module over Management Interface. It also includes the support of programmable control pin logic. |
| DDM | Digital Diagnostic Monitoring. It includes CFP module functions of A/D value reporting, FAWS logic, and programmable alarm pin logic. |
| FAWS | Fault, Alarm, Warning, and Status. |
| GLB_ALRM | It is a CFP module internally generated signal that drives GLB_ALRMn pin. |
| GLB_ALRMn | Global alarm hardware signal pin defined in CFP MSA Hardware Specification. |
| HIPWR_ON | High power mode of module operation. |
| Host | It is equivalent to Station Management Entity (STA) of IEEE 802.3. It sources MDC (MDIO Clock). |
| Host Lane | It refers to high speed data lane between a Host and a CFP module. |
| HW_Interlock | It is a logic signal CFP module generates internally based on Hardware Interlock [Reference 5]. It is defined as follows:<br>1 if CFP module power dissipation/consumption is greater than the Host cooling capacity<br>0 if CFP module power dissipation/consumption is equal or less than the Host cooling capacity or if Hardware Interlock is not used. |
| MOD_LOPWR | Hardware signal driving CFP module into Low-Power State. Reference CFP MSA Hardware Specification Rev. 1.4 for details. |
| MOD_LOPWRs | Combined Module Low Power Signal. Refer to Section 4.1.1.2. |
| MOD_RSTn | Hardware signal driving CFP module into Reset State. Reference CFP MSA Hardware Specification Rev. 1.4 for details. |
| MOD_RSTs | Combined Module Reset Signal. Refer to Section 4.1.1.1. |
| Network Lane | It refers to data lane between CFP module and network, say, optical network. |
| NVM | Non-Volatile Memory |
| NVR | Non-Volatile Register |
| PMD | Physical Medium Dependent |
| Signal | Information represented by hardware pins or CFP register bits and/or transmitted over the management interface or hardware connector. |
| SOA | Solid-State Optical Amplifier |
| TX_DIS | Refer to [Reference 5] for description. |
| TX_DISs | Combined Transmitter Disable Signal. Refer to Section 4.1.1.3. |
| User | The customer of CFP module. |
| Vendor | The manufacturer of CFP module. |
| VR | Volatile Register |

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# 2 CFP MANAGEMENT INTERFACE

## 2.1 Overview

CFP Management Interface is the main communication interface between a Host and a CFP module. Host uses this interface to control and monitor the startup, shutdown, and normal operation of the CFP modules it manages. This interface operates over a set of hardware pins through the CFP module connector and a set of software based protocols.

The primary protocol of CFP Management Interface is specified using MDIO bus structure following the general specification of IEEE 802.3 Clause 45 and on-going IEEE 802.3 40GbE and 100GbE standardization project.

From a hardware point of view, CFP Management Interface consists of following 8 hardware signals: 2 hardware signals of MDC and MDIO, 5 hardware signals of Port Address, and 1 hardware signal GLB_ALRMn. MDC is the MDIO Clock line driven by the Host and MDIO is the bi-directional data line driven by both the Host and module depending upon the data directions. The CFP Management Interface uses these hardware signals in the electrical connector to instantiate the MDIO interface, listed in Table 2.1 MDIO Interface Pins, in *CFP MSA Hardware Specification*.

From a software/protocol point of view, CFP Management Interface consists of the MDIO management frame, a set of CFP registers, and a set of rules for host control, module initialization, and signal exchange between these two. To avoid the conflict with IEEE 802.3, CFP register set does not use the addresses from 0000h to 7FFFh at the present time. The CFP registers use the addresses from 8000h to FFFFh, totaling 32768 addresses.

## 2.2 Specifications

With compliance to IEEE 802.3 Clause 45, CFP MSA defines the following additional specifications for CFP MDIO interface.

a) Support of MDC rate up to 4 MHz while maintaining the downward compatibility to 100 kHz.
b) Both read and write activities occurring on the rising edge of the MDC clock only.
c) Supports MDIO Device Address 1 only, among 32 available addresses.

### 2.2.1 Optional Features

This specification provides a number of optional features. Compliance with this specification does not require the implementation of these optional features by the module supplier. All such optional features shall be clearly identified as "Optional" in the corresponding register and bit definitions as well as the related text.

#### 2.2.1.1 Optional Controls

The module supplier shall explicitly indicate the presence (or absence) of each optional control in the Module Enhanced Options registers in NVR register space. This allows the host to dynamically determine feature availability on a module-by-module basis.

#### 2.2.1.2 Optional FAWS signals

Optional FAWS register bits do not require identification in Module Enhanced Options registers in NVR register space.

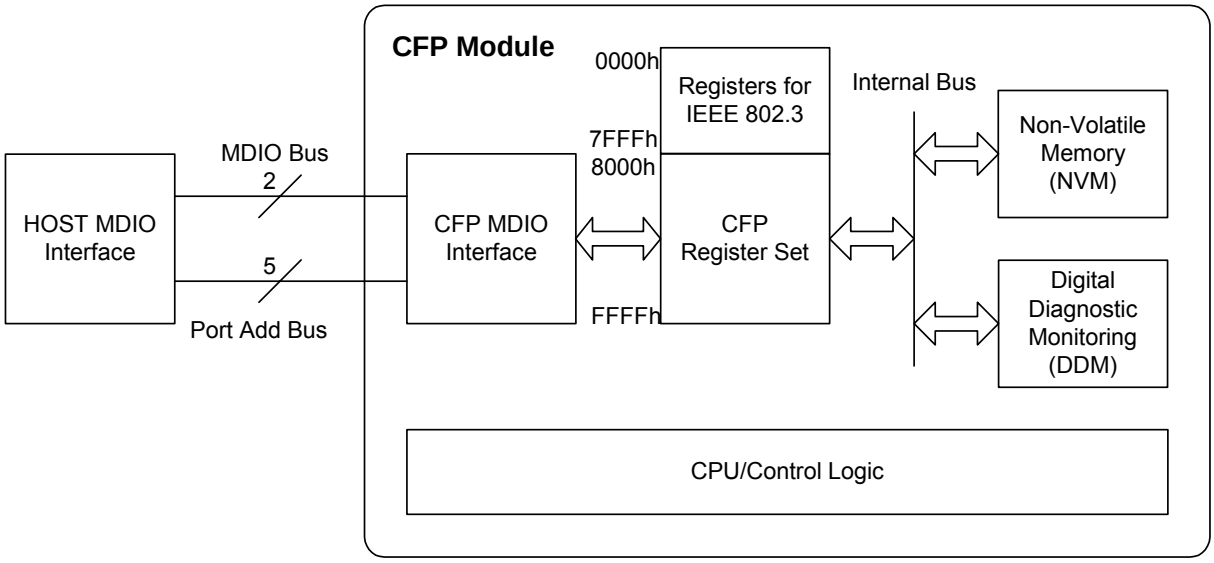
## 2.3 Interface Architecture

CFP MSA exemplifies a MDIO interface architecture illustrated in *Figure 1 CFP Management Interface Architecture*. This architecture recommends a dedicated MDIO logic block in the CFP module to handle the high rate MDIO data and a CFP register set that is divided into two register groups, the Non-Volatile Registers (NVR) and the Volatile Registers (VR). The NVRs are connected to a Non-Volatile Memory device for ID/Configuration data storage. Over the internal bus system, the VRs are connected to a device that executes the Host control commands and reports various Digital Diagnostic Monitoring (DDM) data. Note in the rest of this documentation, independent of implementation, CFP registers are also referred as NVRs or VRs.

In implementation, CFP registers shall use fast memory to shadow the NVM data and the DDM data. The shadow registers decouple the Host-side timing requirements from module vendor's internal processing, timing, and hardware control circuit introduced latency. Then this CFP shadow register set shall meet the following requirements:

a) It supports dual access from the Host and from module internal operations such as NVM and DDM data transfers.
b) It supports continuous Host access (read and write) with fast access memory at maximum MDC rate of 4 MHz.
c) It allows the uploading of NVM content into the CFP register shadow during module initialization. The data saving from CFP register shadow to NVM shall also be supported.
d) It supports the DDM data update periodically during the whole operation of the module. The maximum data refresh period shall meet the 100 ms for single network lane applications. If the number of lanes is greater than one, then the maximum data refresh period shall be 50 * (N + 1) ms, where N = number of network lanes supported in the application.
e) It supports the whole CFP register set including all NVRs and VRs.
f) Incomplete or otherwise corrupted MDIO bus transactions shall be purged from memory and disregarded.
g) The port address shall be allowed to change in fly without a module reset.

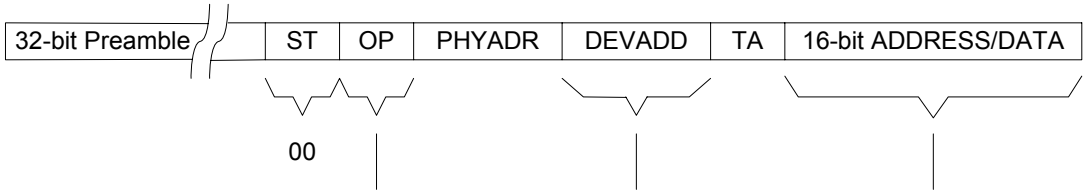
*Figure 1 CFP Management Interface Architecture*




## 2.4 MDIO Management Frame Structure

CFP MDIO interface uses the communication data frame structure defined in IEEE 802.3 Clause 45. Each frame can be either an address frame or a data frame. The total bit length of each frame is 64, consisting of 32 bits preamble, and the frame command body. The command body consists of 6 parts illustrated in *Figure 2 CFP MDIO Management Frame Structure*.

*Figure 2 CFP MDIO Management Frame Structure*




| OP | ACCESS TYPE |
|---|---|
| 00 | Address |
| 01 | Write |
| 11 | Read |
| 10 | Post Read Inc Add |

| DEVADD | DEVICE TYPE |
|---|---|
| 00000 | Reserved |
| 00001 | PMA/PMD |
| 00010 | WIS |
| 00011 | PCS |
| 00100 | PHY XS |
| 00101 | DTE XS |

| Access Type | Content |
|---|---|
| Address | Reg Address |
| Write | Write Data |
| Read | Read Data |
| Read Inc | Read Data |

ST = start bits (2 bits),
OP = operation code (2 bits),
PHYADR = physical port address (5 bits),
DEVADD = MDIO device address (or called device type, 5 bits),
TA = turn around bits (2 bits),
16-bit ADDRESS/DATA is the payload.

# 3 CFP REGISTER OVERVIEW

## 3.1 CFP Register Space

The total CFP register space (from 8000h to FFFFh) is logically divided into 8 pages with each page starting at even hex thousand, that is, 8000h, 9000h, A000h, …, F000h. Each page has 4096 addresses and is further divided into 32 tables. Each table has 128 CFP register addresses. Note that there is no physical boundary in between pages and tables. The sole purpose of this logical segmentation is for the convenience of CFP register space allocation and access control. The overview of the CFP register allocation is listed in *Table 2 CFP Register Allocation*.

## 3.2 Non-volatile Registers (NVRs)

CFP MSA specifies the starting address of all non-volatile registers at 8000h and it specifies 8 NVR tables for storing module ID information, setup data, and additional data stored by vendor and user. All NVR tables are implemented with lower 8-bit of space filled with data and the upper 8-bit of space reserved. A fully populated table shall require a maximum of 128 bytes of NVM to back up.

### 3.2.1 CFP NVR Tables

CFP MSA specifies CFP NVR 1 table for storing Basic ID data, CFP NVR 2 table for storing Extended ID data, CFP NVR 3 table for storing Network Lane Specific data. CFP NVR 4 table is allocated for storing Host Lane Specific data. Currently only the checksum of CFP NVR 3 is stored in CFP NVR 4 table.

### 3.2.2 Vendor NVR Tables

Vendor NVR 1 and Vendor NVR 2 tables are allocated for storing additional data that can be used by the vendor.

### 3.2.3 User NVR Tables

The User NVR 1 and User NVR 2 tables are allocated for module user to store data. User has the full read/write access to these tables.

### 3.2.4 NVR Content Management

All populated CFP NVR tables shall be backed up by physical non-volatile memory (NVM). On module Initialize, CFP NVR tables shall be uploaded with stored NVM values. CFP module vendor shall manage the content of CFP NVR tables.

The content and management of Vendor NVR tables and User NVR tables are subject to additional agreement between user and vendor.

### 3.2.5 User Private Use Registers

Starting at 8F00h, two additional tables are allocated for "User private use". CFP MSA does not specify nor restricts the use of these tables. The use of these User Private Use Registers is subject to additional agreement between CFP module users and vendors.

*Table 2 CFP Register Allocation*

| CFP Register Allocation | | | | | |
|---|---|---|---|---|---|
| **Starting Address in Hex** | **Ending Address in Hex** | **Access Type** | **Allocated Size** | **Data Bit Width** | **Table Name and Description** |
| 0000 | 7FFF | N/A | 32768 | N/A | Reserved for IEEE 802.3 use. |
| 8000 | 807F | RO | 128 | 8 | CFP NVR 1. Basic ID registers. |
| 8080 | 80FF | RO | 128 | 8 | CFP NVR 2. Extended ID registers. |
| 8100 | 817F | RO | 128 | 8 | CFP NVR 3. Network lane specific registers. |
| 8180 | 81FF | RO | 128 | 8 | CFP NVR 4. |
| 8200 | 83FF | RO | 4x128 | N/A | MSA Reserved. |
| 8400 | 847F | RO | 128 | 8 | Vendor NVR 1. Vendor data registers. |
| 8480 | 84FF | RO | 128 | 8 | Vendor NVR 2. Vendor data registers. |
| 8500 | 87FF | RO | 6x128 | N/A | Reserved by CFP MSA. |
| 8800 | 887F | R/W | 128 | 8 | User NVR 1. User data registers. |
| 8880 | 88FF | R/W | 128 | 8 | User NVR 2. User data registers. |
| 8900 | 8EFF | RO | 12x128 | N/A | Reserved by CFP MSA. |
| 8F00 | 8FFF | N/A | 2x128 | N/A | Reserved for User private use. |
| 9000 | 9FFF | RO | 4096 | N/A | Reserved for vendor private use. |
| A000 | A07F | R/W | 128 | 16 | CFP Module VR 1. CFP Module level control and DDM registers. |
| A080 | A0FF | RO | 128 | 16 | Reserved by CFP MSA. |
| A100 | A1FF | RO | 2x128 | N/A | Reserved by CFP MSA. |
| A200 | A27F | R/W | 128 | 16 | Network Lane VR 1. Network lane specific registers. |
| A280 | A2FF | R/W | 128 | 16 | Network Lane VR 2. Network lane specific registers. |
| A300 | A3FF | RO | 2x128 | N/A | Reserved by CFP MSA. |
| A400 | A47F | R/W | 128 | 16 | Host Lane VR 1. Host lane specific registers. |
| A480 | AFFF | RO | 23x128 | N/A | Reserved by CFP MSA. |
| B000 | FFFF | RO | 5x4096 | N/A | Reserved by CFP MSA. |

## 3.3 Volatile Registers (VRs)

Page A000h is allocated for volatile registers. CFP MSA specifies 4 VR tables for module configuration, control, and various DDM related functions. All VR registers are 16-bit data with unused bits reserved. A fully populated table requires a maximum of 256 bytes of physical memory. There is no NVM backup for VR registers but CFP MSA specifies their initial values.

### 3.3.1 CFP Module NV 1 Table

This table, starting at address A000h, contains command/setup, module control, lane control, Module state, FAWS (fault/alarm/warning/status), FAWS Summary, and other DDM related registers. All registers are assigned with initial values to insure the correct startup condition.

### 3.3.2 Network Lane Specific Register Table

Two tables starting from A200h and ending at A2FFh are allocated to support network lane specific registers including lane FAWS, controls, and A/D values (For copper network lanes some of the DDM register support may not apply.). For each supported register, CFP MSA allocates a 16-lane array for it. Should in the future more than 16 lanes are needed additional tables can be allocated in the subsequent reserved addresses.

### 3.3.3 Host Lane Specific Register Table

One table starting at A400h is allocated to support host lane specific registers. For each supported parameter, CFP MSA allocates a 16-lane array for it. Should in the future more than 16 lanes are considered additional tables can be allocated in the subsequent reserved addresses.

## 3.4 Module Vendor Private Registers

Page 9000h is reserved exclusively for module vendors of CFP module for their development and implementation needs.

## 3.5 Reserved CFP Registers

All reserved CFP registers and all the reserved bits in a CFP register shall be “read-only” and they shall be read as all-zeros. Writing to reserved CFP registers or bits shall have no effect. CFP registers related to unused lanes for a specific module type shall be treated as reserved CFP registers. An example would be CFP registers relating to network lanes 15:4 for a 100GBASE-LR4 module (in which only network lanes 3:0 are active).

### 3.5.1 Un-implemented Registers

A particular CFP module may not implement every function by this Specification. The registers or bits in the registers representing the un-implemented functions shall be read as 0. Writing to these registers or register bits has no effect.

## 3.6 CFP Register Data Types

A CFP register collects management information in a basic form of a 16-bit word, occupying one MDIO register address. CFP Registers support the following data types.

### 3.6.1 Byte

A byte can represent a signed number, unsigned number, or an array of 8-bit value. If a CFP register only contains one byte of data, it allocates the least significant 8 bits for it, with all most significant 8 bits reserved. All the non-volatile registers contain a byte with bit 7 being the most significant bit.

### 3.6.2 Word

A word is a 16-bit-wide data type. It can represent a signed number, unsigned number, or an array of 16-bit values. It can also be used as 2 bytes, the most significant byte and the least significant byte. The most significant byte occupies the bits from 15 to 8. The least significant byte occupies the bits from 7 to 0. All the volatile registers contain a word with bit 15 being the most significant bit.

### 3.6.3 Bit Field

A CFP register can contain one or more bit fields. A bit field consists of one or more bits, which can represent a number or an array of bit values. If a bit field represents a number the bit with the highest bit number is the most significant bit.

### 3.6.4 Two's Complement

Wherever signed byte is used, two's complement is assumed. *Table 3* illustrates the example bit patterns and values of a signed byte in two's complement form. For a 16-bit signed word, the same format applies with the most significant bit (bit 15) to be the sign bit. The value of +32767 = 7FFFh and the value of -32768 = 8000h.

*Table 3 Bit Pattern of a Two's Complement Byte Data*

| BIT 7 (SIGN BIT) | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 | | VALUE |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | = | +127 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | = | +1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | = | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | = | -1 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | = | -127 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | = | -128 |

# 4 CFP CONTROL AND SIGNALING THEORY

## 4.1 CFP Module States and Related Signals

To facilitate a well-defined CFP module startup and module turn-off sequences and other applications, CFP MSA specifies a list of CFP module states that CFP module shall support.

In association with these states, a set of signals that are related to state transitions are also defined. In the following text, a signal name with a lower-case "s" suffix stands for a combination of multiple signals.

### 4.1.1 Signals Affecting Transition of CFP Module States

Three inputs and one internally generated signal are defined and each of them is a logical combination of hardware signal status, CFP register bit status, and module internally generated logic signals in some cases. These signals affect the state transition.

#### 4.1.1.1 Combined Module Reset Signal MOD_RSTs

For reset operation, CFP module internally defines MOD_RSTs as follows:
MOD_RSTs = (**NOT** MOD_RSTn) **OR** (Soft Module Reset) **OR** Vcc_Reset,
where,

MOD_RSTn is the hardware pin input,
Soft Module Reset is a CFP register bit, de-asserted in Reset and,
Vcc_Reset is the CFP internally generated logic signal indicating the validity of Vcc

Vcc_Reset = 1 if Vcc at connector is lower than a specified threshold,
= 0 if Vcc is within range.

Note that Vcc_Reset does not correspond to the operating voltage range specified in the CFP MSA Hardware specification. Vcc_Reset is the threshold voltage below which the module is held in reset, and above which normal operation can be initiated.

The threshold for Vcc_Reset is vendor specific and shall be lower than Vcc Low Alarm Threshold (808Eh).

#### 4.1.1.2 Combined Module Low Power Signal MOD_LOPWRs

MOD_LOPWRs = MOD_LOPWR **OR** (Soft Module Low Power) **OR** HW_Interlock,
where,
MOD_LOPWR is the hardware pin input,
Soft Module Low Power is the CFP register bit, de-asserted in Reset, HW_Interlock is defined below.

#### 4.1.1.2.1 HW_Interlock

HW_Interlock (hardware interlock) is an internally generated logic value, based upon the comparison between the module's power class (Refer to Reference 5, Section 2.2.1.4 for power class definition) versus the host cooling capacity as encoded on the HW_IL_MSB and HW_IL_LSB input pins. Its purpose is to prevent an otherwise-dangerous high power condition which might harm either the host or the module itself, due to power requirements which the host is not able to support.

The status of HW_Interlock is defined as follows:
HW_Interlock = 0 if HW_IL_MSB and HW_IL_LSB = 11b or,
HW_Interlock = 0 if module power <= Host cooling capacity, else
HW_Interlock = 1 if module power > Host cooling capacity.

In operation, the module samples the status of the HW_IL_MSB and HW_IL_LSB input pins once during the Initialize State. To ensure a reliable sampling, Host shall hold HW_IL_MSB and HW_IL_LSB signal valid until the module exits Initialize State. The module stores these values in a variable HW_IL_inputs. (The Host is free to reprogram the usage of the PRG_CNTLn input pins and change their values at any time after the module exits the Initialize State.)

When both the MOD_LOPWR input pin and the Soft Module Low Power register bit are de-asserted, the module then compares the variable HW_IL_inputs to the power class for which it is designed (Defined in the Power Class field of register 8001h). The result of this comparison updates the HW_Interlock status. The module remains in the Low-Power State if HW_Interlock evaluates to '1' (this does not result in a transition to the Fault State). Conversely, if HW_Interlock evaluates to '0', the module is allowed to transition to the High-Power-up State.

### 4.1.1.3 Combined Transmitter Disable Signal TX_DISs

TX_DISs = TX_DIS **OR** (Soft TX Disable),
where,
TX_DIS is the hardware pin,
Soft TX Disable is a CFP register bit, de-asserted in Reset.

### 4.1.1.4 Fault Conditions

Fault conditions are represented by all the non-reserved bits except bit 0 in the Module Fault Status register. Each bit is driven by a particular fault condition through hardware or software means in CFP module. Any assertion of these bits causes the CFP module to enter the Fault state.

### 4.1.1.5 Minimum Signal Duration

The host shall provide the minimum assert/de-assert pulse width of 100 micro-seconds to guarantee the module to enter a transient state. The module's behavior for pulse width less

than 100 micro-seconds is un-defined. (This clause is subject to removal per Group discussion. The timing of these signals shall be defined by CFP MSA HW Spec. – Editor)

### 4.1.2 Signals Affected by Module Insertion or State Transition

CFP MSA specifies a number of output signals, both in the form of hardware pins and CFP register bits, reporting to the Host the transitions between states. In most of cases, the hardware pins are mirrored with CFP register bits.

#### 4.1.2.1 MOD_ABS

This is a hardware signal which reports the presence of an inserted CFP module to the Host. There is no MDIO register counterpart of it. For more information please refer to Reference [5].

#### 4.1.2.2 GLB_ALRM

GLB_ALRM is a CFP internal signal that is the invert signal of GLB_ALRMn. The latter is the hardware signal, as an interrupt request to the Host, reporting FAWS occurrence during module operation. When the CFP module detects that any bit is asserted in CFP FAWS latch registers (A022h through A026h), it shall assert GLB_ALRM, provided that those latch bits are enabled by CFP FAWS enable registers (A028h through A02Ch). GLB_ALRM is cleared upon the Host reading corresponding latched CFP registers.

#### 4.1.2.3 INIT_DONE

INIT_DONE is a CFP internally generated and used signal indicating the completion of module initialization. This signal is dedicated to module startup process and it is asserted upon exiting the Initialize state. This signal remains asserted until MOD_RSTs is asserted.

#### 4.1.2.4 HIPWR_ON

HIPWR_ON is a CFP internally generated status signal represented by a CFP register bit. It is the logical OR of TX-Off state, Turn-TX-on state, Ready state, and TX-Turn-off. It is asserted when the module exits High-Power-up state and remains asserted whenever the module is not in the Low Power condition.

#### 4.1.2.5 MOD_READY (Ready State)

MOD_READY is an alias of Ready State bit in Module State register. The Ready State bit is asserted when the module enters Ready state and remains asserted as long as the CFP module is in the Ready state.

#### 4.1.2.6 MOD_FAULT (Fault State)

MOD_FAULT is an alias of Fault State bit in Module State register. The Fault State is asserted when the module enters Fault state and remains asserted as long as the CFP module is in the Fault state.

### 4.1.3 CFP Module States

CFP MSA specifies 10 CFP module states in the context of defining the startup, normal operation, and module turn-off sequences. Five of the 10 states are steady states and the

rest are transient states. The behavior of input and output to a state, and the state itself shall be defined for the clear hand-shaking between the Host and the CFP module.

Host can read CFP Registers Module State and Module State Latch to determine the module state at the time of read, except in Reset State and Initialize State.

#### 4.1.3.1 Reset State (Steady)

MOD_RSTs assertion causes CFP module to reset, including reset of any digital circuitry that may consist of module control function and any high speed circuitry if they are re-settable. In particular the MDIO interface will be held in a high impedance state. Therefore, the Host will read "FFFFh" from any CFP register addresses while a host write will have no effect.

In this state, all circuits are in low power mode and stay in reset whenever MOD_RSTs is asserted. The MOD_RSTs supersedes the status of other input such as MOD_LOPWRs and TX_DISs.

Module reset shall happen when MOD_RSTs is asserted, when 3.3 V power supply is turned on, or when CFP module is hot-plugged in to the connector. When CFP module is already in connector, MOD_RSTs assertion can be used to resolve any hardware hang-up, particularly a communication hang-up or other types of control hang-ups.

Reset state is a steady state and shall exit to Initialize State upon the de-assertion of MOD_RSTs.

#### 4.1.3.2 Initialize State (Transient)

Upon entering this state, CFP module shall keep MDIO interface held at high impedance state during the initialization. All the host-reads return “FFFFh” and all the host-writes have no effect.

Upon the completion of initialization, all the NVRs are loaded with NVM values and VRs are initialized. Analog A/D Value Registers shall be read with live values. All the allowed FAWS registers shall contain valid data. CFP module shall then release the hold of MDIO interface and assert GLB_ALRM bit to alert the Host of this MDIO ready condition.

On the exit of initialization, the CFP module shall enter Low-Power State. If initialization fails, it shall enter Fault State. Initialize State is a transient state. The CFP MSA specifies the maximum initialization time to be 2.5 seconds.

#### 4.1.3.3 Low-Power State (Steady)

CFP module enters and stays in the Low-Power state when MOD_LOPWRs is asserted. In Low-Power state, the MDIO interface and control circuits shall remain powered and fully functional. All other high-power consuming circuits shall be in low-power condition.

In this state, the PHYs are powered down and loop-back is not possible. The nAUI outputs shall go to a steady state (no transitions).

Low-Power state is a steady state and it shall exit to High-Power-up state upon the de-assertion of MOD_LOPWRs.

#### 4.1.3.4 High-Power-up State (Transient)

The Host drives CFP module into High-Power-up state from Low-Power state by the transition of de-asserting MOD_LOPWRs. In this state CFP module powers up all the functional circuitry and completes all required initialization such as inrush current control, TEC temperature stabilization, etc.

Upon entering the High-Power-up state, the module shall assert HIPWR_ON signal and then shall enter TX-Off state. If the powering up process fails CFP module shall enter the Fault state and de-assert HIPWR_ON.

High-Power-up is a transient state. The time it takes to complete the process varies from module to module depending upon applications. The vendor shall specify the application-specific value in Maximum High-Power-up Time CFP register.

In this state, the nAUI outputs are not defined.

#### 4.1.3.5 TX-Off State (Steady)

CFP module enters and stays in the TX-Off state when TX_DISs is asserted. In TX-Off state, the transmitters in all the network lanes are turned off but all other parts of the module remain high powered and functional.

TX-Off state is a steady state and it shall exit to TX-Turn-on state upon the de-assertion of TX_DISs, or it shall exit to High-Power-Down state upon the assertion of MOD_LOPWRs or MOD_RSTs.

#### 4.1.3.6 TX-Turn-on State (Transient)

The Host drives CFP module into TX-Turn-on state by the transition of de-asserting TX_DISs signal from TX-Off state.

Asserting TX_DISs causes a global action that turns off all the transmitters across all network lanes.

In this state, CFP module either enables or disables lanes according to the configuration in Individual Network Lane TX_DIS Control CFP register. The lanes that are disabled shall remain disabled after the module enters the TX-Turn-on state.

Changing TX_DISs does not affect Individual Network Lane TX_DIS Control CFP register. Upon successfully turning on the desired transmitters CFP module shall assert MOD_READY to inform the Host. The CFP module shall enter Ready state. If the turning

on TX process fails due to any fault conditions CFP module shall enter the Fault state and keep MOD_READY de-asserted.

TX-Turn-on is a transient state. The time it takes to complete the TX-Turn-on process varies depending upon the applications. The vendor shall specify the Maximum TX-Turn-on Time CFP register.

#### 4.1.3.7 Ready State (Steady)

CFP module enters from TX-Turn-on state and stays in Ready state upon successful transmitter turning on. In this state CFP module is ready for passing data. All the MDIO, DDM, and other functions are fully functional.

Ready state is a steady state and it shall exit to other states upon the assertion of MOD_RSTs, MOD_LOPWRs, TX_DISs, or Fault conditions.

#### 4.1.3.8 TX-Turn-off State (Transient)

The Host drives CFP module into TX-Turn-off state by asserting TX_DISs, MOD_LOPWRs, or MOD_RSTs. In this state CFP module turns off all the network lane transmitters regardless the setting in Individual Network Lane TX_DIS Control register.

TX-Turn-off is a transient state. The time it takes to complete the turn-off shall meet the spec listed in *Table 8 Timing for Management Interface Control and Status*.

#### 4.1.3.9 High-Power-Down State (Transient)

CFP module enters High-Power-down state by the transition of asserting MOD_LOPWRs or MOD_RSTs. In this state, CFP module powers down all the power-consuming circuitry to maintain the overall power consumption less than 2 Watts. CFP module shall maintain MDIO interface fully functional.

Upon powering down the module CFP module shall de-assert HIPWR_ON to inform the Host. The CFP module shall either enter Low-Power state or Reset state depending upon the status of MOD_RSTs.

High-Power-down is a transient state. The time it takes to complete this transient state shall meet the spec listed in *Table 8 Timing for Management Interface Control and Status*.

#### 4.1.3.10 Fault State (Steady)

CFP module enters this state from any states except Reset state upon the assertion of bits in Module Fault Status register. On entry to this state, CFP module shall immediately de-assert MOD_READY.

In this state, the CFP management interface and DDM shall remain fully functional. The module shall be put in low power mode to avoid the possibility of permanent module damage. Further diagnosis of the failure can be conducted by interrogating CFP FAWS summary registers and other registers.

In this state, the PHYs are powered down and loop-back is not possible. The nAUI outputs shall go to a steady state (no transitions).

Fault state is a steady state, and it shall exit to Reset state upon the assertion of MOD_RSTs.

## 4.2 State Transition Diagram

The CFP module state transition is shown in *Figure 3 State Transition Diagram during Startup and Turn-off*. The top row of states and the associated transitions are typical of the CFP module startup sequence. The Host can control the power-on sequence by controlling the conditions of MOD_RSTn, MOD_LOPWR, and TX_DIS.

When TX_DISs is asserted in Ready state, CFP module shall enter the TX-Turn-off state and then transient to TX-Off state.

When MOD_LOPWRs is asserted in Ready state, CFP module shall enter TX-Turn-off state and High-Power-down states sequentially. And then it shall enter Low-Power state.

When MOD_RSTs is asserted in Ready state, CFP module shall first enter TX-Turn-off State and then High-Power-down State before entering Reset State.

When one or more fault conditions occur, CFP module shall enter the Fault State.

Behavior of the signals affected by module state transition is defined in *Table 4 Behavior of Signals Affected by Module State Transition*. Of the four signals listed in the table, GLB_ALRM drives the GLB_ALRMn pin. During module startup GLB_ALRMn signals the Host the completion of Initialization.

The signals HIPWR_ON, MOD_READY, and MOD_FAULT are CFP internally generated signals and are defaults of the programmable alarm pins PRG_ALRMx.

CFP register bits are allocated and can perform the same functions as the hardware control input pins. Additionally, Module State and Module State Latch registers provide the current module state and the state history.

*Figure 3 State Transition Diagram during Startup and Turn-off*

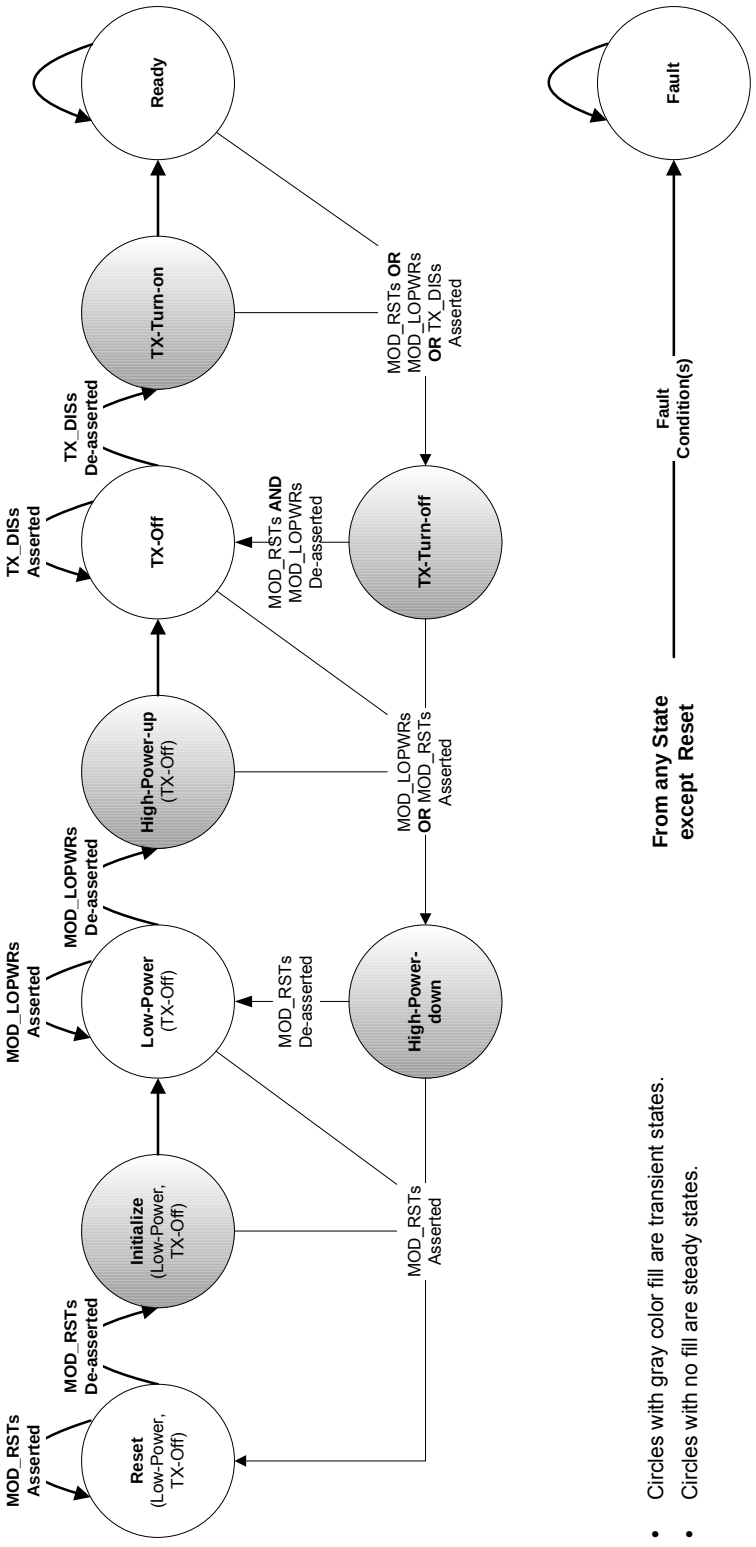


*Table 4 Behavior of Signals Affected by Module State Transition*

| | CFP Module State | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Signals** | **Reset** | **Initialize** | **Low-Power** | **High-Power-up** | **TX-Off** | **TX-Turn-on** | **Ready** | **TX-Turn-off** | **High-Power-down** | **Fault** |
| **GLB_ALRM** | **D*** | **D*** | **A** | **A/D** | **A/D** | **A/D** | **A/D** | **A/D** | **A/D** | **A/D** |
| **HIPWR_ON** | **D*** | **D*** | **D** | **D** | **A** | **A** | **A** | **A** | **D** | **D** |
| **MOD_READY** | **D*** | **D*** | **D** | **D** | **D** | **D** | **A** | **D** | **D** | **D** |
| **MOD_FAULT** | **D*** | **D*** | **D** | **D** | **D** | **D** | **D** | **D** | **D** | **A** |
| **D* = De-asserted, guaranteed by internal hardware INIT_DONE signal. Note GLB_ALRM is the internal complement of GLB_ALRMn pin and it shall be de-asserted if MOD_RSTs is asserted. The HIPWR_ON, MOD_READY, and MOD_FAULT are defaulted to PRG_ALRM1, PRG_ALRM2, and PRG_ALRM3 pins respectively on module startup.** | | | | | | | | | | |
| **A/D = Asserted or De-asserted depending upon Host's clear-on-read and Host-enabled status.** | | | | | | | | | | |
| **A = Asserted.** | | | | | | | | | | |
| **D = De-asserted.** | | | | | | | | | | |

## 4.3 Examples of Module Startup and Turn-off Sequence

The examples below illustrate that the Host can control the module startup sequence by setting the initial conditions of MOD_RSTs, MOD_LOPWRs, and TX_DISs.

### 4.3.1 Power-up CFP Module to Ready State without Host Transition Control

*Figure 4 Module Startup Sequence Example 1: No Host Transition Control* illustrates CFP MSA specified module startup sequence for the Host to power up the CFP module to Ready state without the Host intervention. In this instance, the Host sets up the CFP module connector initial condition by applying Vcc to the connector and de-asserting MOD_RSTn, MOD_LOPWR, and TX_DIS.

The staggering arrangement of the connector pins [Reference 5] causes ground and Vcc to first contact CFP module. At the time when Vcc becomes available the pull-up/pull-down resistors in the module assert MOD_RSTn, MOD_LOPWR, and TX_DIS. As the "Plug-in" action progresses, MOD_RSTn and TX_DIS are in contact with the Host and hence they are de-asserted. Finally MOD_ABS and MOD_LOPWR are engaged. This causes MOD_LOPWR de-assertion. Hence the initial conditions the Host applies to the CFP module take effect.

The CFP module, under these initial conditions, goes through Reset, Initialize, High-Power-up, TX-Off, TX-Turn-on states, and finally enters Ready state. During this course, the CFP module asserts GLB_ALRM, HIPWR_ON, and MOD_READY signals sequentially. These

signals inform host the completion of module initialization and MDIO availability, module fully powering up, and module ready, respectively.

MSA specifies two registers which contain Maximum High-Power-up Time and Maximum TX-Turn-on Time. Host uses these two parameters to determine how long it shall wait at each stage if reading HIPWR_ON and MOD_READY as the signals of progress monitor is not desirable or not available. Vendor shall provide these two register values as they may vary from product to product and from vendor to vendor.

### 4.3.2 Power-up the Module with Full Host Transition Control

In contrast to the case presented in 4.3.1, the Host can apply full control over the course of module power-up sequence. This example is illustrated by *Figure 5 Module Startup Sequence Example 2: Full Host Transition Control*.

### 4.3.3 Power-Up the Module with Some Host Transition Control

In some case, it is desirable to power up the module to Low-Power state. For this example, the Host may change PRG_ALRMs and PRG_CNTLs, before de-asserting MOD_LOPWR in the Low-Power State. This example is illustrated in *Figure 6 Module Startup Sequence Example 3: Some Host Transition Control*.

### 4.3.4 Example of Module Turn-off Sequence

*Figure 7 Module Turn-off Sequence Example: No Host Transition Control* illustrates the example of module turn-off sequence without the Host transition control by hot-un-plug. In this case, un-plug action causes assertions of MOD_ABS and MOD_LOPWR first. Then due to module extraction, MOD_RSTn is asserted. CFP module enters TX-Turn-off state and High-Power-down state subsequently. Between these events, CFP module de-asserts MOD_READY, HIPWR_ON, and GLB_ALRM sequentially and enters Reset. Finally Vcc is disconnected.

## 4.4 Special Modes of Operation

CFP MSA defines additional operation modes such as transmitting only and receiving only for a CFP module. CFP MSA specifies the standard operation mode is bi-directional. Uni-directional operation is optional (vendor-specific support). CFP register Module Enhanced Options register identifies what optional operation modes are supported for a particular module.

To power up the module in receiving only mode, the Host needs to assert TX_DIS and keeps other control signals as required. In this way CFP module will power up to TX-Off state and uses HIPWR_ON to inform the Host it is ready for receiving data. *Figure 8 Module Start-up Sequence Example: Operating in RX Only Mode* depicts this application. The support of transmitting only mode is no different from normal working mode except that the Host may expect CFP module to squelch the electrical outputs.

*Figure 4 Module Startup Sequence Example 1: No Host Transition Control*

NOTE: the following assumes the Host does not change the default register values

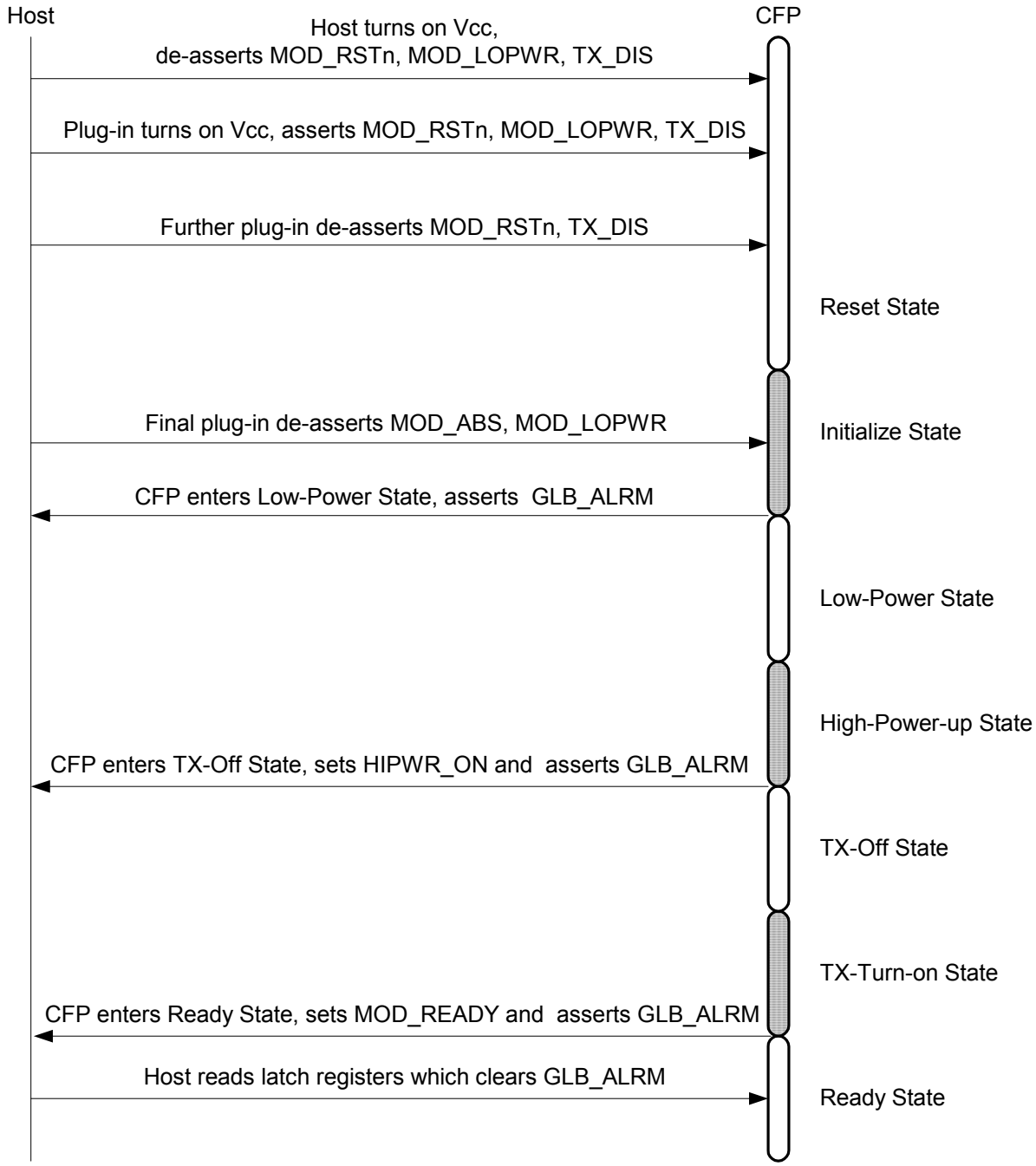


*Figure 5 Module Startup Sequence Example 2: Full Host Transition Control*

NOTE: the following assumes the Host does not change the default register values

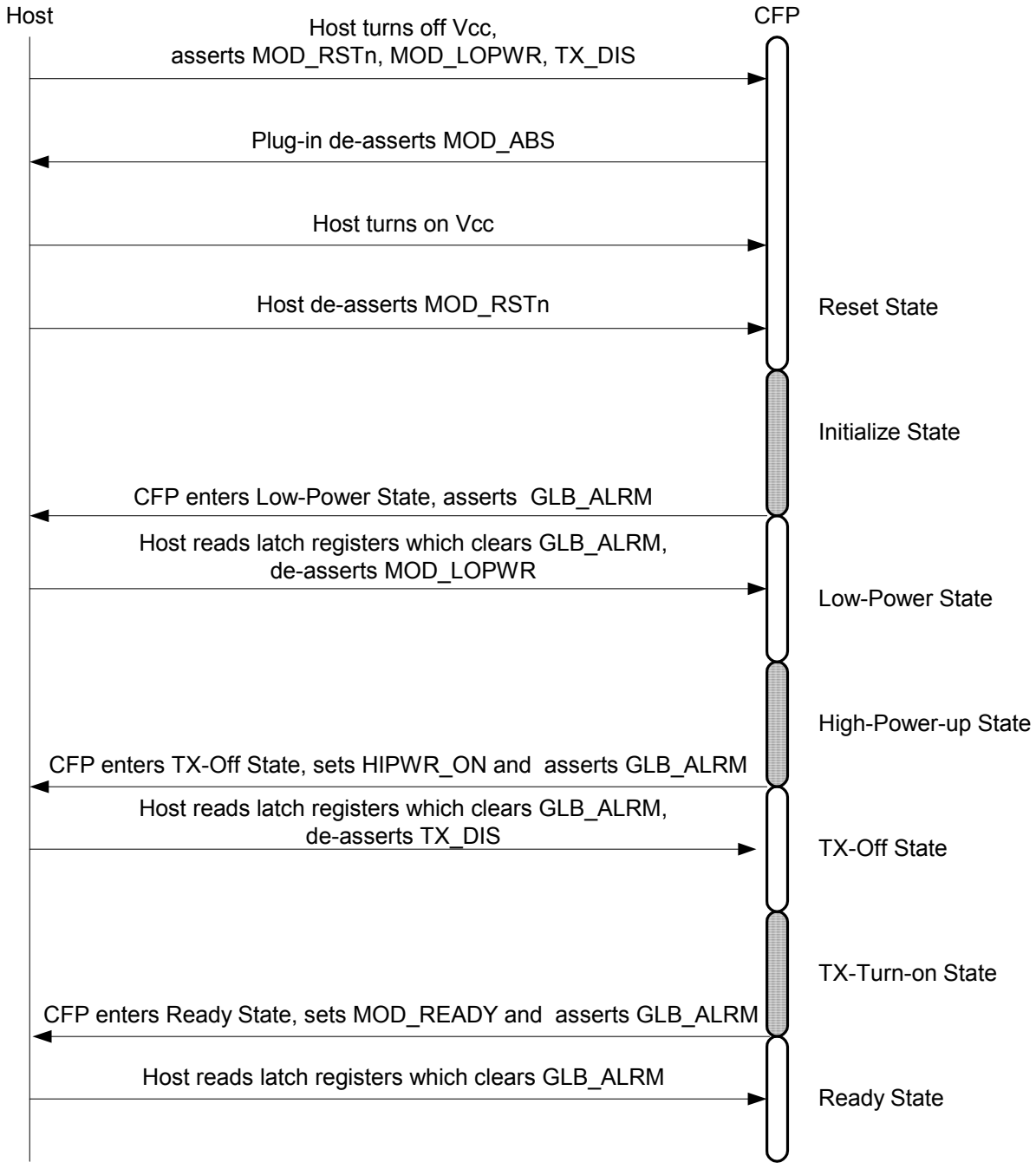


*Figure 6 Module Startup Sequence Example 3: Some Host Transition Control*

NOTE: the following assumes the Host does not change the default register values, except as noted below

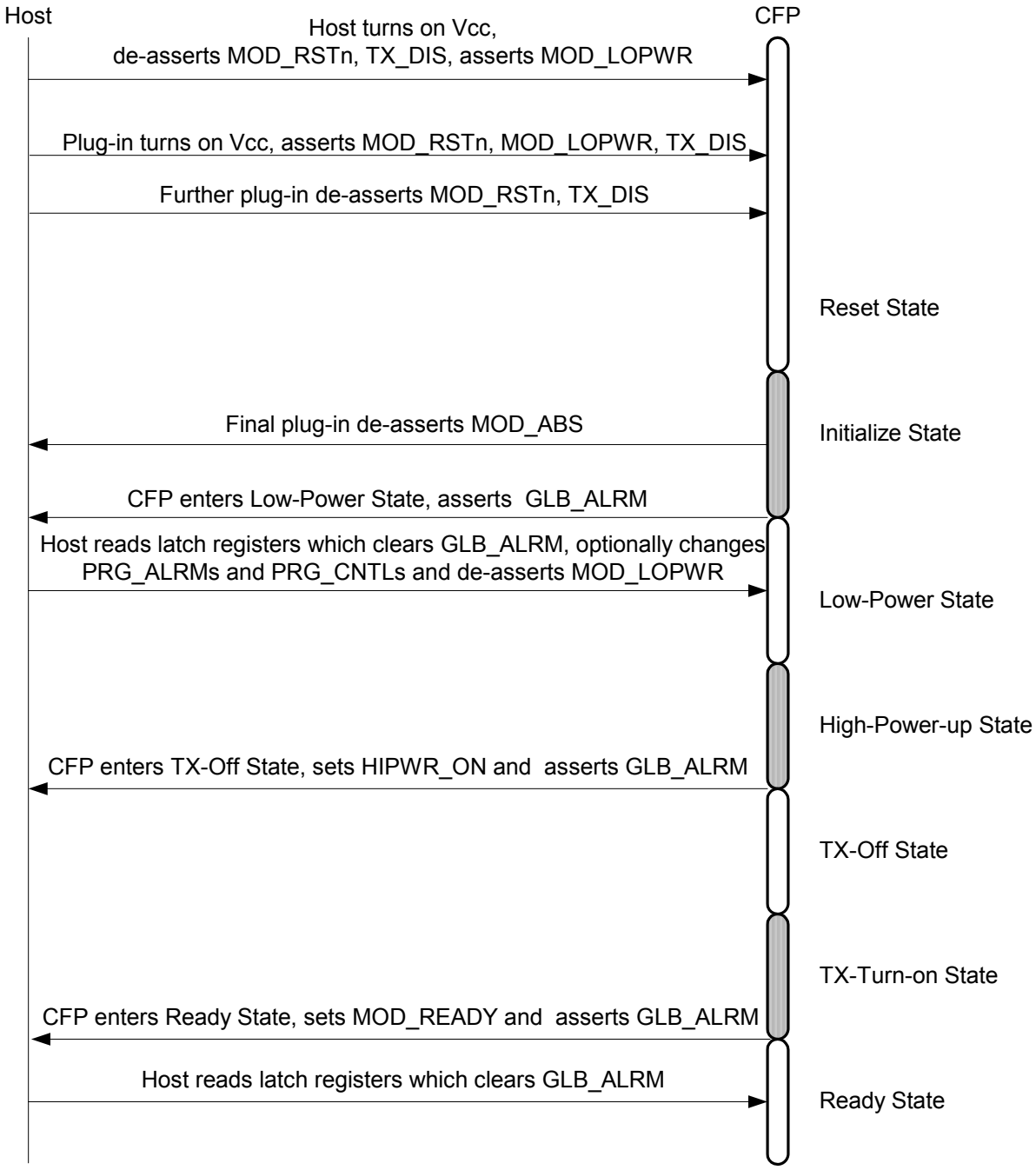


*Figure 7 Module Turn-off Sequence Example: No Host Transition Control*

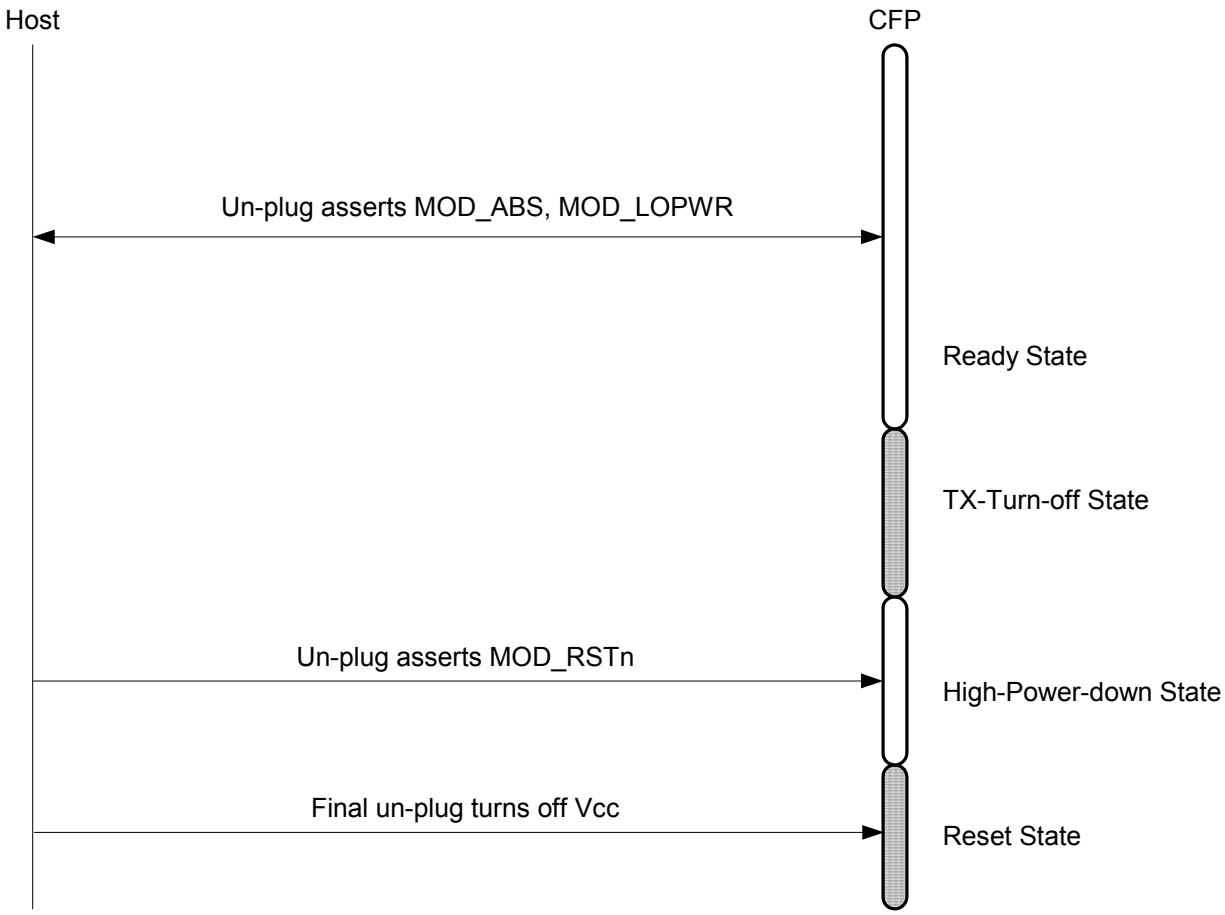
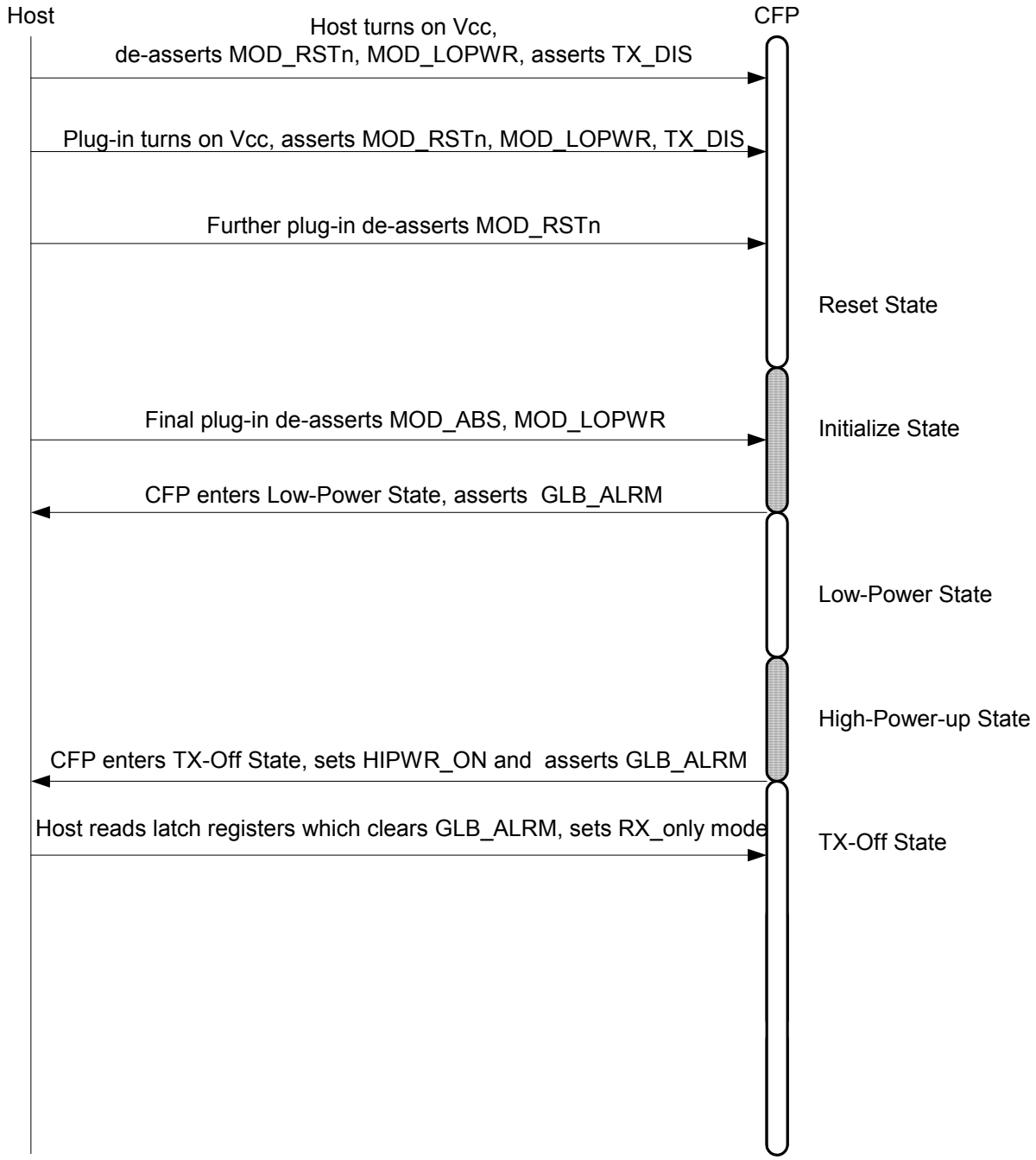


*Figure 8 Module Start-up Sequence Example: Operating in RX Only Mode*

NOTE: the following assumes the Host does not change the default register values



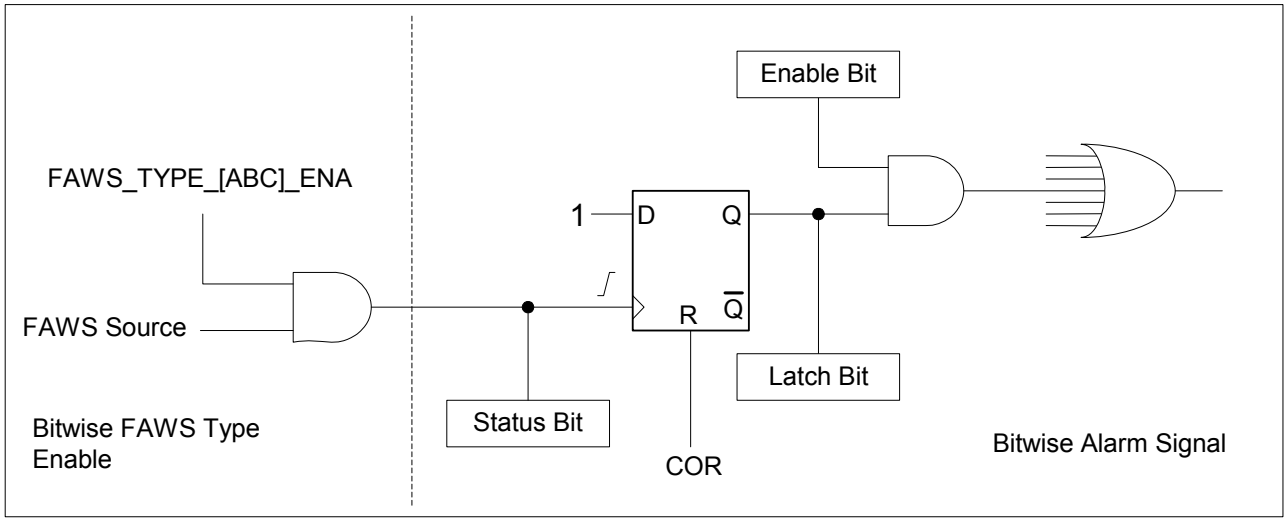
## 4.5 Behavior of FAWS in CFP States

CFP module shall eliminate the spurious FAWS signals in various CFP module states, based on a set of rules defined by CFP MSA. CFP MSA classifies all the GLB_ALRM contributing FAWS signals into three types: FAWS_TYPE_A, FAWS_TYPE_B and FAWS_TYPE_C. The type for each FAWS signal is annotated in *Table 22 CFP Module VR 1*, *Table 23 Network Lane VR 1*, and *Table 25 Host Lane VR 1*.

*Figure 9 FAWS Signal Model for a Single Bit* illustrates the mechanism of a signal source contributing to the global alarm and the relationship between status, latch, and enable registers. In this figure, a set of CFP internal FAWS_[ABC]_ENA signals are used to control the behavior of each FAWS source signal.

Note that Module State register is not subject to FAWS_[ABC]_ENA control.

*Figure 9 FAWS Signal Model for a Single Bit*




CFP MSA specifies the behavior of each FAWS type according to *Table 5 Behavior of FAWS Type in Different Module States*. Note that CFP module shall use FAWS_TYPE_[ABC]_ENA to eliminate any spurious FAWS reporting during state transition.

*Table 5 Behavior of FAWS Type in Different Module States*

| | CFP Module State | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **FAWS Type** | **Reset** | **Initialize** | **Low-Power** | **High-Power-up** | **TX-Off** | **TX-Turn-on** | **Ready** | **TX-Turn-off** | **High-Power-down** | **Fault** |
| **FAWS_TYPE_A** | **OFF** | **OFF** | **A** | **A** | **A** | **A** | **A** | **A*** | **A*** | **A** |
| **FAWS_TYPE_B** | **OFF** | **OFF** | **OFF** | **OFF** | **A** | **A** | **A** | **A*** | **OFF** | **A** |
| **FAWS_TYPE_C** | **OFF** | **OFF** | **OFF** | **OFF** | **OFF** | **OFF** | **A** | **OFF** | **OFF** | **A** |
| **A = FAWS sources are allowed (i. e. not masked). Status registers and latch registers are functional. A/D values reflect the actual measurements.** | | | | | | | | | | |
| **A* = OFF if the MOD_RSTs is asserted.** | | | | | | | | | | |
| **OFF = FAWS sources (status bits) are gated off by CFP module. As a result, the corresponding latch registers will not capture (latch) new events. Latch registers and Enable registers are kept un-changed from previous states. A/D values reflect the actual measurements, although they may not all be available in Low-Power State depending upon module implementation.** | | | | | | | | | | |

## 4.6 Global Alarm System Logic

The CFP module uses GLB_ALRM, to alert the Host any condition outside normal operating conditions. The GLB_ALRM is related to all the contributing FAWS registers including the status registers, the latch registers, and the enable registers, all listed in *Table 6 Global Alarm Related Registers*.

*Figure 10 Global Alarm Signal AggregationFigure 10 Global Alarm Signal Aggregation* depicts the global alarm signal aggregation logic. In this system, status registers drive the latch registers on a bit-by-bit basis. The logic OR of all enabled bits in the latched registers drives GLB_ALRM. This simple and flat OR combinational logic minimizes the assert time after a global alarm condition happens.

Also shown in *Figure 10*, the Host shall control which latched bits resulting in a global alarm assertion by asserting individual bits in the enable registers. All enabling bits shall be volatile and startup with initial values defined in *Table 22 CFP Module VR 1*, *Table 23 Network Lane VR 1*, and *Table 25 Host Lane VR 1*.

When GLB_ALRM alerts the Host to a latched condition, the Host may query the latched registers for the condition. The latched bits are cleared on the read of the corresponding register. Thus a read of all latched registers can be used to clear all latched register bits and to de-assert GLB_ALRM.

In order to minimize the number of reads for locating the origin of the global alarm condition, the Host may use the global alarm query hierarchy listed in *Table 7 Global Alarm Query Hierarchy*.

*Table 6 Global Alarm Related Registers*

| Description | CFP Register Addresses |
|---|---|
| Summary Registers | |
| Global Alarm Summary | A018h |
| Status Registers | |
| Module State | A016h |
| Module General Status | A01Dh |
| Module Fault Status | A01Eh |
| Module Alarms/Warnings 1 | A01Fh |
| Module Alarms/Warnings 2 | A020h |
| Network Lane Alarms and Warnings | A200h + n, n= 0, 1, …, N-1. |
| Network Lane Fault and Status | A210h + n, n = 0, 1, …, N-1. |
| Host Lane Fault and Status | A400h + m, m = 0, 1, …, M-1. |
| Latch Registers | |
| Module State Latch | A022h |
| Module General Status Latch | A023h |
| Module Fault Status Latch | A024h |
| Module Alarms/Warnings 1 Latch | A025h |
| Module Alarms/Warnings 2 Latch | A026h |
| Network Lane Alarms and Warnings Latch | A220h + n, n = 0, 1, …, N-1. |
| Network Lane Fault and Status Latch | A230h + n, n = 0, 1, …, N-1. |
| Host Lane Fault and Status Latch | A410h + m, m = 0, 1, …, M-1. |
| Enable Registers | |
| Module State Enable | A028h |
| Module General Status Enable | A029h |
| Module Fault Status Enable | A02Ah |
| Module Alarms/Warnings 1 Enable | A02Bh |
| Module Alarms/Warnings 2 Enable | A02Ch |
| Network Lane Alarms and Warnings Enable | A240h + n, n = 0, 1, …, N-1. |
| Network Lane Fault and Status Enable | A250h + n, n = 0, 1, …, N-1. |
| Host Lane Fault and Status Enable | A420h + m, m = 0, 1, …, M-1. |

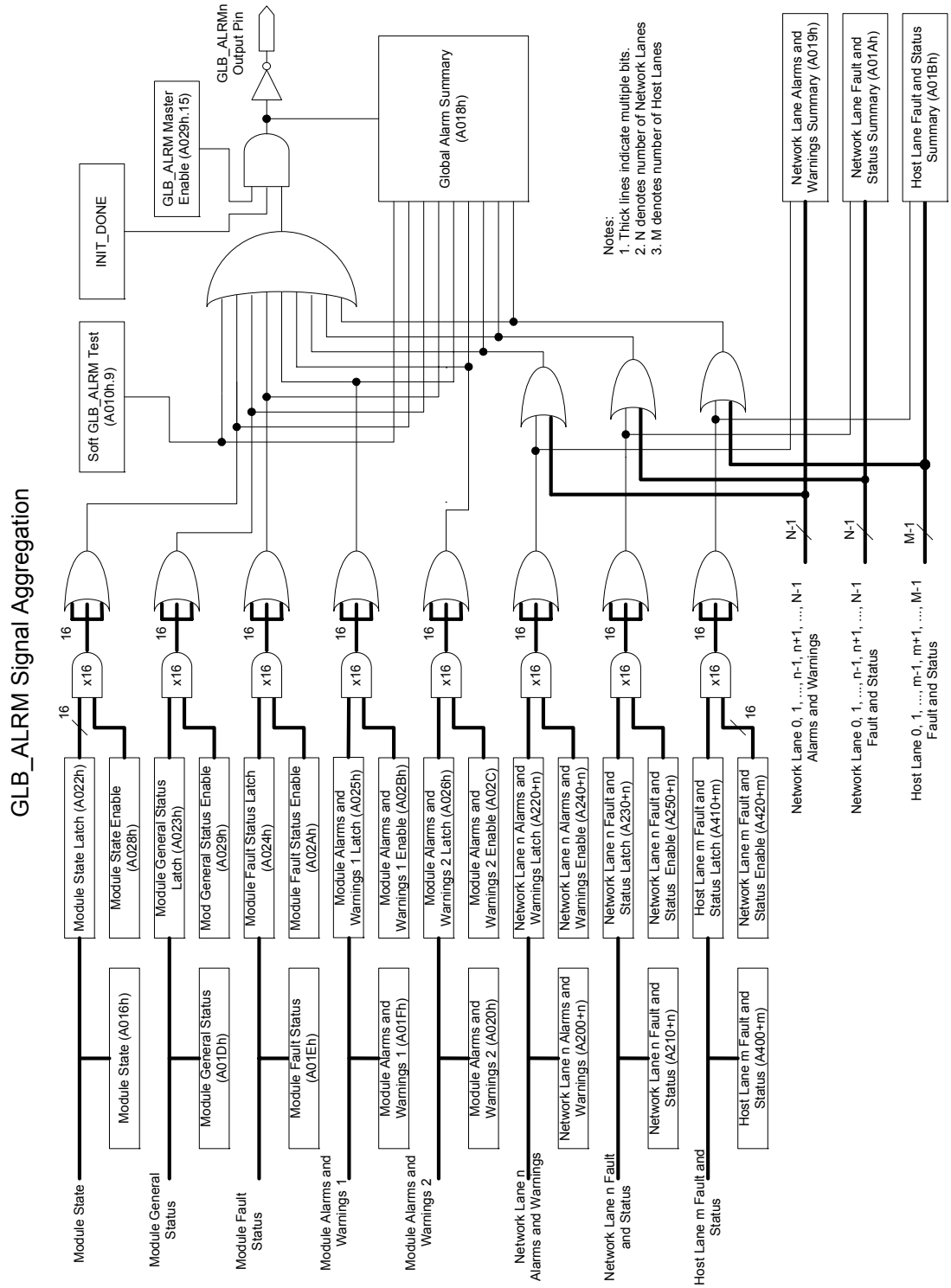
Notes:
1. “n” denotes the network lane index.
2. “N” is the total number of network lanes supported in a CFP module. The maximum value of N is 16.
3. “m” denotes the host lane index.
4. “M” is the total number of host lanes supported in a CFP module. The maximum value of M is 16.

*Table 7 Global Alarm Query Hierarchy*

| Query Level | CFP Register Name | CFP Register Addresses |
|---|---|---|
| 1 | Global Alarm Summary | A018h |
| 2 | Network Lane Alarms and Warnings Summary | A019h |
| 2 | Network Lane Fault and Status Summary | A01Ah |
| 3 | Network Lane Alarms and Warnings Latch, lane n | A220h + n, n = 0, 1, …, N-1. |
| 3 | Network Lane Fault and Status Latch, lane n | A230h + n, n = 0, 1, …, N-1. |
| 3 | Host Lane Fault and Status Latch, lane m | A410h + m, m = 0, 1, …, M-1. |

Notes:
1. “n” denotes the network lane index.
2. “N” is the total number of network lanes supported in a CFP module. The maximum N value is 16.
3. “m” denotes the host lane index.
4. “M” is the total number of host lanes supported in a CFP module. The maximum M value is 16.

*Figure 10 Global Alarm Signal Aggregation*



## 4.7 Specific Host Controls over Management Interface

### 4.7.1 Soft Module Reset (A010h.15) Function

Internal to CFP, this bit is logically OR'ed with both hardware pin MOD_RSTn and internally generated Vcc_Reset. This bit puts CFP module in Reset state when it is asserted by host. Once this bit is asserted by the Host it can only be cleared by CFP module. After a module reset caused by the assertion of this bit, CFP module exits Reset State if neither MOD_RSTn nor Vcc_Reset is asserted.

### 4.7.2 Soft Global Alarm Test (A010h.9) Function

This bit is provided for the host to forcibly assert the GLB_ALRM output, if desired. When GLB_ALRM function (refer to next paragraph) is enabled, asserting this control bit will assert the GLB_ALRM. This bit also directly feeds to Soft GLB_ALRM Test Status bit in Global Alarm Summary register for Host to verify the assertion of this bit.

The effect of this Soft Global Alarm Test bit can be verified by reading the GLB_ALRM State bit in Module General Status register. The GLB_ALRM Master Enable bit in Module General Status Enable register is provided as the master control to globally enable/disable GLB_ALRM. With this function Host does not need to change the settings of individual enable bits to disable the GLB_ALRM function.

## 4.8 Timing for Management Interface control and status reporting

Timing requirements for soft control, status functions and state transitions times are defined in *Table 8 Timing for Management Interface Control and Status*. For timing parameters related to the hard control and alarm pins refer to the CFP MSA Hardware Specification document.

*Table 8 Timing for Management Interface Control and Status*

| Item | Parameter | Min | Max[2] | Unit | Conditions |
|---|---|---|---|---|---|
| 1 | Soft Module Reset assert time | | 150 | ms | Time from Soft Module Reset asserted[1] until CFP module enters Reset state. |
| 2 | Soft TX Disable assert time | | 150 | ms | Time from the Soft TX Disable asserted[1] until all of the network lane optical (or electrical) outputs fall below 10% of nominal. |
| 3 | Soft TX Disable de-assert time | | 150 | ms | Time from Soft TX Disable de-asserted[1] until the CFP module enters the TX-Turn-on State. The actual TX on time is this time plus the Maximum TX-Turn-on Time stored in CFP Register 8073h. The TX on time is when all of the network lane optical (or electrical) outputs rise above 90% of nominal. |
| 4 | Soft Module Low Power assert time | | 150 | ms | Time from Soft Module Low Power asserted[1] until module enters High-Power-down state. The actual power down time is this time plus the Maximum |

| Item | Parameter | Min | Max[2] | Unit | Conditions |
|---|---|---|---|---|---|
| | | | | | High-Power-down Time stored in Register 8077h. The power down time is when the total module power consumption less than 2 Watts. |
| 5 | Soft Module Low Power de-assert time | | 150 | ms | Time from Soft Module Low Power de-asserted[1] until module enters High-Power-up State. |
| 6 | RX_LOS assert time | | 150 | ms | Time from hardware RX_LOS pin asserted to RX_LOS Pin State (in A01Dh) asserted. |
| 7 | RX_LOS de-assert time | | 150 | ms | Time from hardware RX_LOS pin de-asserted to RX_LOS Pin State de-asserted. |
| 8 | GLB_ALRMn assert time | | 150 | ms | Time from any condition of FAWS alarm/status state to GLB_ALRMn asserted. |
| 9 | GLB_ALRMn de-assert time | | 150 | ms | Time from last FAWS condition cleared to GLB_ALRMn de-asserted. |
| 10 | PRG_ALRM1 assert time | | 150 | ms | Time from programmed FAWS condition occurrence to PRG_ALRM1 asserted. |
| 11 | PRG_ALRM2 assert time | | 150 | ms | Time from programmed FAWS condition occurrence to PRG_ALRM2 asserted. |
| 12 | PRG_ALRM3 assert time | | 150 | ms | Time from programmed FAWS condition occurrence to PRG_ALRM3 asserted. |
| 13 | PRG_ALRM1 de-assert time | | 150 | ms | Time from programmed FAWS condition cleared to PRG_ALRM1 de-asserted. |
| 14 | PRG_ALRM2 de-assert time | | 150 | ms | Time from programmed FAWS condition cleared to PRG_ALRM2 de-asserted. |
| 15 | PRG_ALRM3 de-assert time | | 150 | ms | Time from programmed FAWS condition cleared to PRG_ALRM3 de-asserted. |
| 16 | PRG_CNTL1 assert time | | 150 | ms | Time from PRG_CNTL1 asserted to programmed function to take effect. |
| 17 | PRG_CNTL2 assert time | | 150 | ms | Time from PRG_CNTL2 asserted to programmed function to take effect. |
| 18 | PRG_CNTL3 assert time | | 150 | ms | Time from PRG_CNTL3 asserted to programmed function to take effect. |
| 19 | PRG_CNTL1 de-assert time | | 150 | ms | Time from PRG_CNTL1 de-asserted to the programmed function to cancel its effect. |
| 20 | PRG_CNTL2 de-assert time | | 150 | ms | Time from PRG_CNTL2 de-asserted to the programmed function to cancel its effect. |
| 21 | PRG_CNTL3 de-assert time | | 150 | ms | Time from PRG_CNTL3 de-asserted to the programmed function to cancel its effect. |
| 22 | MOD_FAULT assert time | | 150 | ms | Time from the conclusion of any fault condition occurrence to MOD_FAULT asserted |
| 23 | HIPWR_ON assert time | | 150 | ms | Time from module exiting High-Power-up state to HIPWR_ON asserted. |
| 24 | MOD_READY assert time | | 150 | ms | Time from module entering Ready state to MOD_READY asserted. |
| | 1. Measured from the conclusion of Host write transaction.<br>2. Note all the timing values are preliminary at the time of publication of this revision | | | | |

1

### 4.8.1 Miscellaneous Timing

*Table 9 Miscellaneous Timing* lists other timing parameters used in this Specification.

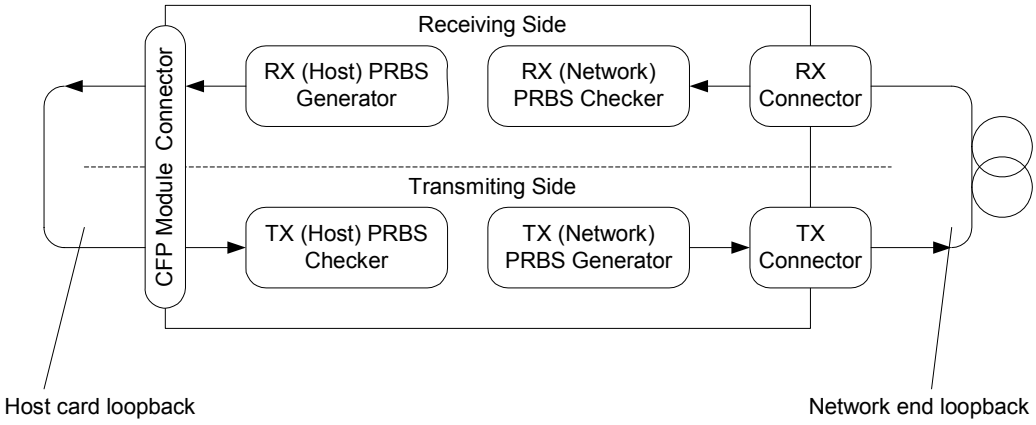
*Table 9 Miscellaneous Timing*

| Item | Parameter | Min | Max | Conditions | Reference Clause |
|---|---|---|---|---|---|
| 1 | T_refresh | - | 50 * (N+1) ms | DDM (A/D) data update rate. N = number of network lanes | 2.3d, 5.5.8 |
| 2 | T_assert | 100 us | - | Minimum h/w input assertion time | 4.1.1.5 |
| 3 | T_initialize | - | 2.5 s | From de-assertion of MOD_RSTs until the end of the Initialize State | 4.1.3.2 |
| 4 | T_high_power_up_max | - | Stored in NVR register 8072h | Max. time for the High-Power-up transient state to persist. | 5.1.46 |
| 5 | T_tx_turn_on_max | - | Stored in CFP NVR register 8073h | Max. time for the TX-Turn-on transient state to persist. | 5.1.47 |
| 6 | T_tx_turn_off_max | - | Stored in CFP NVR register 8076h | Max. time for the TX-Turn-off transient state to persist. | 5.1.50 |
| 7 | T_high_power_down_max | - | Stored in CFP NVR register 8077h | Max. time for the High-Power-down transient state to persist. | 5.1.51 |

## 4.9 Bit Error Rate Calculation

Optionally CFP module may have built-in PRBS generators and checkers. *Figure 11 CFP Built-in PRBS Components and Test Signal Flow* illustrates the relationship between these components and a loopback based test signal flow.

*Figure 11 CFP Built-in PRBS Components and Test Signal Flow*




### 4.9.1 Network Lane PRBS Setup

CFP MSA specifies optional PRBS generator and error checker for each network lane with CFP register controls. To start a PRBS session, Host shall select the desired PRBS pattern by setting the bits TX PRBS Pattern 1 and TX PRBS Pattern 0 in Network Lane TX Control register (A011h.13~12). The Host enables the PRBS generators by asserting the bit TX PRBS Generator Enable in the same register (A011h.14).

Host shall apply the same operation to Network Lane RX Control register correspondingly to set up and enable the PRBS checker. The PRBS generator and checker functions shall be stopped by de-asserting the TX PRBS Generator Enable and the RX PRBS Checker Enable (A012h.14), respectively.

### 4.9.2 Network Lane BER Calculation

Upon assertion of RX PRBS Enable bit CFP module shall automatically set the Network Lane PRBS Data Bit Count and Network Lane PRBS RX Error Count (each per lane) to zero and shall start the accumulation. CFP module shall stop the accumulations for both data bit counting and error bit counting after RX PRBS Checker Enable is de-asserted. The counts shall be kept unchanged until RX PRBS Checker Enable is asserted next time.

The Host can read the Network Lane PRBS Data Bit Count and the per-lane Network Lane PRBS RX Error Count at any time. The bit error rate (BER) can be calculated by simply

dividing the RX error count by data bit count. To achieve an accurate BER calculation, it is recommended that the Host reads these registers after PRBS Enable is de-asserted.

Both Network Lane PRBS Bit Count and Network Lane PRBS Error Count registers use an ad-hoc floating data format with 6-bit unsigned exponent and 10-bit unsigned mantissa. While the maximum count of this ad-hoc floating point number is 1023*2^63 ~= 2*73, CFP MSA specifies the effective maximum count to be 2^64 – 1 with a precision of 1/1024 in using this ad-hoc data format. Some examples in this data format are listed in *Table 10*.

*Table 10 CFP Ad-hoc Floating Point Number Examples*

| Count N (integer) | Mantissa (M) | Exponent (E) | Value Expression |
|---|---|---|---|
| 0 ~ 1023 | N | 0 | N * 2^0 |
| 1024 ~ 2047 | N/2 | 1 | (N/2) * 2^1 |
| 2048 ~ 4095 | N/4 | 2 | (N/4) * 2^2 |
| 4096 ~ 8191 | N/8 | 3 | (N/8) * 2^3 |

### 4.9.3 Host Lane PRBS Control

Host lane PRBS control is specified similar to that of network lane. The mechanism applies to RX PRBS Pattern 1 and RX PRBS Pattern 0 in Host Lane Control register (A014h.6~5). The Host enables the PRBS generators by asserting the bit RX PRBS Generator Enable in the same register (A014h.7).

Host shall apply the same operation to Host Lane Control register (A014h.13~12 and A014h.14) correspondingly to set up and enable the PRBS checker. The host side PRBS generator and checker functions shall be stopped by de-asserting the RX PRBS Generator Enable and the TX PRBS Checker Enable respectively.

### 4.9.4 Host Lane BER Calculation

BER calculation for host lane is similar to that of network lane. In calculation, the Host shall use the Host Lane PRBS Data Bit Count register at A039h and the Host Lane PRBS TX Error Count registers at A430h through A43Fh.

## 4.10 CFP Register Access

### 4.10.1 Read and Write Accesses

Host shall have the read access to the registers or register bits that have Access Type of RO, RW, and COR on Page 8000h and on Page A000h.

Host shall have write access to the CFP registers or register bits that have Access Type of RW and WO on Pages 8000h and A000h Host writes to User NVRs resulted in volatile values which are stored in shadow registers.

Both Read and Write operations are conducted by directly using MDIO Command Frames.

### 4.10.2 User NVR Restore and Save Functions

To write permanently to User NVR registers Host shall use the "Save" function to store the shadowed data into underlying NVM. The host only needs to perform a single Save operation to copy the entire User NVR shadow registers to the underlying NVM after finishing the editing the data. CFP MSA further specifies the minimum number of Save operation greater than 10,000 times.

Upon power-up or reset the User NVR shadow registers are "Restored" with NVM values. Restore function is also called to update the User NVR shadow registers with previously stored NVM values if the edited content of User NVRs is not desired. Note that the Restore function will overwrite the NVR shadow registers, losing any host-written values in them that have occurred since the last Save to the underlying NVM.

The NVR Access Control Register (A004h) provides the Restore and Save functions for Host to restore and save the User NVRs content. This register has a structure described in *Table 11 User NVRs Access Control Register (A004h)* and *Table 22 CFP Module VR 1*.

*Table 11 User NVRs Access Control Register (A004h)*

| Access Type | Bit | Bit Field Name | Description | Init Value |
|---|---|---|---|---|
| RW | 15:9 | Reserved | Vendor specific | 0 |
| RO | 8:6 | Reserved | | 0 |
| RW[1] | 5 | Command[2] | 0: Restore User NVRs<br>1: Save User NVRs | 0 |
| RO | 4 | Reserved | | 0 |
| RO | 3~2 | Command Status | 00b: Idle,<br>01b: Command completed successfully,<br>10b: Command in progress,<br>11b: Command failed. | 00b |
| RW[1] | 1~0 | Extended Command | 00b ~ 10b: Vendor specific,<br>11b: Restore/Save all User NVRs. | 00b |

1. Once a command has been invoked the values written to the "Command" and "Extended Command" bits are held until the RSC state machine transitions back to the idle state.
2. User writes to the User NVRs Access Control Register are not valid, except if an idle state is observed in Command Status. A read of this register after command completes is required to return to idle (reverts command status to 00b. Further commands should be issued without returning to idle.

#### 4.10.2.1 User NVR Restore and Save Command (Bit 5)

Bit 5 in NVR Access Control Register is designated for User NVR restore and save command (RSC). The execution of RSC is illustrated by *Figure 12 Restore and Save Command Execution State Diagram*. In an idle state any write transaction to the NVR Access Control Register shall initiate a User NVR transaction. A "0" written to bit 5 initiates

a User NVR Restore. A "1" written to bit 5 initiates a User NVR Save. The extended command bits (1 and 0) determine the exact nature of the Save/Restore operation.

Only one command on User NVRs can execute at a time. If a command is initiated, the Command Status bits indicate "Command in Progress" in NVR Access Control Register and further writes to the NVR Access Control Register will be ignored.

A Soft Module Reset will be queued to avoid crashing the User NVRs and NVM. The Host should always read the NVR Access Control Register to ensure that Command Status is not set to Command In Progress before attempting to assert the MOD_RSTs.

#### 4.10.2.1.1 Restore and Save Command State Definitions

*Table 12 Restore and Save Command State Definitions* defines the four states in the execution of RSC transitions.

*Table 13 Restore and Save Command State Transitions* further defines the RSC state transitions when a Restore or Save command is executed.

*Table 12 Restore and Save Command State Definitions*

| RSC STATE | When Entered |
|---|---|
| IDLE | Default state when no Save/Restore user NVRs are in progress. |
| CMD_PENDING | State where command is pending availability of system resources, |
| IN_PROGRESS | State assumed while User NVR restore or User NVR save is in process |
| CMD_COMPLETE | State assumed after User NVR restore or User NVR save has occurred but before outcome has been read from the Command Status bits. |

*Table 13 Restore and Save Command State Transitions*

| RSC State Transition | Invocation |
|---|---|
| From IDLE to CMD_PENDING | Initiated by a write to the NVR Access Control Register. |
| From CMD_PENDING to IN_PROGRESS | Occurs when system resources are free to execute the requested command. |
| From IN_PROGRESS to CMD_COMPLETE | Initiated by the NVR logic indicating that a User NVR restore or User NVR save operation has been completed. |
| From CMD_COMPLETE to IDLE | Initiated by a read of the NVR Access Control Register. |

#### 4.10.2.1.2 State Machine Function Definitions

The RSC state machine function definitions used in *Figure 12 Restore and Save Command Execution State Diagram* are as follows.

wr_A004h = MDIO write to NVR Access Control Register (A004h)
rd_A004h = MDIO read from NVR Access Control Register
exec( cmd_code ) = perform command indicated by "cmd_code"

"cmd_code" defined by combination of bit 5 and bit 1:0 of NVR Access Control Register, or in the case of reset, it is "reset User NVR".

#### 4.10.2.2 Command Status (bits 3, 2)

Following a write to register A004h (initiation of Restore/Save command), bits 3 and 2 provide information on the status of the command. A value of 00b indicates an idle condition, 10b indicates that a command is pending or in progress, 01b indicates that the command completed successfully, and 11b indicates that the command failed.

#### 4.10.2.3 Extended Commands (bits 1, 0)

The register bits 1 and 0 supplement the basic RSC (bit 5) function. A value of 11b restores and saves all User NVR contents. All other values implement vendor specific commands.

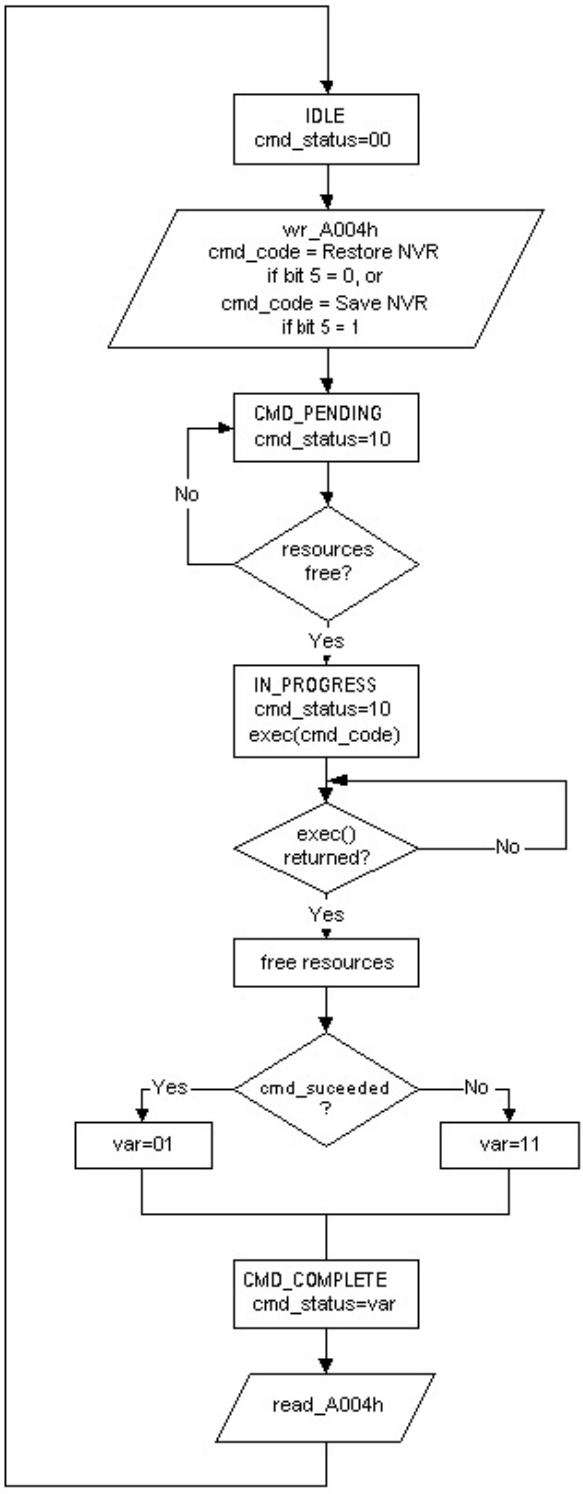
#### 4.10.2.4 NVR Data Safety in Save Function

The following conditions and measures shall be considered to avoid corrupting the user NVR when a Save command is performed.

a) After a Save command is issued, the Host shall wait until the Command Status = Command Complete before performing any one of the operations of shutting down VCC, asserting MOD_RSTn, and asserting Soft Module Reset, otherwise the incomplete execution of Save command or NVR data corruption will be resulted.
b) The Host shall not expect a Save command to be accepted or executed when it is issued with a CFP module in Reset state or in Initialize state. When the module is in Fault state, it may or may not be able to complete the Save Command successfully, depending upon the nature of the fault.
c) Caution should be taken when hot-un-plug the CFP module as described in 4.3.4 "Example of Module Turn-off Sequence". The sequence by the Host and by the CFP module cannot prevent the user NVR data corruption if a Save command is in progress and the module is hot-un-plugged by a user.

*Figure 12 Restore and Save Command Execution State Diagram*



## 4.11 Setup of Programmable Control and Alarm Pins

### 4.11.1 Programmable Control Functions for PRG_CNTLs

Each programmable control pin can be programmed with the functions defined in *Table 14 Programmable Control Functions*.

*Table 14 Programmable Control Functions*

| NAME | FUNCTION | VALUE |
|---|---|---|
| TRXIC_RSTn | Reset TX and RX ICs, PRG_CNTL1 MSA default. | 0: Normal,<br>1: Assign TRXIC_RSTn function to any of the 3 hardware pins PRG_CNTL3, PRG_CNTL2, and PRG_CNTL1. When so assigned these hardware pins use the active low logic, that is, 0 = Assert (Reset). Note that when so assigned, their soft counterparts Soft PRG_CNTL3, Soft PRG_CNTL2, and Soft PRG_CNTL1 (A010h.12~10) use an active high logic, that is, 1 = Assert (Reset). |

### 4.11.2 Programmable Alarm Sources for PRG_ALRMs

Each programmable alarm pin can be programmed with the alarm sources defined in *Table 15 Programmable Alarm Sources*.

*Table 15 Programmable Alarm Sources*

| NAME | ALARM SOURCE | VALUE |
|---|---|---|
| HIPWR_ON | Module high-power-on indicator. PRG_ALRM1 MSA default. | 0: Module not high powered up,<br>1: Module high power up completed. |
| MOD_READY | MOD_READY, module startup sequence done, PRG_ALRM2 MSA default. | 0: Not done,<br>1: Done. |
| MOD_FAULT | Fault detected. PRG_ALRM3 MSA default. | 0: No Fault,<br>1: Fault. |
| RX_ALRM | Receive path alarm = RX_LOS + RX_LOL. | 0: No receive path alarm,<br>1: Receive path alarm asserted. |
| TX_ALRM | Transmit path alarm = TX_LOSF + TX_HOST_LOL + TX_CMU_LOL. | 0: No transmit path alarm,<br>1: Transmit path alarm asserted. |
| RX_LOL | RX IC Lock Indicator. | 0: Locked,<br>1: Loss of lock. |
| TX_LOSF | Transmitter Loss of Signal Functionality. | 0: All transmitter signals functional,<br>1: Any transmitter signal not functional |
| TX_LOL | TX IC Lock Indicator. | 0: Locked,<br>1: Loss of lock. |
| OOA | Host lane skew out of alignment indicator. | 0: No OOA,<br>1: Out of alignment. |

# 5 CFP REGISTER DESCRIPTION

The detailed CFP register descriptions are listed in *Table 18 CFP NVR 1* through *Table 25 Host Lane VR 1*. Each table has 7 columns with the following definition.

*Table 16 Table Column Description*

| Column | Description |
|---|---|
| Hex Addr. | MDIO address in hex number format For multi-register Data Field, it represents the lowest address of the field. |
| Size | Number of CFP registers in a given Data Field. |
| Access Type | RO = Read Only; RW = Read and Write; LH = Latched High[1]; COR = Clear On Read[2]; SC = Self Clearing. |
| Bit | This field indicates the range of bits used for a particular field in the format of m~n, where m is starting high bit and n is the ending low bit. |
| Register Name | This is the name of a register. Full English words are used for maximum clarity. Acronym use is minimized. |
| Bit Field Name | This is the name of a specific bit data field. Full English words are used for maximum clarity. Acronym use is minimized. Normally in non-bold face. |
| Description | Details of each Register field and/or behavior of a bit. |
| LSB Unit | This column contains the unit of a physical quantity represented by the least significant bit of the register field. |
| Init Value | The initial value that each volatile registers takes after the module boots up or is reset. |

1. Latch registers are set on the rising edge of the associated status signals.
2. Clear-on-Read bits are cleared to 0 upon Host-read, independent of the condition of the (unlatched) status signal.

## 5.1 CFP NVR 1 Table: Base ID Registers

### 5.1.1 Module Identifier (8000h)

For CFP MSA compliant modules, this value shall be 0Eh. Other module form factors used in the industry are identified with other values. For details, please refer to CFP NVR Table 1.

### 5.1.2 Extended Identifier (8001h)

It provides additional information about CFP module.

#### 5.1.2.1 Power Class

As outlined in the CFP MSA Hardware Specification, there are four power classes identified for the CFP MSA. The power classes are provided to allow the host to identify the power requirements of the module and determine if the system is capable of providing and dissipating the specified power class. For a more detailed description, please refer to the CFP MSA Hardware Specification.

#### 5.1.2.2 Lane Ratio Type

The CFP module shall support network interfaces which may comply with various physical interfaces such as IEEE PMD, SONET/SDH, OTN or that from other standards body. For example, 100GBASE-LR4 network interface corresponds to the optical PMD specified in IEEE clause 88. The CFP module shall also support the Host interface which is instantiated as an electrical interface with multiple lanes operating at a nominal 10Gbps.

#### 5.1.2.3 WDM Type

It shall identify any optical grid spacing which is in use by the CFP module.

### 5.1.3 Connector Type Code (8002h)

It shall identify the connector technology used for the network interface. Early iterations of the CFP MSA have identified SC optical connectors, and it is expected that further connectors will be identified.

### 5.1.4 Ethernet Application Code (8003h)

It shall identify what if any Ethernet PMD application is supported. Any CFP module which supports an application not including Ethernet such as SONET/SDH, OTN, Fiber Channel or other, shall record a 00h to signify that the Ethernet application is undefined. Any CFP module which supports an application which includes Ethernet and additional applications such as SONET/SDH, OTN, Fiber Channel or other, shall record the value in Ethernet Application Code corresponding to the supported Ethernet application.

### 5.1.5 Fiber Channel Application Code (8004h)

It shall identify what if any Fiber Channel PMD application is supported. Any CFP module which supports an application not including Fiber Channel such as SONET/SDH, OTN, Ethernet or other, shall record a 00h to signify that the Fiber Channel application is undefined. Any CFP module which supports an application which includes Fiber Channel and additional applications such as SONET/SDH, OTN, Ethernet or other, shall record the value in Fiber Channel Application Code corresponding to the supported Fiber Channel application.

### 5.1.6 Copper Link Application Code (8005h)

In this CFP register, the CFP module shall identify what if any non-Ethernet Copper based PMD application which is supported. At the time of the writing, this application is undefined.

### 5.1.7 SONET/SDH Application Code (8006h)

It shall identify what if any SONET/SDH PMD application is supported. Any CFP module which supports an application not including SONET/SDH such as Ethernet, OTN, Fiber Channel or other, shall record a 00h to signify that the SONET/SDH application is undefined. Any CFP module which supports an application which includes SONET/SDH and additional applications such as Ethernet, OTN, Fiber Channel or other, shall record the

value in SONET/SDH Application Code corresponding to the supported SONET/SDH application.

### 5.1.8 OTN Application Code (8007h)

It shall identify what if any OTN PMD application is supported. Any CFP module which supports an application not including OTN such as SONET/SDH, Ethernet, Fiber Channel or other, shall record a 00h to signify that the OTN application is undefined. Any CFP module which supports an application which includes OTN and additional applications such as SONET/SDH, Ethernet, Fiber Channel or other, shall record the value in OTN Application Code corresponding to the supported OTN application.

### 5.1.9 Additional Capable Rates Supported (8008h)

### 5.1.10 Number of Lanes Supported (8009h)

The network lane number assignment shall always start from 0h and end with the number of lanes supported minus one, with no number skipped in between. This shall be applicable to both network and host lanes whether the lane numbers are different or the same. For example, a serial network lane implementation shall use lane 0 and a 4 network lane PMD shall use lane number 0 ~ 3. A CAUI host interface shall use lane numbers 0 ~ 9.

#### 5.1.10.1 Number of Network Lanes

It is a 4-bit number representing the number of network data I/O supported in this module. The value of 0 represents 16 network data I/O supported. The values of 1 through 15 represent the actual number of network lanes supported.

#### 5.1.10.2 Number of Host Lanes

It is a 4-bit number representing the number of host data I/O supported in this module. The value of 0 represents 16 host data I/O supported. The values of 1 through 15 represent the actual number of host lanes supported.

### 5.1.11 Media Properties (800Ah)

#### 5.1.11.1 Media Type

It shall identify the type of transmission media for the supported application using bits 7~6.

#### 5.1.11.2 Directionality

It shall identify if supported application uses the same transmission media for the transmit/receive network interfaces (Bi-Directional) or if separate transmission media are required for transmit and receive network interfaces, respectively.

#### 5.1.11.3 Optical Multiplexing and De-Multiplexing

It shall identify if optical multiplexing and optical de-multiplexing are supported within the CFP module.

#### 5.1.11.4 Active Fiber per Connector

It shall identify the number of active TX/RX fiber pairs in an optical connector. For example, a CFP module supporting the 100GBASE-SR10 application using an MPO connector shall report 10 in Active Fiber per Connector.

### 5.1.12 Maximum Network Lane Bit Rate (800Bh)

It shall identify maximum data rate supported per network lane. For more complex modulation schemes than OOK (on/off keying), the value reported shall be the bit rate and not the baud rate. The value shall be based upon units of 0.2 Gbps. A value of 0h is considered undefined.

### 5.1.13 Maximum Host Lane Bit Rate (800Ch)

It shall identify maximum data rate supported per host lane. The value shall be based upon units of 0.2 Gbps. The nominal lane rate suggested in the CFP MSA HW Specification is 10Gbps. However, various applications such as support for OTU4 and future applications will require higher lane rates. A value 0h is considered undefined.

### 5.1.14 Maximum Single Mode Optical Fiber Length (800Dh)

It shall identify the specified maximum reach supported by the application for transmission over single mode fiber. The value shall be based upon units of 1km. For applications which operate over compensated transmission systems, it is suggested to enter an undefined value. A value of 0h is considered undefined.

### 5.1.15 Maximum Multi-Mode Optical Fiber Length (800Eh)

It shall identify the specified maximum reach supported by the application for transmission over OM3 multi-mode fiber. The value shall be based upon units of 10 m. A value of 0h is considered undefined.

### 5.1.16 Maximum Copper Cable Length (800Fh)

The module shall identify the specified maximum reach supported by the application for transmission over copper cable. The value shall be based upon units of 1 m. A value of 0h is considered undefined.

### 5.1.17 Transmitter Spectral Characteristics 1 (8010h)

#### 5.1.17.1 Number of Active Transmit Fibers

Bits 4~0 are a value identifying the number of active optical fiber outputs supported. The value 0 represents 0 active transmit fibers (i. e., receive-only), copper or undefined. The values of 1 through 31 represent the actual number of active transmit fibers. For example, the value for 100GBASE-SR10 is 10.

### 5.1.18 Transmitter Spectral Characteristics 2 (8011h)

#### 5.1.18.1 Number of Wavelengths per Active Transmit Fiber

Bits 4~0 are a value representing the number of wavelengths per active transmit fiber. The value 0h represents an 850 nm multimode source or undefined. The values 1 through 31 represent the actual number of wavelengths per transmit fiber. For example, the value for 100GBASE-LR4 is 4.

### 5.1.19 Minimum Wavelength per Active Fiber (8012h, 8013h)

It is a 16-bit unsigned value data field and shall identify the minimum wavelength, in the unit of 25 pm, of any supported optical fiber output per the application. For an example, the value for 100GBASE-LR4 with a minimum specified wavelength of 1294.53 nm would be CA45h. A value of 0 indicates a multimode source or undefined.

### 5.1.20 Maximum Wavelength per Active Fiber (8014h, 8015h)

It is a 16-bit unsigned value data field and shall identify the maximum wavelength, in the unit of 25 pm, of any supported optical fiber output per the application. For an example, the value for 100GBASE-LR4 with a maximum specified wavelength of 1310.19 nm would be CCB8h. A value of 0 indicates a multimode source or undefined.

### 5.1.21 Maximum per Lane Optical Width (8016h, 8017h)

It shall identify the maximum network lane optical wavelength width, in the unit of 1pm, of any supported optical fiber output per the application. For an example, the value for 100GBASE-LR4 with a maximum specified optical wavelength width of 2.1nm for network lane $L_3$ would be 834h. A value of 0 indicates a multimode source or undefined.

### 5.1.22 Device Technology 1 (8018h)

#### 5.1.22.1 Laser Source Technology

It shall identify the type of laser technology which is used. There is a CFP register value for electrical/copper (non-laser) transmission, as well as additional reserved space for as of yet undefined laser types.

#### 5.1.22.2 Transmitter Modulation Technology

It shall identify the type of modulation technology used. This is a 4-bit unsigned value representing commonly used modulation technologies with reserved values to represent for as of yet undefined modulator types.

### 5.1.23 Device Technology 2 (8019h)

Several data fields in this register are related to tunable transmitters. However the full support of tunability is not fully covered in the Draft. It shall be supported either in the future release of this draft or in a follow-up MSA.

#### 5.1.23.1 Wavelength Control

It shall identify if the wavelength of the laser technology which is used includes an active wavelength control mechanism. Active wavelength control mechanism is defined to be a wavelength sensitive device which can be used to compare the actual transmitted wavelength from the expected transmitted wavelength. The value of 0b signifies no control mechanism and 1b signifies the presence of such a mechanism within the CFP module.

#### 5.1.23.2 Cooled Transmitter

It shall identify if the transmitter is coupled to a cooling mechanism within the module. A popular implementation for such a coupled cooling mechanism is to mount a laser such that it is thermally coupled to a thermoelectric cooler which is controlled to keep the laser within a defined temperature range. If any cooling mechanism is present the transmitter is considered to be cooled. A transmitter is considered to be cooled even if the cooling mechanism is not always active. The value of 0b signifies no cooling mechanism and 1b signifies the presence of such a cooling mechanism within the CFP module.

#### 5.1.23.3 Tunability

It shall identify if the transmitted optical wavelength may be tuned over a specified spectral range. The value of 0b signifies no tuning mechanism and 1b signifies the presence of such a tuning mechanism within the CFP module.

#### 5.1.23.4 VOA Implemented

It shall identify if the optical receiver implements a variable optical attenuator (VOA) within the optical receive chain. The value of 0b signifies no VOA mechanism and 1b signifies the presence of such a VOA mechanism within the CFP module.

#### 5.1.23.5 Detector Type

It shall identify the type of detector technology which is used. There is a CFP register value for undefined detector types.

#### 5.1.23.6 CDR with EDC

It shall identify if the Clock and Data Recovery (CDR) circuitry within the CFP module receive path contains any electronic dispersion compensation (EDC) techniques to improve the receiver performance. It is recognized that there exist a variety of EDC techniques with varying performance enhancements and tradeoffs – this CFP register does not convey any detail, only if the CFP module implements EDC within the receiver. The value of 0b signifies no EDC mechanism and “1” signifies the presence of such an EDC mechanism within the CFP module.

### 5.1.24 Signal Code (801Ah)

#### 5.1.24.1 Modulation

It shall identify the polarity coding used in the optical modulation. A value of 0b is considered undefined.

#### 5.1.24.2 Signal Coding

It shall identify the signaling coding used in the optical modulation. A value of 0b is considered undefined.

### 5.1.25 Maximum Total Optical Output Power per Connector (801Bh)

It shall identify the maximum optical output power of any supported optical fiber output per the application. A value of 0h is considered undefined.

### 5.1.26 Maximum Optical Input Power per Network Lane (801Ch)

It shall identify the maximum optical input power of any supported optical fiber input per the application. A value of 0h is considered undefined.

### 5.1.27 Maximum Power Consumption (801Dh)

It shall identify the maximum power consumption of any supported application. A value of 0h is considered undefined.

### 5.1.28 Maximum Power Consumption in Low Power Mode (801Eh)

It shall identify the maximum power consumption of the low power mode state. The low power mode state is described in detail in the CFP MSA Hardware specification. A value of 0h is considered undefined.

### 5.1.29 Maximum Operating Case Temp Range (801Fh)

It shall identify the maximum operating case temperature specified of any supported application. It is a signed 8-bit value expressed in two's-complement, representing a total range from -127 to +127 in increments of 1 degree C'. The value -128 (80h) indicates the value is not defined.

### 5.1.30 Minimum Operating Case Temp Range (8020h)

It shall identify the minimum operating case temperature specified of any supported application. It is a signed 8-bit value expressed in two's-complement, representing a total range from -127 to +127 in increments of 1 degree C'. The value -128 (80h) indicates the value is not defined.

### 5.1.31 Vendor Name (8021h)

It shall identify the CFP module Vendor name in ASCII code. The vendor name is a 16 byte field that contains ASCII characters, left aligned and padded on the right with ASCII spaces (20h). The vendor name shall be the full name of the corporation, a commonly accepted abbreviation of the name or the stock exchange code for the corporation. Vendor is the CFP module vendor.

### 5.1.32 Vendor OUI (8031h)

It is a 3 byte field that contains the IEEE Company Identifier for CFP module vendor (as opposed to the OUI of any third party ICs which may be used therein). Bit order for the OUI follows the format of IEEE 802.3 Clause 22.2.4.3.1 and is therefore reversed in comparison to other NVRs. A value of all zero in the 3 byte field indicates that the Vendor OUI is unspecified. Vendor is the CFP module vendor.

### 5.1.33 Vendor Part Number (8034h)

It is a 16 byte field that contains ASCII characters, left aligned and padded on the right with ASCII spaces (20h), defining the vendor part number or product name. A value of all zero in the 16 byte field indicates that the Vendor Part Number is unspecified. Vendor is the CFP module vendor.

### 5.1.34 Vendor Serial Number (8044h)

It is a 16 byte field that contains ASCII characters, left aligned and padded on the right with ASCII spaces (20h), defining the vendor's serial number. A value of all zero in the 16 byte field indicates that the Vendor SN is unspecified. Vendor is the CFP module vendor.

### 5.1.35 Date Code (8054h)

It is an 8 byte field that contains the vendor's date code in ASCII characters. A value of all zero in the 8 byte field indicates that the Vendor date code is unspecified. Vendor is the CFP module vendor.

*Table 17 Date Code Example*

| CFP Register | Date Value Example of March 10, 2009.<br>(Bit 7 = MSB, bit 0 = LSB) |
|---|---|
| 8054 | 32h ('2') |
| 8055 | 30h ('0') |
| 8056 | 30h ('0') |
| 8057 | 39h ('9') |
| 8058 | 30h ('0') |
| 8059 | 33h ('3') |
| 805A | 31h ('1') |
| 805B | 30h ('0') |

### 5.1.36 Lot Code (805Ch)

It is a 2-byte field that contains the vendor's lot code in ASCII characters. A value of all zero in the 2-byte field indicates that the Vendor lot code is unspecified. Vendor is the CFP module vendor.

### 5.1.37 CLEI Code (805Eh)

It is a 10 byte field that contains the Common Language Equipment Identifier code in ASCII characters. A value of all zero in the 10 byte field indicates that the CLEI code is unspecified.

### 5.1.38 CFP MSA Hardware Specification Revision Number (8068h)

It indicates the CFP MSA hardware specification version number supported by the transceiver. This 8-bit value represents the version number times 10. This yields a max of 25.5 revisions.

### 5.1.39 CFP MSA Management Interface Specification Revision Number (8069h)

It indicates the CFP MSA Management specification version number supported by the CFP module. This 8-bit value represents the version number times 10. This yields a max of 25.5 revisions.

### 5.1.40 Module Hardware Version Number (806Ah)

It is a 2-byte number in the format of x.y with x at lower address and y at higher address. In each register this 8-bit value represents the version number from 0 to 255. A value of all zero in this 2-byte field indicates that the vendor HW version number is unspecified.

### 5.1.41 Module Firmware Version Number (806Ch)

It is a 2-byte field in the format of “x.y”. The “x” value is contained within the lower address. The “y” value is contained in the upper address. In each register this 8-bit value represents the release number from 0 to 255. A value of all zero in this 2-byte field indicates that the vendor FW version number is unspecified.

### 5.1.42 Digital Diagnostic Monitoring Type (806Eh)

It is a one byte field with 8 single bit indicators describing how DDM functions are implemented in CFP module.

### 5.1.43 Digital Diagnostic Monitoring Capability 1 (806Fh)

It describes DDM functions implemented at CFP module level (not lane specific). This MSA draft specifies 4 A/D inputs, transceiver SOA bias current monitor, transceiver power supply voltage monitor, transceiver internal temperature monitor, and transceiver case temperature monitor. The last quantity, transceiver case temperature monitor is intended for supplying an additional monitor to transceiver internal temperature monitor. The definition and implementation of case temperature is left to be specified by vendor datasheet.

### 5.1.44 Digital Diagnostic Monitoring Capability 2 (8070h)

It describes DDM functions implemented at network lane level.

### 5.1.45 Module Enhanced Options (8071h)

It describes enhanced optional functions implemented in CFP module. Refer to register description for details.

### 5.1.46 Maximum High-Power-up Time (8072h)

It is for a vendor defined parameter which specifies the maximum time to transit the "High-Power-up" state shown in *Figure 3 State Transition Diagram during Startup and Turn-off*. The Host may use this value as the time-out value. It is an unsigned 8-bit value * 1 second. Use 1 second if the actual time is less than one second.

### 5.1.47 Maximum TX-Turn-on Time (8073h)

It is for a vendor defined parameter which specifies the maximum time to transit the "TX-Turn-on" state shown in *Figure 3 State Transition Diagram during Startup and Turn-off*. The Host may use this value as the time-out value. It is an unsigned 8-bit value in units of 1 second. Use 1 second if the actual time is less than 1 second.

### 5.1.48 Host Lane Signal Spec (8074h)

It specifies the host lane signal type a module supports. Refer to register description for details.

### 5.1.49 Heat Sink Type (8075h)

It identifies if the top surface of the CFP module has a flat top or integrated heat sink. The CFP MSA supports various networking applications which may require different thermal management solutions. The default top surface of the CFP module is a flat top, however, some networking applications will benefit from an integrated heat sink. An integrated heat sink complies with the total module height requirements and shall not disrupt, disable nor damage any riding heat sink system. For further details, refer to the CFP MSA Hardware specification.

### 5.1.50 Maximum TX-Turn-off Time (8076h)

It is for a vendor defined parameter which specifies the maximum time to transit the "TX-Turn-off" state shown in *Figure 3 State Transition Diagram during Startup and Turn-off*. The Host may use this value as the time-out value. It is an unsigned 8-bit value in units of ms. Use 1 ms if the actual time is less than 1 second.

### 5.1.51 Maximum High-Power-down Time (8077h)

It is for a vendor defined parameter which specifies the maximum time to transit the "High-Power-down" state shown in *Figure 3 State Transition Diagram during Startup and Turn-off*. The Host may use this value as the time-out value. It is an unsigned 8-bit value * 1 second. Use 1 second if the actual time is less than one second.

### 5.1.52 Module Enhanced Options 2 (8078h)

It describes the second enhanced optional functions implemented in CFP module. Refer to register description for details.

### 5.1.53 Transmitter Monitor Clock Options (8079h)

This register contains the transmitter monitor clock option bits. The clock is intended to be used as a reference for measurements of the optical output. If provided, the clock shall operate at a rate relative to the optical lane rate of 1/16 rate for 40Gbit/s applications and a 1/8 rate of 25Gbit/s for 100Gbit/s applications. Another option is a clock at 1/16 or 1/64 the rate of transmitter electrical input data.

### 5.1.54 Receiver Monitor Clock Options (807Ah)

This register contains the receiver monitor clock option bits. The clock is intended to be used as a reference for measurements of the optical input. If provided, the clock shall operate at a rate relative to the optical lane rate of 1/16 rate for 40Gbit/s applications and a 1/8 rate of 25Gbit/s for 100Gbit/s applications. Another option is a clock at 1/16 or 1/64 the rate of transmitter electrical input data.

### 5.1.55 Module Enhanced Options 3 (807Bh)

It describes the third enhanced optional functions implemented in CFP module. Refer to register description for details.

### 5.1.56 CFP NVR 1 Checksum (807Fh)

It is the 8 bit unsigned result of the checksum of all of the CFP register LSB contents from addresses 8000h to 807Eh inclusive. Note that all the reserved registers have zero value contribution to the calculation of this Checksum.

*Table 18 CFP NVR 1*

| CFP NVR 1 | | | | | | |
|---|---|---|---|---|---|---|
| ***Hex Addr*** | ***Size*** | ***Access Type*** | ***Bit*** | ***Register Name*** *Bit Field Name* | ***Description*** | ***LSB Unit*** |
| ***Base ID Information*** | | | | | | |
| **8000** | **1** | **RO** | **7~0** | **Module Identifier** | **00h: Unknown or unspecified,<br>01h: GBIC,<br>02h: Module/connector soldered to motherboard,<br>03h: SFP,<br>04h: 300 pin XSBI,<br>05h: XENPAK,<br>06h: XFP,<br>07h: XFF,<br>08h: XFP-E,<br>09h: XPAK,<br>0Ah: X2,<br>0Bh: DWDM-SFP,<br>0Ch: QSFP,<br>0Dh: QSFP+,<br>0Eh: CFP,** | **N/A** |

| CFP NVR 1 | | | | | | |
|---|---|---|---|---|---|---|
| ***Hex Addr*** | ***Size*** | ***Access Type*** | ***Bit*** | ***Register Name*** *Bit Field Name* | ***Description*** | ***LSB Unit*** |
| | | | | | **0Fh: CXP (TBD),**<br>**10h ~ FFh : Reserved.** | |
| **8001** | **1** | **RO** | | **Extended Identifier** | | **N/A** |
| | | | 7~6 | Power Class | 00b: Power Class 1 Module (≤ 8 W max),<br>01b: Power Class 2 Module (≤16 W max),<br>10b: Power Class 3 Module (≤ 24 W max),<br>11b: Power Class 4 Module (≤ 32W). | N/A |
| | | | 5~4 | Lane Ratio Type | 00b: Network lane : Host lane = 1 : n (Mux type),<br>01b: Network lane : Host lane = n : m (Gear Box type),<br>10b: Network lane : Host lane = n : n (Parallel type),<br>11b: Reserved. | N/A |
| | | | 3~1 | WDM Type | 000b: Non-WDM,<br>001b: CWDM,<br>010b: LANWDM,<br>011b: DWDM on 200G-grid,<br>100b: DWDM on 100G-grid,<br>101b: DWDM on 50G-grid,<br>110b: DWDM on 25G-grid,<br>111b: Other type WDM. | N/A |
| | | | 0 | CLEI Presence | 0: No CLEI code present,<br>1: CLEI code present. | N/A |
| **8002** | **1** | **RO** | **7~0** | **Connector Type Code** | **00h: Undefined,**<br>**01h : SC,**<br>**07h : LC,**<br>**08h : MT-RJ,**<br>**09h : MPO,**<br>**Other Codes : Reserved.** | **N/A** |
| **8003** | **1** | **RO** | **7~0** | **Ethernet Application Code** | **Ethernet Application Code.**<br>**00h: Undefined type,**<br>**01h: 100GE SMF 10km, 100GE-LR4,**<br>**02h: 100GE SMF 40km, 100GE-ER4,**<br>**03h: 100GE MMF 100m OM3, 100GE-SR10,**<br>**04h: For future use,**<br>**05h: 40GE SMF 10km, 40GE-LR4,**<br>**07h: 40GE MMF 100m OM3, 40GE-SR4,**<br>**0Dh: 40GE-CR4 Copper**<br>**For future use:**<br>**100G G.959.1 OTU4**<br>**40G G.693 SDH**<br>**40G G.693 OTU3**<br>**40G G.695 SDH**<br>**40G G.695 OTU3,**<br>**0Eh: 100GE-CR10 Copper,**<br>**0Fh: 40G BASE-FR,**<br>**10h~FFh: Reserved.** | **N/A** |
| **8004** | **1** | **RO** | **7~0** | **Fiber Channel Application Code** | **00h: Undefined type.** | **N/A** |
| **8005** | **1** | **RO** | **7~0** | **Copper Link Application Code** | **00h: Undefined type.** | **N/A** |
| **8006** | **1** | **RO** | **7~0** | **SONET/SDH Application Code** | **00h: Undefined type,**<br>**01h: VSR2000-3R2,**<br>**02h: VSR2000-3R3,**<br>**03h: VSR2000-3R5,**<br>**04h ~ 0FFh: Reserved.** | **N/A** |
| **8007** | **1** | **RO** | | **OTN Application Code** | **00h: Undefined type,**<br>**01h: VSR2000-3R2F,**<br>**02h: VSR2000-3R3F,**<br>**03h: VSR2000-3R5F,**<br>**04h: VSR2000-3L2F,** | **N/A** |

| CFP NVR 1 | | | | | | |
|---|---|---|---|---|---|---|
| ***Hex Addr*** | ***Size*** | ***Access Type*** | ***Bit*** | ***Register Name*** *Bit Field Name* | ***Description*** | ***LSB Unit*** |
| | | | | | **05h: VSR2000-3L3F,<br>06h: VSR2000-3L5F,<br>07h: C4S1-2D1 (OTL3.4),<br>08h: 4I1-9D1F (OTL4.4),<br>09h ~ 0FFh: Reserved.** | |
| **8008** | **1** | **RO** | | **Additional Capable Rates Supported** | **Additional application rates module supporting.** | **N/A** |
| | | | 7~5 | Reserved | | 0 |
| | | | 4 | 111.8 Gbps | 0: Not supported, 1: Supported. | N/A |
| | | | 3 | 103.125 Gbps | 0: Not supported, 1: Supported. | N/A |
| | | | 2 | 41.25 Gbps | 0: Not supported, 1: Supported. | N/A |
| | | | 1 | 43 Gbps | 0: Not supported, 1: Supported. | N/A |
| | | | 0 | 39.8 Gbps | 0: Not supported, 1: Supported. | N/A |
| **8009** | **1** | **RO** | | **Number of Lanes Supported** | **Number of Network Lane supported and number of Host Lane supported in this particular module.** | **N/A** |
| | | | 7~4 | Number of Network Lanes | The value of 0 represents 16 network lanes supported. The values of 1 through 15 represent the actual number of network lanes supported. | N/A |
| | | | 3~0 | Number of Host Lanes | The value of 0 represents 16 host lanes supported. The values of 1 through 15 represent the actual number of host lanes supported. | N/A |
| **800A** | **1** | **RO** | | **Media Properties** | | **N/A** |
| | | | 7~6 | Media Type | 00b: SMF ,<br>01b: MMF (OM3),<br>10b: Reserved,<br>11b: Copper. | N/A |
| | | | 5 | Directionality | 0: Normal,<br>1: BiDi. | N/A |
| | | | 4 | Optical Multiplexing and De-multiplexing | 0: Without optical MUX/DEMUX,<br>1: With optical MUX/DEMUX. | N/A |
| | | | 3~0 | Active Fiber per Connector | A 4-bit unsigned number representing number of active fibers for TX and RX per connector.<br>0: 16 TX Lanes and 16 RX Lanes,<br>1: 1 TX Lane and 1 RX Lane,<br>4: 4 TX Lanes and 4 RX Lanes,<br>10: 10 TX Lanes and 10 RX Lanes,<br>12: 12 TX Lanes and 12 RX Lanes. | N/A |
| **800B** | **1** | **RO** | **7~0** | **Maximum Network Lane Bit Rate** | **8-bit value x 0.2 Gbps.** | **0.2 Gbps** |
| **800C** | **1** | **RO** | **7~0** | **Maximum Host Lane Bit Rate** | **8-bit value x 0.2 Gbps.** | **0.2 Gbps** |
| **800D** | **1** | **RO** | **7~0** | **Maximum Single Mode Optical Fiber Length** | **8-bit value x 1 km for single mode fiber length.** | **1 km** |
| **800E** | **1** | **RO** | **7~0** | **Maximum Multi-Mode Optical Fiber Length** | **8-bit value x 10 m for multi-mode fiber length.** | **10 m** |
| **800F** | **1** | **RO** | **7~0** | **Maximum Copper Cable Length** | **8-bit value x 1 m for copper cable length.** | **1 m** |
| **8010** | **1** | **RO** | | **Transmitter Spectral Characteristics 1** | | **N/A** |
| | | | 7~5 | Reserved | | 0 |
| | | | 4~0 | Number of Active Transmit Fibers | 0: Undefined. | N/A |
| **8011** | **1** | **RO** | | **Transmitter Spectral Characteristics 2** | | **N/A** |
| | | | 7~5 | Reserved | | 0 |
| | | | 4~0 | Number of Wavelengths per active Transmit Fiber | 0: Undefined. | N/A |
| **8012** | **2** | **RO** | **7~0** | **Minimum Wavelength per Active Fiber** | **16-bit unsigned value x 0.025 nm. (MSB** | **0.025** |

| CFP NVR 1 | | | | | | |
|---|---|---|---|---|---|---|
| ***Hex Addr*** | ***Size*** | ***Access Type*** | ***Bit*** | ***Register Name*** *Bit Field Name* | ***Description*** | ***LSB Unit*** |
| | | | | | **is at 8012h, LSB is at 8013h).** | **nm** |
| **8014** | **2** | **RO** | **7~0** | **Maximum Wavelength per Active Fiber** | **16-bit unsigned value x 0.025 nm. (MSB is at 8014h, LSB is at 8015h).** | **0.025 nm** |
| **8016** | **2** | **RO** | **7~0** | **Maximum per Lane Optical Width** | **Guaranteed range of laser wavelength. 16-bit unsigned value x 1 pm. MSB is at 8016h, LSB is at 8017h.** | **1 pm** |
| **8018** | **1** | **RO** | | **Device Technology 1** | | **N/A** |
| | | | 7~4 | Laser Source Technology | 0000b: VCSEL,<br>0001b: FP,<br>0010b: DFB,<br>0011b: DBR,<br>0100b: Copper,<br>0101b ~ 1111b:Reserved. | N/A |
| | | | 3~0 | Transmitter modulation technology | 0000b: DML,<br>0001b: EML,<br>0010b: InP-MZ,<br>0011b: LN-MZ<br>0100b: Copper,<br>0101b ~ 1111b: Reserved. | N/A |
| **8019** | **1** | **RO** | | **Device Technology 2** | | **N/A** |
| | | | 7 | Wavelength control | 0: No wavelength control,<br>1: Active wavelength control. | N/A |
| | | | 6 | Cooled transmitter | 0: Un-cooled transmitter device,<br>1: Cooled or Semi-cooled transmitter. | N/A |
| | | | 5 | Tunability | 0: Transmitter not Tunable,<br>1: Transmitter Tunable. | N/A |
| | | | 4 | VOA implemented | 0: Detector side VOA not implement,<br>1: Detector side VOA implement. | N/A |
| | | | 3~2 | Detector Type | 00b: Undefined,<br>01b: PIN detector,<br>10b: APD detector,<br>11b: Optical Amplifier + PIN detector. | N/A |
| | | | 1 | CDR with EDC | 0: CDR without EDC,<br>1: CDR with EDC. | N/A |
| | | | 0 | Reserved | | 0 |
| **801A** | **1** | **RO** | | **Signal Code** | | **N/A** |
| | | | 7~6 | Modulation | 00b: Undefined,<br>01b: NRZ,<br>10b: RZ,<br>11b: Reserved. | N/A |
| | | | 5~2 | Signal coding | 0000b: Non-PSK,<br>0001b: ODB,<br>0010b: DPSK,<br>0011b: QPSK,<br>0100b: DQPSK,<br>0101b: DPQPSK,<br>0110~1010b: Reserved,<br>1011b: 16QAM,<br>1100b: 64QAM,<br>1101b: 256QAM,<br>1110~1111b: Reserved. | N/A |
| | | | 1~0 | Reserved | | 0 |
| **801B** | **1** | **RO** | **7~0** | **Maximum Total Optical Output Power per Connector** | **Unsigned 8 bit value * 100 uW.** | **100 uW** |
| **801C** | **1** | **RO** | **7~0** | **Maximum Optical Input Power per Network Lane** | **Unsigned 8 bit value * 100 uW.** | **100 uW** |
| **801D** | **1** | **RO** | **7~0** | **Maximum Power Consumption** | **Unsigned 8 bit value * 200 mW.** | **200 mW** |
| **801E** | **1** | **RO** | **7~0** | **Maximum Power Consumption in Low Power Mode** | **Unsigned 8 bit value * 20 mW.** | **20 mW** |

| CFP NVR 1 | | | | | | |
|---|---|---|---|---|---|---|
| ***Hex Addr*** | ***Size*** | ***Access Type*** | ***Bit*** | ***Register Name*** *Bit Field Name* | ***Description*** | ***LSB Unit*** |
| **801F** | **1** | **RO** | **7~0** | **Maximum Operating Case Temp Range** | **Signed 8 bit value of * 1 degC with valid range of 0 ~ 100 degC. Use 2's complement representation.** | **1 degC** |
| **8020** | **1** | **RO** | **7~0** | **Minimum Operating Case Temp Range** | **Signed 8 bit value. Increments of * 1 degC with valid range of –40 ~ +40 degC. Use 2's complement representation.** | **1 degC** |
| **8021** | **16** | **RO** | **7~0** | **Vendor Name** | **Vendor (manufacturer) name in any combination of letters and/or digits in ASCII code.** | **N/A** |
| **8031** | **3** | **RO** | **7~0** | **Vendor OUI** | **The vendor organizationally unique identifier field (vendor OUI) is a 3-byte field that contains the IEEE Company Identifier for the vendor.** | **N/A** |
| **8034** | **16** | **RO** | **7~0** | **Vendor Part Number** | **Vendor (manufacturer) part number in any combination of letters and/or digits in ASCII code.** | **N/A** |
| **8044** | **16** | **RO** | **7~0** | **Vendor Serial Number** | **Vendor (manufacturer) serial number in any combination of letters and/or digits in ASCII code.** | **N/A** |
| **8054** | **8** | **RO** | **7~0** | **Date Code** | **Vendor (manufacturer) date code in ASCII characters, in the format YYYYMMDD (e.g., 20090310 for March 10, 2009). One character at each MDIO address.** | **N/A** |
| **805C** | **2** | **RO** | **7~0** | **Lot Code** | **Lot code in any combination of letters and/or digits in ASCII code.** | **N/A** |
| **805E** | **10** | **RO** | **7~0** | **CLEI Code** | **CLEI Code in any combination of letters and/or digits in ASCII code.** | **N/A** |
| **8068** | **1** | **RO** | **7~0** | **CFP MSA Hardware Specification Revision Number** | **This register indicates the CFP MSA Hardware Specification version number supported by the transceiver. The 8 bits are used to represent the version number times 10. This yields a max of 25.5 revisions.** | **N/A** |
| **8069** | **1** | **RO** | **7~0** | **CFP MSA Management Interface Specification Revision Number** | **This register indicates the CFP MSA Management Interface Specification version number supported by the transceiver. The 8 bits are used to represent the version number times 10. This yields a max of 25.5 revisions.** | |
| **806A** | **2** | **RO** | **7~0** | **Module Hardware Version Number** | **A two-register number in the format of x.y with x at lower address and y at higher address.** | **N/A** |
| **806C** | **2** | **RO** | **7~0** | **Module Firmware Version Number** | **A two-register number in the format of x.y with x at lower address and y at higher address.** | **N/A** |
| **806E** | **1** | **RO** | | **Digital Diagnostic Monitoring Type** | | **N/A** |
| | | | 7~4 | Reserved | | 0 |
| | | | 3 | Received power measurement type | 0: OMA, 1: Average Power. | N/A |
| | | | 2 | Transmitted power measurement type | 0: OMA, 1: Average Power. | N/A |
| | | | 1~0 | Reserved | | 0 |
| **806F** | **1** | **RO** | | **Digital Diagnostic Monitoring Capability 1** | **Module level DDM capability.** | **N/A** |
| | | | 7~6 | Transceiver auxiliary monitor 2 | 00b: Not supported,<br>01b ~ 11b: TBD. | N/A |
| | | | 5~4 | Transceiver auxiliary monitor 1 | 00b: Not supported,<br>01b ~ 11b: TBD. | N/A |
| | | | 3 | Reserved | | 0 |
| | | | 2 | Transceiver SOA bias current monitor | 0: Not supported, 1: supported. | N/A |

| CFP NVR 1 | | | | | | |
|---|---|---|---|---|---|---|
| ***Hex Addr*** | ***Size*** | ***Access Type*** | ***Bit*** | ***Register Name*** *Bit Field Name* | ***Description*** | ***LSB Unit*** |
| | | | 1 | Transceiver power supply voltage monitor | 0: Not supported, 1: supported. | N/A |
| | | | 0 | Transceiver temperature monitor | 0: Not supported, 1: supported. | N/A |
| **8070** | **1** | **RO** | | **Digital Diagnostic Monitoring Capability 2** | **Per lane DDM capability.** | **N/A** |
| | | | 7~4 | Reserved | | 0 |
| | | | 3 | Network Lane received power monitor | 0: Not supported, 1: supported. | N/A |
| | | | 2 | Network Lane laser output power monitor | 0: Not supported, 1: supported. | N/A |
| | | | 1 | Network Lane laser bias current monitor | 0: Not supported, 1: supported. | N/A |
| | | | 0 | Network Lane laser temperature monitor | 0: Not supported, 1: supported. | N/A |
| **8071** | **1** | **RO** | | **Module Enhanced Options** | | **N/A** |
| | | | 7 | Host Lane Loop-back | 0: Not supported, 1: Supported. | N/A |
| | | | 6 | Host Lane PRBS Supported | 0: Not supported, 1: Supported. | N/A |
| | | | 5 | Host Lane emphasis control | 0: Not supported, 1: Supported. | N/A |
| | | | 4 | Network Lane Loop-back | 0: Not supported, 1: Supported. | N/A |
| | | | 3 | Network Lane PRBS | 0: Not supported, 1: Supported. | N/A |
| | | | 2 | Decision Threshold Voltage control function of FEC | This bit indicates whether bit 2 of A012h is supported.<br>0: Not supported, 1: Supported. | N/A |
| | | | 1 | Decision Phase control function of FEC | This bit indicates whether bit 1 of A012 is supported.<br>0: Not supported, 1: Supported. | N/A |
| | | | 0 | Unidirectional TX/RX only Operation Modes | 0: Not supported, 1: Supported. | N/A |
| **8072** | **1** | **RO** | **7~0** | **Maximum High-Power-up Time** | **Fully power up time required by module. Unsigned 8-bit value * 1 sec. Use 1 sec if the actual time is less than 1 sec.** | **1 sec** |
| **8073** | **1** | **RO** | **7~0** | **Maximum TX-Turn-on Time** | **Maximum time required to turn on all TX lanes and to let them reach stability. Unsigned 8-bit value * 1 sec. Use 1 sec if it is less than 1 sec.** | **1 sec.** |
| **8074** | **1** | **RO** | **7~0** | **Host Lane Signal Spec** | **0: Unspecified,<br>1: CAUI,<br>2: XLAUI,<br>3: SFI5.2,<br>4~255: Reserved.** | **N/A** |
| **8075** | **1** | **RO** | | **Heat Sink Type** | | **N/A** |
| | | | 7~1 | Reserved | | 0 |
| | | | 0 | Heat Sink Type | 0: Flat top,<br>1: Integrated heat sink. | N/A |
| **8076** | **1** | **RO** | **7~0** | **Maximum TX-Turn-off Time** | **Maximum time required to turn off all transmitters. Unsigned 8-bit value * 1 ms.** | **1 ms** |
| **8077** | **1** | **RO** | **7~0** | **Maximum High-Power-down Time** | **Maximum time required from entering the High-Power-down state to exit from this state. Unsigned 8-bit value * 1 sec. Use 1 sec if it is less than 1 second.** | **1 sec.** |
| **8078** | **1** | **RO** | | **Module Enhanced Options 2** | | **N/A** |
| | | | 7~5 | Reserved | | N/A |
| | | | 4 | Active Decision Voltage and Phase function | 0: Not supported, 1: Supported. | N/A |
| | | | 3 | RX FIFO Reset | 0: Not supported, 1: Supported. | N/A |
| | | | 2 | RX FIFO Auto Reset | 0: Not supported, 1: Supported. | N/A |
| | | | 1 | TX FIFO Reset | 0: Not supported, 1: Supported. | N/A |
| | | | 0 | TX FIFO Auto Reset | 0: Not supported, 1: Supported. | N/A |
| **8079** | **1** | **RO** | | **Transmitter Monitor Clock Options** | **This clock is intended to be used as a reference for measurements of the** | **0** |

| CFP NVR 1 | | | | | | |
|---|---|---|---|---|---|---|
| ***Hex Addr*** | ***Size*** | ***Access Type*** | ***Bit*** | ***Register Name*** *Bit Field Name* | ***Description*** | ***LSB Unit*** |
| | | | | | **optical output. If provided, the clock shall operate at a rate relative to the optical lane rate of 1/16 rate for 40Gbit/s applications and a 1/8 rate of 25Gbit/s for 100Gbit/s applications. Another option is a clock at 1/16 or 1/64 the rate of transmitter electrical input data.** | |
| | | | 7 | 1/16 of Host Lane Rate | 0: Not supported, 1: Supported. | 0 |
| | | | 6 | 1/16 of Network Lane Rate | 0: Not supported, 1: Supported. | 0 |
| | | | 5 | 1/64 of Host Lane Rate | 0: Not supported, 1: Supported. | 0 |
| | | | 4 | 1/64 of Network Lane Rate | 0: Not supported, 1: Supported. | 0 |
| | | | 3 | Reserved | | 0 |
| | | | 2 | 1/8 of Network Lane Rate | 0: Not supported, 1: Supported. | 0 |
| | | | 1 | Reserved | | 0 |
| | | | 0 | Monitor Clock Option | 0: Supported, 1: Supported. | 0 |
| **807A** | **1** | **RO** | | **Receiver Monitor Clock Options** | **The CFP module may supply an optional receiver monitor clock. This clock is intended to be used as a reference for measurements of the optical input. If provided, the clock shall operate at a rate relative to the optical lane rate of 1/16 rate for 40Gbit/s applications and 1/8 rate of 25Gbit/s for 100Gbit/s applications. Another option is a clock at 1/16 or 1/64 rate of the receiver electrical output data.** | **0** |
| | | | 7 | 1/16 of Host Lane Rate | 0: Not supported, 1: Supported. | 0 |
| | | | 6 | 1/16 of Network Lane Rate | 0: Not supported, 1: Supported. | 0 |
| | | | 5 | 1/64 of Host Lane Rate | 0: Not supported, 1: Supported. | 0 |
| | | | 4 | 1/64 of Network Lane Rate | 0: Not supported, 1: Supported. | 0 |
| | | | 3 | Reserved | | 0 |
| | | | 2 | 1/8 of Network Lane Rate | 0: Not supported, 1: Supported. | 0 |
| | | | 1 | Reserved | | 0 |
| | | | 0 | Monitor Clock Option | 0: Not supported, 1: Supported. | 0 |
| **807B** | **4** | **RO** | | **Reserved** | | **0** |
| **807F** | **1** | **RO** | **7~0** | **CFP NVR 1 Checksum** | **The 8-bit unsigned sum of all CFP NVR 1 contents from address 8000h through 807Eh inclusive.** | **N/A** |

## 5.2 CFP NVR 2 Table: Alarm/Warning Threshold Registers

This whole table contains alarm and warning thresholds for DDM A/D measurement values, listed in CFP registers 8080h through 80FEh. Each register field is a 16-bit value with the type of signed and unsigned detailed in *Table 19 CFP NVR 2*. Each register field uses two addresses with MSB at lower address. All of the alarm and warning thresholds are listed in *Table 19 CFP NVR 2*.

Each A/D value has a corresponding high alarm, low alarm, high warning and low warning threshold. The warning thresholds have more conservative value in terms of reporting the monitored A/D measurements while alarm thresholds represent more severe conditions that call for immediate attention when A/D measurements hit these values. These factory-

set values allow the host to determine when a particular value is outside of "normal" limits as determined by the CFP module manufacturer. It is assumed that these threshold values will vary with different technologies and different implementations.

*Table 19 CFP NVR 2*

| CFP NVR 2 | | | | | | |
|---|---|---|---|---|---|---|
| ***Hex Addr*** | ***Size*** | ***Access Type*** | ***Bit*** | ***Register Name*** *Bit Field Name* | ***Description*** | ***LSB Unit*** |
| ***Alarm/Warning Threshold Registers*** | | | | | | |
| **8080** | **2** | **RO** | **7~0** | **Transceiver Temp High Alarm Threshold** | **These thresholds are a signed 16-bit integer with LSB = 1/256 of a degree Celsius representing a range from -128 to + 127 255/256 degree C. MSA valid range is between –40 and +125C." MSB stored at low address, LSB stored at high address.** | **1/256 degC** |
| **8082** | **2** | **RO** | **7~0** | **Transceiver Temp High Warning Threshold** | | |
| **8084** | **2** | **RO** | **7~0** | **Transceiver Temp Low Warning Threshold** | | |
| **8086** | **2** | **RO** | **7~0** | **Transceiver Temp Low Alarm Threshold** | | |
| **8088** | **2** | **RO** | **7~0** | **VCC High Alarm Threshold** | **These thresholds are an unsigned 16-bit integer with LSB = 0.1 mV, representing a range of voltage from 0 to 6.5535 V. MSB stored at low address, LSB stored at high address.** | **0.1 mV** |
| **808A** | **2** | **RO** | **7~0** | **VCC High Warning Threshold** | | |
| **808C** | **2** | **RO** | **7~0** | **VCC Low Warning Threshold** | | |
| **808E** | **2** | **RO** | **7~0** | **VCC Low Alarm Threshold** | | |
| **8090** | **2** | **RO** | **7~0** | **SOA Bias Current High Alarm Threshold** | **These threshold values are an unsigned 16-bit integer with LSB = 2 uA, representing a range of current from 0 to 131.072 mA. MSB stored at low address, LSB stored at high address.** | **2 uA** |
| **8092** | **2** | **RO** | **7~0** | **SOA Bias Current High Warning Threshold** | | |
| **8094** | **2** | **RO** | **7~0** | **SOA Bias Current Low Warning Threshold** | | |
| **8096** | **2** | **RO** | **7~0** | **SOA Bias Current Low Alarm Threshold** | | |
| **8098** | **2** | **RO** | **7~0** | **Auxiliary 1 Monitor High Alarm Threshold** | **TBD** | **TBD** |
| **809A** | **2** | **RO** | **7~0** | **Auxiliary 1 Monitor High Warning Threshold** | **TBD** | |
| **809C** | **2** | **RO** | **7~0** | **Auxiliary 1 Monitor Low Warning Threshold** | **TBD** | |
| **809E** | **2** | **RO** | **7~0** | **Auxiliary 1 Monitor Low Alarm Threshold** | **TBD** | |
| **80A0** | **2** | **RO** | **7~0** | **Auxiliary 2 Monitor High Alarm Threshold** | **TBD** | **TBD** |
| **80A2** | **2** | **RO** | **7~0** | **Auxiliary 2 Monitor High Warning Threshold** | **TBD** | |
| **80A4** | **2** | **RO** | **7~0** | **Auxiliary 2 Monitor Low Warning Threshold** | **TBD** | |
| **80A6** | **2** | **RO** | **7~0** | **Auxiliary 2 Monitor Low Alarm Threshold** | **TBD** | |
| **80A8** | **2** | **RO** | **7~0** | **Laser Bias Current High Alarm Threshold** | **Alarm and warning thresholds for measured laser bias current. Reference A2A0h Description for additional information. MSB stored at low address, LSB stored at high address.** | **See A2A0h** |
| **80AA** | **2** | **RO** | **7~0** | **Laser Bias Current High Warning Threshold** | | |
| **80AC** | **2** | **RO** | **7~0** | **Laser Bias Current Low Warning Threshold** | | |
| **80AE** | **2** | **RO** | **7~0** | **Laser Bias Current Low Alarm Threshold** | | |
| **80B0** | **2** | **RO** | **7~0** | **Laser Output Power High Alarm Threshold** | **Alarm and warning thresholds for measured laser output power.** | **See A2B0h** |

| CFP NVR 2 | | | | | | |
|---|---|---|---|---|---|---|
| ***Hex Addr*** | ***Size*** | ***Access Type*** | ***Bit*** | ***Register Name*** *Bit Field Name* | ***Description*** | ***LSB Unit*** |
| **80B2** | **2** | **RO** | **7~0** | **Laser Output Power High Warning Threshold** | **Reference A2B0h Description for additional information. MSB stored at low address, LSB stored at high address.** | |
| **80B4** | **2** | **RO** | **7~0** | **Laser Output Power Low Warning Threshold** | | |
| **80B6** | **2** | **RO** | **7~0** | **Laser Output Power Low Alarm Threshold** | | |
| **80B8** | **2** | **RO** | **7~0** | **Laser Temperature High Alarm Threshold** | **Alarm and warning thresholds for measured received input power. Reference A2C0h Description for additional information. MSB stored at low address, LSB stored at high address.** | **See A2C0h** |
| **80BA** | **2** | **RO** | **7~0** | **Laser Temperature High Warning Threshold** | | |
| **80BC** | **2** | **RO** | **7~0** | **Laser Temperature Low Warning Threshold** | | |
| **80BE** | **2** | **RO** | **7~0** | **Laser Temperature Low Alarm Threshold** | | |
| **80C0** | **2** | **RO** | **7~0** | **Receive Optical Power High Alarm Threshold** | **Alarm and warning thresholds for measured received input power. Reference A2D0h Description for additional information. MSB stored at low address, LSB stored at high address.** | **See A2D0h** |
| **80C2** | **2** | **RO** | **7~0** | **Receive Optical Power High Warning Threshold** | | |
| **80C4** | **2** | **RO** | **7~0** | **Receive Optical Power Low Warning Threshold** | | |
| **80C6** | **2** | **RO** | **7~0** | **Receive Optical Power Low Alarm Threshold** | | |
| **80C8** | **55** | **RO** | **7~0** | **Reserved** | | **0** |
| **80FF** | **1** | **RO** | **7~0** | **CFP NVR 2 Checksum** | **The 8-bit unsigned sum of all CFP NVR 2 contents from address 8080h through 80FEh inclusive.** | **NA** |

## 5.3 CFP NVR 3 Table: Network Lane BOL Measurement Registers

*Table 20 CFP NVR 3* lists four beginning-of-life measurements of network lanes as the reference data for module aging consideration. CFP MSA specifies that vendor provides these data as an option. For details regarding each measurement please refer to description of each register in the table.

*Table 20 CFP NVR 3*

| CFP NVR 3 | | | | | | |
|---|---|---|---|---|---|---|
| ***Hex Addr*** | ***Size*** | ***Access Type*** | ***Bit*** | ***Register Name*** *Bit Field Name* | ***Description*** | ***LSB Unit*** |
| ***Network Lane BOL Measurements*** | | | | | | |
| **8100** | **32** | **RO** | **7~0** | **RX Sensitivity Spec for network lanes 0 ~ 15.** | **RX Sensitivity measured in dBm @ BER=1e-12 at Typical condition. The value is a signed 16-bit integer with LSB = 0.01dBm. It uses two register addresses each for a total 32 register addresses for total 16 lanes.** | **0.01 dBm** |
| **8120** | **32** | **RO** | **7~0** | **TX Power Spec for network lanes 0 ~ 15.** | **TX Power measured in dBm at typical condition. The value is a signed 16-bit integer with LSB = 0.01dBm. It uses two register addresses each for a total 32 register addresses for total 16 lanes.** | **0.01 dBm** |

| CFP NVR 3 | | | | | | |
|---|---|---|---|---|---|---|
| ***Hex Addr*** | ***Size*** | ***Access Type*** | ***Bit*** | ***Register Name*** *Bit Field Name* | ***Description*** | ***LSB Unit*** |
| **8140** | **32** | **RO** | **7~0** | **Measured ER for network lanes 0 ~ 15.** | **Measured Extinction ratio at Typical condition in dB. The value is an unsigned 16-bit integer with LSB = 0.01dB. It uses two register addresses each for a total 32 register addresses for total 16 lanes.** | **0.01 dB** |
| **8160** | **32** | **RO** | **7~0** | **Path Penalty for network lanes 0 ~ 15.** | **Path penalty @worst CD at Typical condition. The value is an unsigned 16-bit integer with LSB = 0.01dB. It uses two register addresses each for a total 32 register addresses for total 16 lanes.** | **0.01 dB** |

## 5.4 CFP NVR 4 Table

*Table 21 CFP NVR 4*

| CFP NVR 4 | | | | | | |
|---|---|---|---|---|---|---|
| ***Hex Add*** | ***Size*** | ***Access Type*** | ***Bit*** | ***Register Name*** *Bit Field Name* | ***Description*** | ***LSB Unit*** |
| | | | | | | |
| **8180** | **1** | **RO** | **7~0** | **CFP NVR 3 Checksum** | **The 8-bit unsigned sum of all CFP NVR 3 contents from address 8100h through 817Fh inclusive.** | **N/A** |
| **8181** | **127** | **RO** | **7~1** | **Reserved** | | **N/A** |

## 5.5 CFP Module VR 1 Table

*Table 22 CFP Module VR 1* lists all the registers in several distinctive groups in terms of their function. All of the registers in this table use 16-bit data format. The description of each register field consists of three parts. The "Description" column of this table provides some rudimentary information about each register. For more involved description, a dedicated section of discussion is presented in "CFP Control and Signaling Theory". The sections presented in this chapter, provides additional information whenever it is appropriate.

Some CFP Control, Status and DDM registers are application specific. CFP MSA intent is to define registers and addresses. CFP MSA-compliant modules shall not use the specified registers for alternate purposes.

CFP MSA-compliant modules need not support all application-specific A/D or status registers defined here. For example, a parallel optical transceiver for short reach application may not need APD power supply or TEC status support.

### 5.5.1 CFP Command/Setup Registers

This group includes 8 registers that host may use to control module behavior.

#### 5.5.1.1 NVR Access Control (A004h)

This is a one address register with all the details documented in 4.10.

#### 5.5.1.2 PRG_CNTLs Function Select (A005h, A006, A007h)

Each of these registers selects a control function for the programmable control pins. Refer to 4.11.1 Programmable Control Functions for PRG_CNTLs for details.

#### 5.5.1.3 PRG_ALRMs Source Select (A008h, A009h, A00Ah)

Each of these registers selects an alarm source for the programmable alarm pins. Refer to 4.11.2 Programmable Alarm Sources for PRG_ALRMs for details.

#### 5.5.1.4 Module Bi-/Uni- Directional Operating Mode Select (A00Bh)

CFP module users may seek special applications where the CFP module is used for single directional operation. In addition to the "Description" column of this CFP register more information is referenced to 4.4 Special Modes of Operation.

### 5.5.2 Module Control Registers (A010h~A014h)

These registers provide both additional and alternative controls to hardware pins and programmable control pins in controlling CFP module. More information is documented in the "Description" column.

### 5.5.3 Module State Register (A016h)

Module State register provides real time States of the module operation. Its use has been discussed in detail in 4.1 CFP Module States and Related Signals. Note that this register is part of the global alarm system.

### 5.5.4 Module Alarm Summary Registers (A018h, A019h, A01Ah, A01Bh)

This set of CFP registers enable the fast diagnosis of locating the origin of a FAWS condition for the Host in response to a global alarm interrupt request generated by GLB_ALRM. This set of CFP registers is at the top level of the global alarm aggregation hierarchy. Host can use this set of CFP registers as the top-level index for tracking down the origin of the interrupt request. For more details in using these registers please reference 4.6 Global Alarm System Logic.

### 5.5.5 Module FAWS Registers (A01Dh, A01Eh, A01Fh, A020h)

This set of CFP registers is the main source of module status and alarm/warning conditions.

### 5.5.6 Module FAWS Latch Registers (A022h, A023h, A024h, A025h, A026h)

All the CFP registers in this group contain the latched version of Module Alarm/Status Registers described above. Global Alarm uses these latched bits to report to the Host as depicted by *Figure 10 Global Alarm Signal Aggregation*. All of the bits in these CFP registers are cleared upon the Host reading.

### 5.5.7 Module FAWS Enable Registers (A028h, A029h, A02Ah, A02Bh, A02Ch)

All the CFP registers in this group are the enable registers for Module Alarm/Status Register group (A01Dh, A01Eh, A01Fh, A020h). These CFP registers allow host to enable or disable any particular FAWS bits to contribute to GLB_ALRM. Optional features and not-supported functions will have their corresponding Enable bit(s) set to 0 by the CFP during the Initialize state.

### 5.5.8 Module Analog A/D Value Registers (A02Fh, A030h, A031h, A032h, A033h)

Three analog quantities, Module Temperature Monitor A/D Value, Module Power Supply 3.3 V Monitor A/D Value, and SOA Bias Current A/D Value, are supported by this group of registers. These monitoring quantities are at module level and non-network lane specific. Two additional auxiliary monitoring quantities are specified future use.

The values in these and all other A/D registers are automatically updated with maximum period of 100 ms for single network lane applications. If the number of network lane is greater than 1, the maximum update period shall be 50 * (N + 1) ms, where N denotes the number of network lanes supported in the application.

### 5.5.9 Module PRBS Registers (A038h, A039h)

These are Network Lane PRBS Data Bit Count and Host Lane PRBS Data Bit Count registers. For their use reference 4.9 Bit Error Rate Calculation and the register descriptions.

*Table 22 CFP Module VR 1*

| CFP Module VR 1 | | | | | | |
|---|---|---|---|---|---|---|
| ***Hex Addr.*** | ***Size*** | ***Access Type*** | ***Bit*** | ***Register Name*** *Bit Field Name* | ***Description*** | ***Init Value*** |
| **Module Command/Setup Registers** | | | | | | |
| **A000** | **2** | **RO** | **15~0** | **Reserved** | **Vendor/User optional use, not specified by MSA.** | **0000h 0000h** |
| **A002** | **2** | **RO** | **15~0** | **Reserved** | **Vendor/User optional use, not specified by MSA.** | **0000h 0000h** |
| **A004** | **1** | | | **NVR Access Control** | **User NVRs Restore/Save command. Refer to 4.10.2 for details.** | **0000h** |
| | | RW | 15~9 | Reserved | **Vendor specific.** | 0 |
| | | RO | 8~6 | Reserved | | 000b |
| | | RW | 5 | User Restore and Save Command | 0: Restore the User NVR section,<br>1: Save the User NVR section. | 0 |
| | | RO | 4 | Reserved | | 0 |
| | | RO | 3~2 | Command Status | 00b: Idle,<br>01b: Command completed successfully,<br>10b: Command in progress,<br>11b: Command failed. | 00b |
| | | RW | 1~0 | Extended Commands | 00b: No effect,<br>01b: Vendor Specific,<br>10b: Vendor Specific,<br>11b: Restore/Save the User NVRs. | 00b |
| **A005** | **1** | | | **PRG_CNTL3 Function Select** | **Selects, and assigns, a control function to PRG_CNTL3.** | **0000h** |

| CFP Module VR 1 | | | | | | |
|---|---|---|---|---|---|---|
| ***Hex Addr.*** | ***Size*** | ***Access Type*** | ***Bit*** | ***Register Name*** *Bit Field Name* | ***Description*** | ***Init Value*** |
| | | RO | 15~8 | Reserved | | 00h |
| | | RW | 7~0 | Function Select Code | This multi-function input is used as HW_IL_MSB during the Initialize State and it can be programmed to other functions afterward.<br>0: No effect,<br>1: Assign TRXIC_RSTn function to hardware pins PRG_CNTL3. When so assigned this pin uses the active low logic, that is, 0 = Assert (Reset). Note that when so assigned, its soft counterpart Soft PRG_CNTL3 Control (A010h.12) uses an active high logic, that is, 1 = Assert (Reset).<br>2~255: Reserved. | 00h |
| **A006** | **1** | | | **PRG_CNTL2 Function Select** | **Selects, and assigns, a control function to PRG_CNTL2.** | **0000h** |
| | | RO | 15~8 | Reserved | | 00h |
| | | RW | 7~0 | Function Select Code | This multi-function input is used as HW_IL_LSB during the Initialize State and it can be programmed to other functions afterward.<br>0: No effect,<br>1: Assign TRXIC_RSTn function to hardware pins PRG_CNTL2. When so assigned this pin uses the active low logic, that is, 0 = Assert (Reset). Note that when so assigned, its soft counterpart Soft PRG_CNTL2 Control (A010h.11) uses an active high logic, that is, 1 = Assert (Reset).<br>2~255: Reserved. | 00h |
| **A007** | **1** | | | **PRG_CNTL1 Function Select** | **Selects, and assigns, a control function to PRG_CNTL1.** | **0001h** |
| | | RO | 15~8 | Reserved | | 00h |
| | | RW | 7~0 | Function Select Code | 0: No effect,<br>1: Assign TRXIC_RSTn function to hardware pins PRG_CNTL1. When so assigned this pin uses the active low logic, that is, 0 = Assert (Reset). Note that when so assigned, its soft counterpart Soft PRG_CNTL1 Control (A010h.10) uses an active high logic, that is, 1 = Assert (Reset). TRXIC_RSTn is the CFP MSA default function for PRG_CNTL1.<br>2~255: Reserved. | 01h |
| **A008** | **1** | | | **PRG_ALRM3 Source Select** | **Selects, and assigns, an alarm source for PRG_ALRM3.** | **0003h** |
| | | RO | 15~8 | Reserved | | 00h |
| | | RW | 7~0 | Alarm Source Code | 0: Not active, always de-asserted,<br>1: HIPWR_ON,<br>2: Ready State,<br>3: Fault State, MSA default setting,<br>4: RX_ALRM = RX_LOS + RX_NETWORK_LOL,<br>5: TX_ALRM = TX_LOSF + TX_HOST_LOL + TX_CMU_LOL,<br>6: RX_NETWORK_LOL,<br>7: TX_LOSF,<br>8: TX_HOST_LOL,<br>9: OOA, Out of alignment, (Only applicable to certain products. If not implemented in the module, Writing 9 to this register has no effect and shall be read as 0. This is also true for Registers A009h and A00Ah).<br>10~255: Reserved. | 03h |
| **A009** | **1** | | | **PRG_ALRM2 Source Select** | **Selects, and assigns, an alarm source for PRG_ALRM2.** | **0002h** |
| | | RO | 15~8 | Reserved | | 00h |
| | | RW | 7~0 | Alarm Source Code | 0: Not active, always de-asserted,<br>1: HIPWR_ON, | 02h |

| CFP Module VR 1 | | | | | | |
|---|---|---|---|---|---|---|
| ***Hex Addr.*** | ***Size*** | ***Access Type*** | ***Bit*** | ***Register Name*** *Bit Field Name* | ***Description*** | ***Init Value*** |
| | | | | | 2: Ready State, MSA default setting,<br>3: Fault State,<br>4: RX_ALRM = RX_LOS + RX_NETWORK_LOL,<br>5: TX_ALRM = TX_LOSF + TX_HOST_LOL + TX_CMU_LOL,<br>6: RX_NETWORK_LOL,<br>7: TX_LOSF,<br>8: TX_HOST_LOL,<br>9: OOA, Out of alignment, refer to description of A008h for details,<br>10~255: Reserved. | |
| **A00A** | **1** | | | **PRG_ALRM1 Source Select** | **Selects, and assigns, an alarm source for PRG_ALRM1.** | **0001h** |
| | | RO | 15~8 | Reserved | | 00h |
| | | RW | 7~0 | Alarm Source Code | 0: Not active, always de-asserted,<br>1: HIPWR_ON, MSA default setting,<br>2: Ready State,<br>3: Fault State,<br>4: RX_ALRM = RX_LOS + RX_NETWORK_LOL,<br>5: TX_ALRM = TX_LOSF + TX_HOST_LOL + TX_CMU_LOL,<br>6: RX_NETWORK_LOL,<br>7: TX_LOSF,<br>8: TX_HOST_LOL,<br>9: OOA, Out of alignment, refer to description of A008h for details,<br>10~255: Reserved. | 01h |
| **A00B** | **1** | | | **Module Bi-/Uni-Directional Operating Mode Select** | | **0000h** |
| | | RO | 15~3 | Reserved | | 0 |
| | | RW | 2~0 | Module Bi/uni-direction mode Select | 000b: Normal bi-directional mode,<br>001b: Uni-direction TX only mode (optional),<br>010b: Uni-direction RX only mode (optional),<br>011b: Special bi-directional mode (optional),<br>100b~111b: Reserved. | 000b |
| **A00C** | **4** | **RO** | | **Reserved** | | **0000h** |
| **Module Control Registers** | | | | | | |
| **A010** | **1** | | | **Module General Control** | | **0000h** |
| | | RW/SC/LH | 15 | Soft Module Reset | Register bit for module reset function. Writing a 0 to this bit has no effect regardless it was 0 or 1 previously.<br>1: Module reset assert. | 0 |
| | | RW | 14 | Soft Module Low Power | Register bit for module low power function.<br>1: Assert. | 0 |
| | | RW | 13 | Soft TX Disable | Register bit for TX Disable function.<br>1: Assert. | 0 |
| | | RW | 12 | Soft PRG_CNTL3 Control | Register bit for PRG_CNTL3 control function.<br>1: Assert. | 0 |
| | | RW | 11 | Soft PRG_CNTL2 Control | Register bit for PRG_CNTL2 control function.<br>1: Assert. | 0 |
| | | RW | 10 | Soft PRG_CNTL1 Control | Register bit for PRG_CNTL1 control function.<br>1: Assert. | 0 |
| | | RW | 9 | Soft GLB_ALRM Test | Command bit for software forced test signal. When this bit is asserted it generates GLB_ALRM signal.<br>1: Assert. | 0 |
| | | RO | 8~6 | Reserved | | 0 |
| | | RO | 5 | TX_DIS Pin State | Logical state of the TX_DIS pin.<br>1: Assert. | 0 |
| | | RO | 4 | MOD_LOPWR Pin State | Logical state of the MOD_LOPWR pin. | 0 |

| CFP Module VR 1 | | | | | | |
|---|---|---|---|---|---|---|
| ***Hex Addr.*** | ***Size*** | ***Access Type*** | ***Bit*** | ***Register Name*** *Bit Field Name* | ***Description*** | ***Init Value*** |
| | | | | | 1: Assert. | |
| | | RO | 3 | PRG_CNTL3 Pin State | Logical state of the PRG_CNTL3 pin.<br>1: Assert. | 0 |
| | | RO | 2 | PRG_CNTL2 Pin State | Logical state of the PRG_CNTL2 pin.<br>1: Assert. | 0 |
| | | RO | 1 | PRG_CNTL1 Pin State | Logical state of the PRG_CNTL1 pin.<br>1: Assert. | 0 |
| | | RO | 0 | Reserved | | 0 |
| **A011** | **1** | | | **Network Lane TX Control** | **This control acts upon all the network lanes.** | **0200h** |
| | | RO | 15 | Reserved | | 0 |
| | | RW | 14 | TX PRBS Generator Enable | 0: Normal operation, 1: PRBS mode. (Optional) | 0 |
| | | RW | 13 | TX PRBS Pattern 1 | 00b:2^7,<br>01b:2^15,<br>10b:2^23,<br>11b:2^31. | 00b |
| | | RW | 12 | TX PRBS Pattern 0 | | |
| | | RW | 11 | TX De-skew Enable | 0:Normal, 1:Disable | 0 |
| | | RW | 10 | TX FIFO Reset | This bit affects both host and network side TX FIFOs.<br>0: Normal operation, 1: Reset (Optional). | 0 |
| | | RW | 9 | TX FIFO Auto Reset | This bit affects both host and network side TX FIFOs.<br>0: Not Auto Reset, 1: Auto Reset. (Optional). | 1 |
| | | RW | 8 | TX Reset | 0: Normal operation, 1: Reset. Definition and implementation are vendor specific. | 0 |
| | | RW | 7~5 | TX MCLK Control | 000b: Disabled,<br>001b: Reserved,<br>010b: 1/8 of network lane rate,<br>011b: Reserved,<br>100b: 1/64 of network lane rate,<br>101b: 1/64 of host lane rate,<br>110b: 1/16 of network lane rate,<br>111b: 1/16 of host lane rate. | 000b |
| | | RO | 4 | Reserved | | 0b |
| | | RW | 3~1 | TX Rate Select (10G lane rate) | 000b: GbE=10.31,<br>001b:SDH=9.95,<br>010b:OTU3=10.7,<br>011b:OTU4=11.2,<br>100b~111b: Reserved. | 000b |
| | | RW | 0 | TX Reference CLK Rate Select | 0: 1/16,<br>1: 1/64. | 0b |
| **A012** | **1** | | | **Network Lane RX Control** | **This control acts upon all the network lanes.** | **0200h** |
| | | RW | 15 | Active Decision Voltage and Phase function | This bit activates the active decision voltage and phase function in the module.<br>0: not active, 1: active. (Optional) | 0b |
| | | RW | 14 | RX PRBS Checker Enable | 0: Normal operation, 1: PRBS mode. (Optional) | 0b |
| | | RW | 13 | RX PRBS Pattern 1 | 00b: 2^7,<br>01b: 2^15,<br>10b: 2^23,<br>11b: 2^31. | 00b |
| | | RW | 12 | RX PRBS Pattern 0 | | |
| | | RW | 11 | RX Lock RX_MCLK to Reference CLK | 0: Normal operation, 1: Lock RX_MCLK to REFCLK. | 0b |
| | | RW | 10 | Network Lane Loop-back | 0: Normal operation, 1: Network lane loop-back. (Optional) | 0b |
| | | RW | 9 | RX FIFO Auto Reset | 0: Not auto reset, 1: Auto reset. (Optional). | 1b |
| | | RW | 8 | RX Reset | 0: Normal operation, 1: Reset. Definition and implementation are vendor specific. | 0b |
| | | RW | 7~5 | RX MCLK Control | 000b: Disabled, | 000b |

| CFP Module VR 1 | | | | | | |
|---|---|---|---|---|---|---|
| ***Hex Addr.*** | ***Size*** | ***Access Type*** | ***Bit*** | ***Register Name*** *Bit Field Name* | ***Description*** | ***Init Value*** |
| | | | | | 001b: Reserved,<br>010b: 1/8 of network lane rate,<br>011b: Reserved,<br>100b: 1/64 of network lane rate,<br>101b: 1/64 of host lane rate,<br>110b: 1/16 of network lane rate,<br>111b: 1/16 of host lane rate. | |
| | | RW | 4 | RX FIFO Reset | 0: Normal, 1: Reset. (Optional). | 0b |
| | | RW | 3~1 | RX Rate Select | 000b: GbE=10.31,<br>001b:SDH=9.95,<br>010b:OTU3=10.7,<br>011b:OTU4=11.2,<br>100b~111b: Reserved. | 000b |
| | | RW | 0 | RX Reference CLK Rate Select | 0: 1/16,<br>1: 1/64. | 0b |
| **A013** | **1** | **RW** | | **Individual Network Lane TX_DIS Control** | **This register acts upon individual network lanes. Note that toggling individual network lane TX disable bit does not change module state.** | **0000h** |
| | | | 15 | Lane 15 Disable | 0: Normal, 1: Disable. | 0 |
| | | | 14 | Lane 14 Disable | 0: Normal, 1: Disable. | 0 |
| | | | 13 | Lane 13 Disable | 0: Normal, 1: Disable. | 0 |
| | | | 12 | Lane 12 Disable | 0: Normal, 1: Disable. | 0 |
| | | | 11 | Lane 11 Disable | 0: Normal, 1: Disable. | 0 |
| | | | 10 | Lane 10 Disable | 0: Normal, 1: Disable. | 0 |
| | | | 9 | Lane 9 Disable | 0: Normal, 1: Disable. | 0 |
| | | | 8 | Lane 8 Disable | 0: Normal, 1: Disable. | 0 |
| | | | 7 | Lane 7 Disable | 0: Normal, 1: Disable. | 0 |
| | | | 6 | Lane 6 Disable | 0: Normal, 1: Disable. | 0 |
| | | | 5 | Lane 5 Disable | 0: Normal, 1: Disable. | 0 |
| | | | 4 | Lane 4 Disable | 0: Normal, 1: Disable. | 0 |
| | | | 3 | Lane 3 Disable | 0: Normal, 1: Disable. | 0 |
| | | | 2 | Lane 2 Disable | 0: Normal, 1: Disable. | 0 |
| | | | 1 | Lane 1 Disable | 0: Normal, 1: Disable. | 0 |
| | | | 0 | Lane 0 Disable | 0: Normal, 1: Disable. | 0 |
| **A014** | **1** | | | **Host Lane Control** | **This control acts upon all the host lanes.** | **0000h** |
| | | RO | 15 | Reserved | | 0 |
| | | RW | 14 | TX PRBS Checker Enable | 0: Normal operation, 1: PRBS mode. (Optional) | 0 |
| | | RW | 13 | TX PRBS Pattern 1 | 00:2^7, 01:2^15, 10:2^23, 11:2^31. | 00b |
| | | RW | 12 | TX PRBS Pattern 0 | | |
| | | RO | 11 | Reserved | | 0 |
| | | RW | 10 | Host Lane Loop-back Enable | 0: Normal operation, 1: Host lane loop-back. (Optional) | 0 |
| | | RO | 9 | Reserved | | 0 |
| | | RO | 8 | Reserved | | 0 |
| | | RW | 7 | RX PRBS Generator Enable | 0: Normal operation, 1: PRBS mode. (Optional) | 0 |
| | | RW | 6 | RX PRBS Pattern 1 | 00b: 2^7, 01b: 2^15, 10b: 2^23, 11b: 2^31. | 00b |
| | | RW | 5 | RX PRBS Pattern 0 | | |
| | | RO | 4~0 | Reserved | | 0h |
| **A015** | **1** | **RO** | | **Reserved** | | **0000h** |
| **Module State Register** | | | | | | |
| **A016** | **1** | **RO** | | **Module State** | **CFP module state. Only a single bit set at any time.** | **0000h** |
| | | | 15~9 | Reserved | | 0 |
| | | | 8 | High-Power-down State | 1: Corresponding state is active. Word value = 0100h. | 0 |
| | | | 7 | TX-Turn-off State | 1: Corresponding state is active. Word value = 0080h. | 0 |
| | | | 6 | Fault State | 1: Corresponding state is active. Word value = 0040h. | 0 |

| CFP Module VR 1 | | | | | | |
|---|---|---|---|---|---|---|
| ***Hex Addr.*** | ***Size*** | ***Access Type*** | ***Bit*** | ***Register Name*** *Bit Field Name* | ***Description*** | ***Init Value*** |
| | | | | | (Also referred to as MOD_FAULT) | |
| | | | 5 | Ready State | 1: Corresponding state is active. Word value = 0020h. (Also referred to as MOD_READY) | 0 |
| | | | 4 | TX-Turn-on State | 1: Corresponding state is active. Word value = 0010h. | 0 |
| | | | 3 | TX-Off State | 1: Corresponding state is active. Word value = 0008h. | 0 |
| | | | 2 | High-Power-up State | 1: Corresponding state is active. Word value = 0004h. | 0 |
| | | | 1 | Low-Power State | 1: Corresponding state is active. Word value = 0002h. | 0 |
| | | | 0 | Initialize State | 1: Corresponding state is active. Word value = 0001h. | 0 |
| **Module Alarm Summary Registers** | | | | | | |
| **A017** | **1** | **RO** | | **Reserved** | | **0000h** |
| **A018** | **1** | **RO** | | **Global Alarm Summary** | | |
| | | | 15 | GLB_ALRM Assertion Status | Internal status of global alarm output. 1: Asserted. | 0 |
| | | | 14 | Host Lane Fault and Status Summary | Logical OR of all the enabled bits of Host Lane Fault and Status Summary register. | 0 |
| | | | 13 | Network Lane Fault and Status Summary | Logical OR of all the bits in the Network Lane Fault and Status Summary register. | 0 |
| | | | 12 | Network Lane Alarm and Warning Summary | Logical OR of all the bits in the Network Lane Alarm and Warning Summary register. | 0 |
| | | | 11 | Module Alarm and Warning 2 Summary | Logical OR of all the enabled bits of Module Alarms and Warnings 2 Latch register. | 0 |
| | | | 10 | Module Alarm and Warning 1 Summary | Logical OR of all the enabled bits of Module Alarms and Warnings 1 Latch register. | 0 |
| | | | 9 | Module Fault Summary | Logical OR of all the enabled bits of Module Fault Status Latch register. | 0 |
| | | | 8 | Module General Status Summary | Logical OR of all the enabled bits of Module General Status Latch register. | 0 |
| | | | 7 | Module State Summary | Logical OR of all the enabled bits of Module State Latch register. | 0 |
| | | | 6~1 | Reserved | | 0 |
| | | | 0 | Soft GLB_ALRM Test Status | Soft GLB_ALRM Test bit Status. | 0 |
| **A019** | **1** | **RO** | | **Network Lane Alarm and Warning Summary** | **Each bit is the logical OR of all enabled bits in each of Network Lane Alarm and Warning Latch registers.** | **0000h** |
| | | | 15 | Lane 15 Alarm and Warning Summary | Logical OR of all enabled bits in Latched Lane 15 Network Lane Alarm and Warning Register. 1=Fault asserted. | 0 |
| | | | 14 | Lane 14 Alarm and Warning Summary | Logical OR of all enabled bits in Latched Lane 14 Network Lane Alarm and Warning Register. 1=Fault asserted. | 0 |
| | | | 13 | Lane 13 Alarm and Warning Summary | Logical OR of all enabled bits in Latched Lane 13 Network Lane Alarm and Warning Register. 1=Fault asserted. | 0 |
| | | | 12 | Lane 12 Alarm and Warning Summary | Logical OR of all enabled bits in Latched Lane 12 Network Lane Alarm and Warning Register. 1=Fault asserted. | 0 |
| | | | 11 | Lane 11 Alarm and Warning Summary | Logical OR of all enabled bits in Latched Lane 11 Network Lane Alarm and Warning Register. 1=Fault asserted. | 0 |
| | | | 10 | Lane 10 Alarm and Warning Summary | Logical OR of all enabled bits in Latched Lane 10 Network Lane Alarm and Warning Register. 1=Fault asserted. | 0 |
| | | | 9 | Lane 9 Alarm and Warning Summary | Logical OR of all enabled bits in Latched Lane 9 Network Lane Alarm and Warning Register. 1=Fault asserted. | 0 |
| | | | 8 | Lane 8 Alarm and Warning Summary | Logical OR of all enabled bits in Latched Lane 8 Network Lane Alarm and Warning Register. 1=Fault asserted. | 0 |
| | | | 7 | Lane 7 Alarm and Warning Summary | Logical OR of all enabled bits in Latched Lane 7 Network Lane Alarm and Warning Register. 1=Fault asserted. | 0 |
| | | | 6 | Lane 6 Alarm and Warning Summary | Logical OR of all enabled bits in Latched Lane 6 Network Lane Alarm and Warning Register. 1=Fault asserted. | 0 |
| | | | 5 | Lane 5 Alarm and Warning Summary | Logical OR of all enabled bits in Latched Lane 5 Network Lane Alarm and Warning Register. 1=Fault asserted. | 0 |
| | | | 4 | Lane 4 Alarm and Warning Summary | Logical OR of all enabled bits in Latched Lane 4 Network Lane Alarm and Warning Register. 1=Fault asserted. | 0 |

| CFP Module VR 1 | | | | | | |
|---|---|---|---|---|---|---|
| ***Hex Addr.*** | ***Size*** | ***Access Type*** | ***Bit*** | ***Register Name*** *Bit Field Name* | ***Description*** | ***Init Value*** |
| | | | 3 | Lane 3 Alarm and Warning Summary | Logical OR of all enabled bits in Latched Lane 3 Network Lane Alarm and Warning Register. 1=Fault asserted. | 0 |
| | | | 2 | Lane 2 Alarm and Warning Summary | Logical OR of all enabled bits in Latched Lane 2 Network Lane Alarm and Warning Register. 1=Fault asserted. | 0 |
| | | | 1 | Lane 1 Alarm and Warning Summary | Logical OR of all enabled bits in Latched Lane 1 Network Lane Alarm and Warning Register. 1=Fault asserted. | 0 |
| | | | 0 | Lane 0 Alarm and Warning Summary | Logical OR of all enabled bits in Latched Lane 0 Network Lane Alarm and Warning Register. 1=Fault asserted. | 0 |
| **A01A** | **1** | **RO** | | **Network Lane Fault and Status Summary** | **Each bit is the logical OR of all enabled bits in each of the Network Lane fault and Status Latch registers.** | **0000h** |
| | | | 15 | Lane 15 Fault and Status Summary | Logical OR of all enabled bits in Latched Lane 15 Network Lane Fault and Status Register. 1=Fault asserted. | 0 |
| | | | 14 | Lane 14 Fault and Status Summary | Logical OR of all enabled bits in Latched Lane 14 Network Lane Fault and Status Register. 1=Fault asserted. | 0 |
| | | | 13 | Lane 13 Fault and Status Summary | Logical OR of all enabled bits in Latched Lane 13 Network Lane Fault and Status Register. 1=Fault asserted. | 0 |
| | | | 12 | Lane 12 Fault and Status Summary | Logical OR of all enabled bits in Latched Lane 12 Network Lane Fault and Status Register. 1=Fault asserted. | 0 |
| | | | 11 | Lane 11 Fault and Status Summary | Logical OR of all enabled bits in Latched Lane 11 Network Lane Fault and Status Register. 1=Fault asserted. | 0 |
| | | | 10 | Lane 10 Fault and Status Summary | Logical OR of all enabled bits in Latched Lane 10 Network Lane Fault and Status Register. 1=Fault asserted. | 0 |
| | | | 9 | Lane 9 Fault and Status Summary | Logical OR of all enabled bits in Latched Lane 9 Network Lane Fault and Status Register. 1=Fault asserted. | 0 |
| | | | 8 | Lane 8 Fault and Status Summary | Logical OR of all enabled bits in Latched Lane 8 Network Lane Fault and Status Register. 1=Fault asserted. | 0 |
| | | | 7 | Lane 7 Fault and Status Summary | Logical OR of all enabled bits in Latched Lane 7 Network Lane Fault and Status Register. 1=Fault asserted. | 0 |
| | | | 6 | Lane 6 Fault and Status Summary | Logical OR of all enabled bits in Latched Lane 6 Network Lane Fault and Status Register. 1=Fault asserted. | 0 |
| | | | 5 | Lane 5 Fault and Status Summary | Logical OR of all enabled bits in Latched Lane 5 Network Lane Fault and Status Register. 1=Fault asserted. | 0 |
| | | | 4 | Lane 4 Fault and Status Summary | Logical OR of all enabled bits in Latched Lane 4 Network Lane Fault and Status Register. 1=Fault asserted. | 0 |
| | | | 3 | Lane 3 Fault and Status Summary | Logical OR of all enabled bits in Latched Lane 3 Network Lane Fault and Status Register. 1=Fault asserted. | 0 |
| | | | 2 | Lane 2 Fault and Status Summary | Logical OR of all enabled bits in Latched Lane 2 Network Lane Fault and Status Register. 1=Fault asserted. | 0 |
| | | | 1 | Lane 1 Fault and Status Summary | Logical OR of all enabled bits in Latched Lane 1 Network Lane Fault and Status Register. 1=Fault asserted. | 0 |
| | | | 0 | Lane 0 Fault and Status Summary | Logical OR of all enabled bits in Latched Lane 0 Network Lane Fault and Status Register. 1=Fault asserted. | 0 |
| **A01B** | **1** | **RO** | | **Host Lane Fault and Status Summary** | **Each bit is the logical OR of all enabled bits in each of the Host Lane fault and Status Latch registers** | **0000h** |
| | | | 15 | Lane 15 Fault and Status Summary | Logical OR of all enabled bits in Latched Lane 15 Host Lane Fault and Status Register. 1=Fault asserted. | 0 |
| | | | 14 | Lane 14 Fault and Status Summary | Logical OR of all enabled bits in Latched Lane 14 Host Lane Fault and Status Register. 1=Fault asserted. | 0 |
| | | | 13 | Lane 13 Fault and Status Summary | Logical OR of all enabled bits in Latched Lane 13 Host Lane Fault and Status Register. 1=Fault asserted. | 0 |
| | | | 12 | Lane 12 Fault and Status Summary | Logical OR of all enabled bits in Latched Lane 12 Host Lane Fault and Status Register. 1=Fault asserted. | 0 |
| | | | 11 | Lane 11 Fault and Status Summary | Logical OR of all enabled bits in Latched Lane 11 Host Lane Fault and Status Register. 1=Fault asserted. | 0 |
| | | | 10 | Lane 10 Fault and Status Summary | Logical OR of all enabled bits in Latched Lane 10 Host Lane Fault and Status Register. 1=Fault asserted. | 0 |
| | | | 9 | Lane 9 Fault and Status Summary | Logical OR of all enabled bits in Latched Lane 9 Host Lane Fault and Status Register. 1=Fault asserted. | 0 |

| CFP Module VR 1 | | | | | | |
|---|---|---|---|---|---|---|
| ***Hex Addr.*** | ***Size*** | ***Access Type*** | ***Bit*** | ***Register Name*** *Bit Field Name* | ***Description*** | ***Init Value*** |
| | | | 8 | Lane 8 Fault and Status Summary | Logical OR of all enabled bits in Latched Lane 8 Host Lane Fault and Status Register. 1=Fault asserted. | 0 |
| | | | 7 | Lane 7 Fault and Status Summary | Logical OR of all enabled bits in Latched Lane 7 Host Lane Fault and Status Register. 1=Fault asserted. | 0 |
| | | | 6 | Lane 6 Fault and Status Summary | Logical OR of all enabled bits in Latched Lane 6 Host Lane Fault and Status Register. 1=Fault asserted. | 0 |
| | | | 5 | Lane 5 Fault and Status Summary | Logical OR of all enabled bits in Latched Lane 5 Host Lane Fault and Status Register. 1=Fault asserted. | 0 |
| | | | 4 | Lane 4 Fault and Status Summary | Logical OR of all enabled bits in Latched Lane 4 Host Lane Fault and Status Register. 1=Fault asserted. | 0 |
| | | | 3 | Lane 3 Fault and Status Summary | Logical OR of all enabled bits in Latched Lane 3 Host Lane Fault and Status Register. 1=Fault asserted. | 0 |
| | | | 2 | Lane 2 Fault and Status Summary | Logical OR of all enabled bits in Latched Lane 2 Host Lane Fault and Status Register. 1=Fault asserted. | 0 |
| | | | 1 | Lane 1 Fault and Status Summary | Logical OR of all enabled bits in Latched Lane 1 Host Lane Fault and Status Register. 1=Fault asserted. | 0 |
| | | | 0 | Lane 0 Fault and Status Summary | Logical OR of all enabled bits in Latched Lane 0 Network Lane Fault and Status Register. 1=Fault asserted. | 0 |
| | | | | | | |
| **A01C** | **1** | **RO** | | **Reserved** | | **0** |
| **Module FAWS Registers** | | | | | | |
| **A01D** | **1** | **RO** | | **Module General Status** | | **0000h** |
| | | | 15 | Reserved | | 0 |
| | | | 14 | Reserved | | 0 |
| | | | 13 | HW_Interlock | Module internally generated status signal. (FAWS_TYPE_A)<br>0: If module power <= Host cooling capacity or if hardware Interlock is not used,<br>1: If module power > Host cooling capacity. | 0 |
| | | | 12~11 | Reserved | | 0 |
| | | | 10 | Loss of REFCLK Input | Loss of reference clock input. It is an optional feature. (FAWS_TYPE_B).<br>0: Normal,<br>1: Loss of signal. | 0 |
| | | | 9 | TX_JITTER_PLL_LOL | TX jitter PLL loss of lock. It is an optional feature. (FAWS_TYPE_B).<br>0: Normal,<br>1: Loss of lock. | 0 |
| | | | 8 | TX_CMU_LOL | TX CMU loss of lock. It is the loss of lock indicator on the network side of the CMU. It is an optional feature. (FAWS_TYPE_B).<br>0: Normal,<br>1: Loss of lock. | 0 |
| | | | 7 | TX_LOSF | Transmitter Loss of Signal Functionality. Logic OR of all of Network Lanes TX_LOSF bits. PRG_ALRMx mappable. . (FAWS_TYPE_C, since the TX must be enabled).<br>**Note: The corresponding latch register is set to 1 on any change (0-->1 or 1 --> 0) of this status signal.**<br>0: all transmitter signals functional,<br>1: any transmitter signal not functional. | 0 |
| | | | 6 | TX_HOST_LOL | TX IC Lock Indicator. Logic OR of all host lane TX_LOL bits. PRG_ALRMx mappable. (FAWS_TYPE_B).<br>**Note: The corresponding latch register is set to 1 on any change (0-->1 or 1 --> 0) of this status signal.**<br>0: Locked,<br>1: Loss of lock. | 0 |
| | | | 5 | RX_LOS | Receiver Loss of Signal. Logic OR of all of network lane RX_LOS bits. (FAWS_TYPE_B).<br>**Note: The corresponding latch register is set to 1 on any change (0-->1 or 1 --> 0) of this status signal.** | 0 |

| CFP Module VR 1 | | | | | | |
|---|---|---|---|---|---|---|
| ***Hex Addr.*** | ***Size*** | ***Access Type*** | ***Bit*** | ***Register Name*** *Bit Field Name* | ***Description*** | ***Init Value*** |
| | | | | | 0: No network lane RX_LOS bit asserted,<br>1: Any network lane RX_LOS bit asserted. | |
| | | | 4 | RX_NETWORK_LOL | RX IC Lock Indicator. Logic OR of all network lane RX_LOL bits. PRG_ALRMx mappable. (FAWS_TYPE_B).<br>**Note: The corresponding latch register is set to 1 on any change (0-->1 or 1 --> 0) of this status signal.**<br>0: Locked,<br>1: Loss of lock. | 0 |
| | | | 3 | Out of Alignment | Host lane skew out of alignment indicator. Applicable only for some internal implementations. (FAWS_TYPE_B).<br>0: Normal,<br>1: Out of alignment. | 0 |
| | | | 2 | Reserved | | 0 |
| | | | 1 | HIPWR_ON | Status bit representing the condition of module in high power status. FAWS Type is not applicable.<br>0: Module is not in high power on status,<br>1: Module is in high powered on status. | 0 |
| | | | 0 | Reserved | | 0 |
| **A01E** | **1** | **RO** | | **Module Fault Status** | **Module Fault Status bit pattern. Only fatal faults that are potentially harmful to the module can trigger the bits here. All the bits are 0: Normal; 1: fault detected. When any bit in this register is a '1', The Module State register will also be set to the Fault State.** | **0000h** |
| | | | 15 | Reserved | Reserved for extension of "other faults" in case of all the bits used up in this register. | 0 |
| | | | 14~7 | Reserved | | 0 |
| | | | 6 | PLD or Flash Initialization Fault | PLD, CPLD, or FPGA initialization fault. (FAWS_TYPE_A) | 0 |
| | | | 5 | Power Supply Fault | 1: Power supply is out of range. (FAWS_TYPE_A) | 0 |
| | | | 4~2 | Reserved | | 000b |
| | | | 1 | CFP Checksum Fault | 1: CFP Checksum failed. (FAWS_TYPE_A) | 0 |
| | | | 0 | Reserved | | 0 |
| **A01F** | **1** | **RO** | | **Module Alarms and Warnings 1** | | **0000h** |
| | | | 15~12 | Reserved | | 0000b |
| | | | 11 | Mod Temp High Alarm | Mod temp high Alarm. (FAWS_TYPE_A)<br>0: Normal, 1: Asserted. | 0 |
| | | | 10 | Mod Temp High Warning | Mod temp high Warning. (FAWS_TYPE_A)<br>0: Normal, 1: Asserted. | 0 |
| | | | 9 | Mod Temp Low Warning | Mod temp low Warning. (FAWS_TYPE_A)<br>0: Normal, 1: Asserted. | 0 |
| | | | 8 | Mod Temp Low Alarm | Mod temp low Alarm. (FAWS_TYPE_A)<br>0: Normal, 1: Asserted. | 0 |
| | | | 7 | Mod Vcc High Alarm | Input Vcc high Alarm. (FAWS_TYPE_A)<br>0: Normal, 1: Asserted. | 0 |
| | | | 6 | Mod Vcc High Warning | Input Vcc high Warning. (FAWS_TYPE_A)<br>0: Normal, 1: Asserted. | 0 |
| | | | 5 | Mod Vcc Low Warning | Input Vcc low Warning. (FAWS_TYPE_A)<br>0: Normal, 1: Asserted. | 0 |
| | | | 4 | Mod Vcc Low Alarm | Input Vcc low Alarm. (FAWS_TYPE_A)<br>0: Normal, 1: Asserted. | 0 |
| | | | 3 | Mod SOA Bias High Alarm | SOA bias current high alarm. (FAWS_TYPE_B)<br>0: Normal, 1: Asserted. | 0 |
| | | | 2 | Mod SOA Bias High Warning | SOA bias current high warning. (FAWS_TYPE_B)<br>0: Normal, 1: Asserted. | 0 |
| | | | 1 | Mod SOA Bias Low Warning | SOA bias current low warning. (FAWS_TYPE_B)<br>0: Normal, 1: Asserted. | 0 |
| | | | 0 | Mod SOA Bias Low Alarm | SOA bias current low alarm. (FAWS_TYPE_B)<br>0: Normal, 1: Asserted. | 0 |

| CFP Module VR 1 | | | | | | |
|---|---|---|---|---|---|---|
| ***Hex Addr.*** | ***Size*** | ***Access Type*** | ***Bit*** | ***Register Name*** *Bit Field Name* | ***Description*** | ***Init Value*** |
| **A020** | **1** | **RO** | | **Module Alarms and Warnings 2** | | **0000h** |
| | | | 15~8 | Reserved | | 0 |
| | | | 7 | Mod Aux 1 High Alarm | Module aux ch 1 high alarm. (FAWS Type is vendor TBD)<br>0: Normal, 1: Asserted.. | 0 |
| | | | 6 | Mod Aux 1 High Warning | Module aux ch 1 high warning. (FAWS Type is vendor TBD)<br>0: Normal, 1: Asserted. | 0 |
| | | | 5 | Mod Aux 1 Low Warning | Module aux ch 1 low warning. (FAWS Type is vendor TBD)<br>0: Normal, 1: Asserted. | 0 |
| | | | 4 | Mod Aux 1 Low Alarm | Module aux ch 1 low alarm. (FAWS Type is vendor TBD)<br>0: Normal, 1: Asserted. | 0 |
| | | | 3 | Mod Aux 2 High Alarm | Module aux ch 2 high alarm. (FAWS Type is vendor TBD)<br>0: Normal, 1: Asserted. | 0 |
| | | | 2 | Mod Aux 2 High Warning | Module aux ch 2 high warning. (FAWS Type is vendor TBD)<br>0: Normal, 1: Asserted. | 0 |
| | | | 1 | Mod Aux 2 Low Warning | Module aux ch 2 low warning. (FAWS Type is vendor TBD)<br>0: Normal, 1: Asserted. | 0 |
| | | | 0 | Mod Aux 2 Low Alarm | Module aux ch 2 low alarm. (FAWS Type is vendor TBD)<br>0: Normal, 1: Asserted. | 0 |
| **A021** | **1** | **RO** | | **Reserved** | | 0 |
| **Module FAWS Latch Registers** | | | | | | |
| **A022** | **1** | | | **Module State Latch** | **CFP module state Latch.** | **0000h** |
| | | RO | 15~9 | Reserved | | 0 |
| | | RO/LH/COR | 8 | High-Power-down State Latch | 1: Latched. | 0 |
| | | RO/LH/COR | 7 | TX-Turn-off State Latch | 1: Latched. | 0 |
| | | RO/LH/COR | 6 | Fault State Latch | 1: Latched. | 0 |
| | | RO/LH/COR | 5 | Ready State Latch | 1: Latched. | 0 |
| | | RO/LH/COR | 4 | TX-Turn-on State Latch | 1: Latched. | 0 |
| | | RO/LH/COR | 3 | TX-Off State Latch | 1: Latched. | 0 |
| | | RO/LH/COR | 2 | High-Power-up State Latch | 1: Latched. | 0 |
| | | RO/LH/COR | 1 | Low-Power State Latch | 1: Latched. | 0 |
| | | RO/LH/COR | 0 | Initialize State Latch | 1: Latched. | 0 |
| **A023** | **1** | | | **Module General Status Latch** | | **0000h** |
| | | RO | 15 | Reserved | | 0 |
| | | RO | 14 | Reserved | | 0 |
| | | RO/LH/COR | 13 | HW_Interlock Latch | 1: Latched. | 0 |
| | | RO | 12~11 | Reserved | | 0 |
| | | RO/LH/COR | 10 | Loss of REFCLK Input Latch | 1: Latched. | 0 |
| | | RO/LH/COR | 9 | TX_JITTER_PLL_LOL Latch | 1: Latched. | 0 |
| | | RO/LH/COR | 8 | TX_CMU_LOL Latch | 1: Latched. | 0 |
| | | RO/LH/COR | 7 | TX_LOSF Latch | 1: Latched.<br>**Note:** Set to 1 on any change (0-->1 or 1 --> 0) of the corresponding status signal. | 0 |
| | | RO/LH/COR | 6 | TX_HOST_LOL Latch | 1: Latched.<br>**Note:** Set to 1 on any change (0-->1 or 1 --> 0) of the corresponding status signal. | 0 |
| | | RO/LH/COR | 5 | RX_LOS Latch | 1: Latched.<br>**Note:** Set to 1 on any change (0-->1 or 1 --> 0) of the corresponding status signal. | 0 |
| | | RO/LH/COR | 4 | RX_NETWORK_LOL Latch | 1: Latched.<br>**Note:** Set to 1 on any change (0-->1 or 1 --> 0) of the corresponding status signal. | 0 |

| CFP Module VR 1 | | | | | | |
|---|---|---|---|---|---|---|
| ***Hex Addr.*** | ***Size*** | ***Access Type*** | ***Bit*** | ***Register Name*** *Bit Field Name* | ***Description*** | ***Init Value*** |
| | | RO/LH/COR | 3 | Out of Alignment Latch | 1: Latched. | 0 |
| | | RO | 2~0 | Reserved | | 000b |
| **A024** | **1** | | | **Module Fault Status Latch** | **Module Fault Status latched bit pattern.** | **0000h** |
| | | RO | 15~7 | Reserved | | 0 |
| | | RO/LH/COR | 6 | PLD or Flash Initialization Fault Latch | 1: Latched. | 0 |
| | | RO/LH/COR | 5 | Power Supply Fault Latch | 1: Latched. | 0 |
| | | RO | 4~2 | Reserved | | 000b |
| | | RO/LH/COR | 1 | CFP Checksum Fault Latch | 1: Latched. | 0 |
| | | RO | 0 | Reserved | | 0 |
| **A025** | **1** | | | **Module Alarms and Warnings 1 Latch** | | **0000h** |
| | | RO | 15~12 | Reserved | | 0000b |
| | | RO/LH/COR | 11 | Mod Temp High Alarm Latch | 1: Latched. | 0 |
| | | RO/LH/COR | 10 | Mod Temp High Warning Latch | 1: Latched. | 0 |
| | | RO/LH/COR | 9 | Mod Temp Low Warning Latch | 1: Latched. | 0 |
| | | RO/LH/COR | 8 | Mod Temp Low Alarm Latch | 1: Latched. | 0 |
| | | RO/LH/COR | 7 | Mod Vcc High Alarm Latch | 1: Latched. | 0 |
| | | RO/LH/COR | 6 | Mod Vcc High Warning Latch | 1: Latched. | 0 |
| | | RO/LH/COR | 5 | Mod Vcc Low Warning Latch | 1: Latched. | 0 |
| | | RO/LH/COR | 4 | Mod Vcc Low Alarm Latch | 1: Latched. | 0 |
| | | RO/LH/COR | 3 | Mod SOA Bias High Alarm Latch | 1: Latched. | 0 |
| | | RO/LH/COR | 2 | Mod SOA Bias High Warning Latch | 1: Latched. | 0 |
| | | RO/LH/COR | 1 | Mod SOA Bias Low Warning Latch | 1: Latched. | 0 |
| | | RO/LH/COR | 0 | Mod SOA Bias Low Alarm Latch | 1: Latched. | 0 |
| **A026** | **1** | | | **Module Alarms and Warnings 2 Latch** | | 0 |
| | | RO | 15~8 | Reserved | | 0 |
| | | RO/LH/COR | 7 | Mod Aux 1 High Alarm Latch | 1: Latched. | 0 |
| | | RO/LH/COR | 6 | Mod Aux 1 High Warning Latch | 1: Latched. | 0 |
| | | RO/LH/COR | 5 | Mod Aux 1 Low Warning Latch | 1: Latched. | 0 |
| | | RO/LH/COR | 4 | Mod Aux 1 Low Alarm Latch | 1: Latched. | 0 |
| | | RO/LH/COR | 3 | Mod Aux 2 High Alarm Latch | 1: Latched. | 0 |
| | | RO/LH/COR | 2 | Mod Aux 2 High Warning Latch | 1: Latched. | 0 |
| | | RO/LH/COR | 1 | Mod Aux 2 Low Warning Latch | 1: Latched. | 0 |
| | | RO/LH/COR | 0 | Mod Aux 2 Low Alarm Latch | 1: Latched. | 0 |

| CFP Module VR 1 | | | | | | |
|---|---|---|---|---|---|---|
| ***Hex Addr.*** | ***Size*** | ***Access Type*** | ***Bit*** | ***Register Name*** *Bit Field Name* | ***Description*** | ***Init Value*** |
| **A027** | **1** | **RO** | | **Reserved** | | 0 |
| **Module FAWS Enable Registers** | | | | | | |
| **A028** | **1** | | | **Module State Enable** | **GLB_ALRM Enable register for Module State change. One bit for each state.** | **006Ah** |
| | | RO | 15~9 | Reserved | | 0 |
| | | RW | 8 | High-Power-down State Enable | 1: Enable corresponding signal to assert GLB_ALRM. | 0 |
| | | RW | 7 | TX-Turn-off State Enable | 1: Enable corresponding signal to assert GLB_ALRM. | 0 |
| | | RW | 6 | Fault State Enable | 1: Enable corresponding signal to assert GLB_ALRM. (Init Value is 1 to allow GLB_ALRM in startup sequence.) | 1 |
| | | RW | 5 | Ready State Enable | 1: Enable corresponding signal to assert GLB_ALRM. (Init Value is 1 to allow GLB_ALRM in startup sequence.) | 1 |
| | | RW | 4 | TX-Turn-on State Enable | 1: Enable corresponding signal to assert GLB_ALRM. | 0 |
| | | RW | 3 | TX-Off State Enable | 1: Enable corresponding signal to assert GLB_ALRM. (Init Value is 1 to allow GLB_ALRM in startup sequence.) | 1 |
| | | RW | 2 | High-Power-up State Enable | 1: Enable corresponding signal to assert GLB_ALRM. | 0 |
| | | RW | 1 | Low-Power State Enable | 1: Enable corresponding signal to assert GLB_ALRM. (Init Value is 1 to allow GLB_ALRM in startup sequence) | 1 |
| | | RO | 0 | Initialize State Enable | 1: Enable corresponding signal to assert GLB_ALRM. | 0 |
| **A029** | **1** | | | **Module General Status Enable** | **1: Enable signal to assert GLB_ALRM. Bits 14~0 are AND'ed with corresponding bits in the Module General Status Latch register; the result is used to assert GLB_ALRM. Bit 15 is the master enable of GLB_ALRM and it is AND'ed with the output of the "OR" gate output in Global Alarm Signal Aggregation, Figure 10.** | **A0F0h** |
| | | RW | 15 | GLB_ALRM Master Enable | 1: Enable. | 1 |
| | | RO | 14 | Reserved | | 0 |
| | | RW | 13 | HW_Interlock | 1: Enable. | 1 |
| | | RO | 12~11 | Reserved | | 0 |
| | | RW | 10 | Loss of REFCLK Input Enable | 1: Enable. | 1 |
| | | RW | 9 | TX_JITTER_PLL_LOL Enable | 1: Enable. | 1 |
| | | RW | 8 | TX_CMU_LOL Enable | 1: Enable. | 1 |
| | | RW | 7 | TX_LOSF Enable | 1: Enable. | 1 |
| | | RW | 6 | TX_HOST_LOL Enable | 1: Enable. | 1 |
| | | RW | 5 | RX_LOS Enable | 1: Enable. | 1 |
| | | RW | 4 | RX_NETWORK_LOL Enable | 1: Enable. | 1 |
| | | RW | 3 | Out of Alignment Enable | 1. Enable. | 1 |
| | | RO | 2~0 | Reserved | | 000b |
| **A02A** | **1** | | | **Module Fault Status Enable** | **These bits are AND'ed with corresponding bits in the Module Fault Latch register; the result is used to assert GLB_ALRM. Optional features that are not implemented shall have their Enable bit forced to '0'.** | **0062h** |
| | | RO | 15~7 | Reserved | | 0 |
| | | RW | 6 | PLD or Flash Initialization Fault Enable | 1: Enable. | 1 |
| | | RW | 5 | Power Supply Fault Enable | 1: Enable. | 1 |
| | | RO | 4~2 | Reserved | | 000b |
| | | RW | 1 | CFP Checksum Fault Enable | 1: Enable. | 1 |
| | | RO | 0 | Reserved | | 0 |
| **A02B** | **1** | | | **Module Alarm and** | **These bits are AND'ed with corresponding bits in the** | **0FFFh** |

| CFP Module VR 1 | | | | | | |
|---|---|---|---|---|---|---|
| ***Hex Addr.*** | ***Size*** | ***Access Type*** | ***Bit*** | ***Register Name*** *Bit Field Name* | ***Description*** | ***Init Value*** |
| | | | | **Warnings 1 Enable** | **Module Alarm and Warnings 1 Latch register; the result is used to assert GLB_ALRM. Optional features that are not implemented shall have their Enable bit forced to '0'.** | |
| | | RO | 15~12 | Reserved | | 0000b |
| | | RW | 11 | Mod Temp Hi Alarm Enable | 1: Enable. | 1 |
| | | | 10 | Mod Temp Hi Warn Enable | 1: Enable. | 1 |
| | | | 9 | Mod Temp Low Warning Enable | 1: Enable. | 1 |
| | | | 8 | Mod Temp Low Alarm Enable | 1: Enable. | 1 |
| | | | 7 | Mod Vcc High Alarm Enable | 1: Enable. | 1 |
| | | | 6 | Mod Vcc High Warning Enable | 1: Enable. | 1 |
| | | | 5 | Mod Vcc Low Warning Enable | 1: Enable. | 1 |
| | | | 4 | Mod Vcc Low Alarm Enable | 1: Enable. | 1 |
| | | | 3 | Mod SOA Bias High Alarm Enable | 1: Enable. | 1 |
| | | | 2 | Mod SOA Bias High Warning Enable | 1: Enable. | 1 |
| | | | 1 | Mod SOA Bias Low Warning Enable | 1: Enable. | 1 |
| | | | 0 | Mod SOA Bias Low Alarm Enable | 1: Enable. | 1 |
| **A02C** | **1** | | | **Module Alarms and Warnings 2 Enable** | **These bits are AND'ed with corresponding bits in the Module Alarm and Warnings 2 Latch register; the result is used to assert GLB_ALRM. Optional features that are not implemented shall have their Enable bit forced to '0'.** | **00FFh** |
| | | RO | 15~8 | Reserved | | 00h |
| | | RW | 7 | Mod Aux 1 High Alarm Enable | 1: Enable. | 1 |
| | | | 6 | Mod Aux 1 High Warning Enable | 1: Enable. | 1 |
| | | | 5 | Mod Aux 1 Low Warning Enable | 1: Enable. | 1 |
| | | | 4 | Mod Aux 1 Low Alarm Enable | 1: Enable. | 1 |
| | | | 3 | Mod Aux 2 High Alarm Enable | 1: Enable. | 1 |
| | | | 2 | Mod Aux 2 High Warning Enable | 1: Enable. | 1 |
| | | | 1 | Mod Aux 2 Low Warning Enable | 1: Enable. | 1 |
| | | | 0 | Mod Aux 2 Low Alarm Enable | 1: Enable. | 1 |
| **A02D** | **2** | **RO** | | **Reserved** | | **0000h** |
| **Module Analog A/D Value Registers** | | | | | | |
| **A02F** | **1** | **RO** | **15~0** | **Module Temp Monitor A/D Value** | **Internally measured temperature in degrees Celsius, a 16-bit signed integer with LSB = 1/256 of a degree Celsius, representing a total range from -128 to + 127 255/256 degC. MSA valid range is between –40 and +125C. Accuracy shall be better than +/- 3 degC over the whole temperature range.** | **0000h** |
| **A030** | **1** | **RO** | **15~0** | **Module Power supply** | **Internally measured transceiver supply voltage, a 16-bit** | **0000h** |

| CFP Module VR 1 | | | | | | |
|---|---|---|---|---|---|---|
| ***Hex Addr.*** | ***Size*** | ***Access Type*** | ***Bit*** | ***Register Name*** *Bit Field Name* | ***Description*** | ***Init Value*** |
| | | | | **3.3 V Monitor A/D Value** | **unsigned integer with LSB = 0.1 mV, yielding a total measurement range of 0 to 6.5535 Volts. Accuracy shall be better than +/-3% of the nominal value over specified operating temperature and voltage range.** | |
| **A031** | **1** | **RO** | **15~0** | **SOA Bias Current A/D Value** | **Measured SOA bias current in uA, a 16-bit unsigned integer with LSB = 2 uA, representing a total range of from 0 to 131.072 mA. Accuracy shall be better than +/-10% of the nominal value over specified temperature and voltage.** | **0000h** |
| **A032** | **1** | **RO** | **15~0** | **Module Auxiliary 1 Monitor A/D Value** | **Definition depending upon the designated use.** | **0000h** |
| **A033** | **1** | **RO** | **15~0** | **Module Auxiliary 2 Monitor A/D Value** | **Definition depending upon the designated use.** | **0000h** |
| **A034** | **4** | **RO** | | **Reserved** | | |
| **Module PRBS Registers** | | | | | | |
| **A038** | **1** | **RO** | | **Network Lane PRBS Data Bit Count** | **Network lane data bit counter increments when network lane RX PRBS Checker is enabled. It stops counting when RX PRBS Checker is disabled. It uses an ad-hoc format floating point number with 6-bit unsigned exponent and 10-bit unsigned mantissa.** | **0000h** |
| | | | 15~10 | Exponent | 6-bit unsigned exponent. | 0 |
| | | | 9~0 | Mantissa | 10-bit mantissa giving better than 0.1% accuracy in bit counts. | 0 |
| **A039** | **1** | | | **Host Lane PRBS Data Bit Count** | **Host lane data bit counter increments when host side TX PRBS Checker is enabled. It stops counting when TX PRBS Checker is disabled. It uses an ad-hoc format floating point number with 6-bit unsigned exponent and 10-bit unsigned mantissa.** | **0000h** |
| | | RO | 15~10 | Exponent | 6-bit unsigned exponent | 0 |
| | | RO | 9~0 | Mantissa | 10-bit mantissa giving better than 0.1% accuracy in bit counts. | 0 |
| **A03A** | **70** | **RO** | | **Reserved** | | **0** |

## 5.6 Network Lane Specific Register Tables

*Table 23 Network Lane VR 1* and *Table 24 Network Lane VR 2* contain network lane specific registers. Each register listed is the $n_{th}$ element of a 16-register array, representing the $n_{th}$ network lane of N total network lanes. The maximum N CFP MSA specifies is 16. All the register information is detailed in the description column. The registers of all the unused lanes shall be set to zero initial value.

*Table 23 Network Lane VR 1*

| Network Lane VR 1 | | | | | | |
|---|---|---|---|---|---|---|
| ***Hex Addr*** | ***Size*** | ***Access Type*** | ***Bit*** | ***Register Name*** *Bit Field Name* | ***Description*** | ***Init Value*** |
| **Network Lane FAWS Registers** | | | | | | |
| **A200** | **16** | **RO** | | **Network Lane n Alarm and Warning** | **16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent.** | **0000h** |
| | | | 15 | Bias High Alarm | 0: Normal; 1: Asserted. (FAWS_TYPE_C) | 0 |
| | | | 14 | Bias High Warning | 0: Normal; 1: Asserted. (FAWS_TYPE_C) | 0 |

| Network Lane VR 1 | | | | | | |
|---|---|---|---|---|---|---|
| ***Hex Addr*** | ***Size*** | ***Access Type*** | ***Bit*** | ***Register Name*** *Bit Field Name* | ***Description*** | ***Init Value*** |
| | | | 13 | Bias Low Warning | 0: Normal; 1: Asserted. (FAWS_TYPE_C) | 0 |
| | | | 12 | Bias Low Alarm | 0: Normal; 1: Asserted. (FAWS_TYPE_C) | 0 |
| | | | 11 | TX Power High Alarm | 0: Normal; 1: Asserted. (FAWS_TYPE_C) | 0 |
| | | | 10 | TX Power High Warning | 0: Normal; 1: Asserted. (FAWS_TYPE_C) | 0 |
| | | | 9 | TX Power Low Warning | 0: Normal; 1: Asserted. (FAWS_TYPE_C) | 0 |
| | | | 8 | TX Power Low Alarm | 0: Normal; 1: Asserted. (FAWS_TYPE_C) | 0 |
| | | | 7 | Laser Temperature High Alarm | 0: Normal; 1: Asserted. (FAWS_TYPE_B) | 0 |
| | | | 6 | Laser Temperature High Warning | 0: Normal; 1: Asserted. (FAWS_TYPE_B) | 0 |
| | | | 5 | Laser Temperature Low Warning | 0: Normal; 1: Asserted. (FAWS_TYPE_B) | 0 |
| | | | 4 | Laser Temperature Low Alarm | 0: Normal; 1: Asserted. (FAWS_TYPE_B) | 0 |
| | | | 3 | RX Power High Alarm | 0: Normal; 1: Asserted. (FAWS_TYPE_B) | 0 |
| | | | 2 | RX Power High Warning | 0: Normal; 1: Asserted. (FAWS_TYPE_B) | 0 |
| | | | 1 | RX Power Low Warning | 0: Normal; 1: Asserted. (FAWS_TYPE_B) | 0 |
| | | | 0 | RX Power Low Alarm | 0: Normal; 1: Asserted. (FAWS_TYPE_B) | 0 |
| **A210** | **16** | **RO** | | **Network Lane n Fault and Status** | **16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent.** | **0000h** |
| | | | 15 | Lane TEC Fault | 0: Normal; 1: Asserted. (FAWS_TYPE_B) | 0 |
| | | | 14 | Lane Wavelength Unlocked Fault | 0: Normal; 1: Asserted. (FAWS_TYPE_C) | 0 |
| | | | 13 | Lane APD Power Supply Fault | 0: Normal; 1: Asserted. (FAWS_TYPE_B) | 0 |
| | | | 12~8 | Reserved | | 0 |
| | | | 7 | Lane TX_LOSF | 0: Normal; 1: Asserted. (PMD) (FAWS_TYPE_C) | 0 |
| | | | 6 | Lane TX_LOL | 0: Normal; 1: Asserted. (Network) (FAWS_TYPE_B) | 0 |
| | | | 5 | Reserved | | 0 |
| | | | 4 | Lane RX_LOS | 0: Normal; 1: Asserted. (FAWS_TYPE_B) | 0 |
| | | | 3 | Lane RX_LOL | 0: Normal; 1: Asserted. (FAWS_TYPE_B) | 0 |
| | | | 2 | Lane RX FIFO error | 0: Normal, 1: Error. (FAWS_TYPE_B) | 0 |
| | | | 1 | Reserved. | | 0 |
| | | | 0 | Reserved. | | 0 |
| **Network Lane FAWS Latch Registers** | | | | | | |
| **A220** | **16** | **RO/LH/COR** | | **Network Lane n Alarm and Warning Latch** | **16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent.** | **0000h** |
| | | | 15 | Bias High Alarm Latch | 1: Latched. | 0 |
| | | | 14 | Bias High Warning Latch | 1: Latched. | 0 |
| | | | 13 | Bias Low Warning Latch | 1: Latched. | 0 |
| | | | 12 | Bias Low Alarm Latch | 1: Latched. | 0 |
| | | | 11 | TX Power High Alarm Latch | 1: Latched. | 0 |
| | | | 10 | TX Power High Warning Latch | 1: Latched. | 0 |
| | | | 9 | TX Power Low Warning Latch | 1: Latched. | 0 |
| | | | 8 | TX Power Low Alarm Latch | 1: Latched. | 0 |
| | | | 7 | Laser Temperature High Alarm Latch | 1: Latched. | 0 |
| | | | 6 | Laser Temperature High Warning Latch | 1: Latched. | 0 |
| | | | 5 | Laser Temperature Low Warning Latch | 1: Latched. | 0 |
| | | | 4 | Laser Temperature Low Alarm Latch | 1: Latched. | 0 |
| | | | 3 | RX Power High Alarm Latch | 1: Latched. | 0 |
| | | | 2 | RX Power High Warning Latch | 1: Latched. | 0 |
| | | | 1 | RX Power Low Warning Latch | 1: Latched. | 0 |
| | | | 0 | RX Power Low Alarm Latch | 1: Latched. | 0 |

| Network Lane VR 1 | | | | | | |
|---|---|---|---|---|---|---|
| ***Hex Addr*** | ***Size*** | ***Access Type*** | ***Bit*** | ***Register Name*** *Bit Field Name* | ***Description*** | ***Init Value*** |
| **A230** | **16** | | | **Network Lane n Fault and Status Latch** | **16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent.** | **0000h** |
| | | RO/LH/COR | 15 | Lane TEC Fault Latch | 1: Latched. | 0 |
| | | RO/LH/COR | 14 | Lane Wavelength Unlocked Fault Latch | 1: Latched. | 0 |
| | | RO/LH/COR | 13 | Lane APD Power Supply Fault Latch | 1: Latched. | 0 |
| | | RO | 12~8 | Reserved | | 0 |
| | | RO/LH/COR | 7 | Lane TX_LOSF Latch | 1: Latched. | 0 |
| | | RO/LH/COR | 6 | Lane TX_LOL Latch | 1: Latched. | 0 |
| | | RO | 5 | Reserved | | 0 |
| | | RO/LH/COR | 4 | Lane RX_LOS Latch | 1: Latched. | 0 |
| | | RO/LH/COR | 3 | Lane RX_LOL Latch | 1: Latched. | 0 |
| | | RO/LH/COR | 2 | Lane RX FIFO Status Latch | 1: Latched. | 0 |
| | | RO | 1~0 | Reserved | | 0 |
| **Network Lane FAWS Enable Registers** | | | | | | |
| **A240** | **16** | **RW** | | **Network Lane n Alarm and Warning Enable** | **16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent.** | **FFFFh** |
| | | | 15 | Bias High Alarm Enable | 0: Disable, 1: Enable. | 1 |
| | | | 14 | Bias High Warning Enable | 0: Disable, 1: Enable. | 1 |
| | | | 13 | Bias Low Warning Enable | 0: Disable, 1: Enable. | 1 |
| | | | 12 | Bias Low Alarm Enable | 0: Disable, 1: Enable. | 1 |
| | | | 11 | TX Power High Alarm Enable | 0: Disable, 1: Enable. | 1 |
| | | | 10 | TX Power High Warning Enable | 0: Disable, 1: Enable. | 1 |
| | | | 9 | TX Power Low Warning Enable | 0: Disable, 1: Enable. | 1 |
| | | | 8 | TX Power Low Alarm Enable | 0: Disable, 1: Enable. | 1 |
| | | | 7 | Laser Temperature High Alarm Enable | 0: Disable, 1: Enable. | 1 |
| | | | 6 | Laser Temperature High Warning Enable | 0: Disable, 1: Enable. | 1 |
| | | | 5 | Laser Temperature Low Warning Enable | 0: Disable, 1: Enable. | 1 |
| | | | 4 | Laser Temperature Low Alarm Enable | 0: Disable, 1: Enable. | 1 |
| | | | 3 | RX Power High Alarm Enable | 0: Disable, 1: Enable. | 1 |
| | | | 2 | RX Power High Warning Enable | 0: Disable, 1: Enable. | 1 |
| | | | 1 | RX Power Low Warning Enable | 0: Disable, 1: Enable. | 1 |
| | | | 0 | RX Power Low Alarm Enable | 0: Disable, 1: Enable. | 1 |
| **A250** | **16** | | | **Network Lane n Fault and Status Enable** | **16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent.** | **E0D8h** |
| | | RW | 15 | Lane TEC Fault Enable | 0: Disable, 1: Enable. | 1 |
| | | RW | 14 | Lane Wavelength Unlocked Fault Enable | 0: Disable, 1: Enable. | 1 |
| | | RW | 13 | Lane APD Power Supply Fault Enable | 0: Disable, 1: Enable. | 1 |

| Network Lane VR 1 | | | | | | |
|---|---|---|---|---|---|---|
| ***Hex Addr*** | ***Size*** | ***Access Type*** | ***Bit*** | ***Register Name*** *Bit Field Name* | ***Description*** | ***Init Value*** |
| | | RO | 12~8 | Reserved | | 0 |
| | | RW | 7 | Lane TX_LOSF Enable | 0: Disable, 1: Enable. | 1 |
| | | RW | 6 | Lane TX_LOL Enable | 0: Disable, 1: Enable. | 1 |
| | | RO | 5 | Reserved | | 0 |
| | | RW | 4 | Lane RX_LOS Enable | 0: Disable, 1: Enable. | 1 |
| | | RW | 3 | Lane RX_LOL Enable | 0: Disable, 1: Enable. | 1 |
| | | RW | 2 | Lane RX FIFO Status Enable | 0: Disable, 1: Enable. | 1 |
| | | RO | 1~0 | Reserved | | 0 |
| **A260** | **32** | **RO** | | **Reserved** | | **0000h** |

*Table 24 Network Lane VR 2*

| Network Lane VR 2 | | | | | | |
|---|---|---|---|---|---|---|
| ***Hex Addr*** | ***Size*** | ***Access Type*** | ***Bit*** | ***Register Name*** *Bit Field Name* | ***Description*** | ***Init Value*** |
| **Network Lane Control Registers** | | | | | | |
| **A280** | **16** | | | **Network Lane n FEC Controls** | **16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent.** | **0000h** |
| | | RW | 15~8 | Phase Adjustment | This signed 8-bit value represents the phase set point of receive path quantization relative to 0.5 UI, given by: 0.5UI + (Phase Adjustment) / 256 UI. (Optional function) Set this value = -128 (80h) to de-activate this function. | 00h |
| | | RW | 7~0 | Amplitude Adjustment | This signed 8-bit value represents the amplitude threshold of relative amplitude of receive path quantization relative to 50% (Optional function), given by: 50% + (Amplitude Adjustment) / 256 * 100%. (Optional function) Set this value = -128 (80h) to de-activate this function. | 00h |
| **A290** | **16** | **RO** | **15~0** | **Network Lane n PRBS Rx Error Count** | **16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent. This counter increases upon detection of each network lane RX checker error when RX PRBS Checker is enabled. It uses an ad-hoc floating point number format with a 6-bit unsigned exponent and a 10-bit unsigned mantissa. Base of exponent is 2 and Mantissa radix is 0.** | **0000h** |
| | | | 15~10 | Exponent | 6-bit unsigned exponent. | 0 |
| | | | 9~0 | Mantissa | 10-bit mantissa giving better than 0.1% accuracy in bit counts. | 0 |
| **Network Lane A/D value Measurement Registers** | | | | | | |
| **A2A0** | **16** | **RO** | **15~0** | **Network Lane n Laser Bias Current monitor A/D value** | **16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent. Measured laser bias current in uA, a 16-bit unsigned integer with LSB = 2 uA, representing a total measurement range of 0 to 131.072 mA. Minimum accuracy shall be +/- 10% of the nominal value over temperature and voltage.** | **0000h** |

| Network Lane VR 2 | | | | | | |
|---|---|---|---|---|---|---|
| ***Hex Addr*** | ***Size*** | ***Access Type*** | ***Bit*** | ***Register Name*** *Bit Field Name* | ***Description*** | ***Init Value*** |
| **A2B0** | **16** | **RO** | **15~0** | **Network Lane n Laser Output Power monitor A/D value** | **16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent. Measured TX output power in uW, a 16-bit unsigned integer with LSB = 0.1 uW, representing a range of laser output power from 0 to 6.5535 mW (-40 to +8.2 dBm). Accuracy must be better than +/- 2 dB over temperature and voltage range. Relative accuracy must be better than 1 dB.** | **0000h** |
| **A2C0** | **16** | **RO** | **15~0** | **Network Lane n Laser Temp Monitor A/D value** | **16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent. Internally measured temperature in degrees Celsius, a 16-bit signed integer with LSB = 1/256 of a degree Celsius, representing a total range from -128 to + 127 255/256 degC. MSA valid range is between –40 and +125C. Minimum accuracy is +/- 3 degC over temperature range.** | **0000h** |
| **A2D0** | **16** | **RO** | **15~0** | **Network Lane n Receiver Input Power monitor A/D value** | **16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent. Measured received input power in uW, a 16-bit unsigned integer with LSB = 0.1 uW, representing a power range from 0 to 6.5535 mW (-40 to +8.2 dBm). Value can represent either average received power or OMA depending upon how bit 3 of Register 8080h is set. Accuracy must be better than +/- 2dB over temperature and voltage. This accuracy shall be maintained for input power levels up to the lesser of maximum transmitted or maximum received optical power per the appropriate standard. It shall be maintained down to the minimum transmitted power minus cable plant loss per the appropriate standard. Relative accuracy shall be better than 1 dB over the received power range, temperature range, voltage range, and the life of the product.** | **0000h** |
| **A2E0** | **32** | **RO** | **15~0** | **Reserved** | | **0000h** |

## 5.7 Host lane Specific Register Table

*Table 25 Host Lane VR 1* contains host lane specific registers. Each register listed is the $m^{th}$ element of a 16-register array, representing the $m^{th}$ host lane of M total host lanes. The maximum M CFP MSA specifies is 16. All the register information is detailed in the description column. The registers of all the unused lanes shall be set to zero initial value.

1 *Table 25 Host Lane VR 1*

| Host Lane VR 1 | | | | | | |
|---|---|---|---|---|---|---|
| ***Hex Addr*** | ***Size*** | ***Access Type*** | ***Bit*** | ***Register Name*** *Bit Field Name* | ***Description*** | ***Init Value*** |
| **Host Lane FAWS Status Registers** | | | | | | |
| **A400** | **16** | | | **Host Lane m Fault and Status** | **16 registers, one for each host lane, represent 16 host lanes. m = 0, 1, …, M-1. M_max = 16. Actual M is module dependent.** | **0000h** |
| | | RO | 15~2 | Reserved | | 0 |
| | | RO | 1 | Lane TX FIFO Error | Lane specific TX FIFO error. (FAWS_TYPE_B)<br>0: Normal, 1: Error. | 0 |
| | | RO | 0 | TX_HOST_LOL | TX IC Lock Indicator, (FAWS_TYPE_B)<br>0: Locked,<br>1: Loss of lock. | 0 |
| **Host Lane FAWS Latch Registers** | | | | | | |
| **A410** | **16** | | | **Host Lane m Fault and Status Latch** | **16 registers, one for each host lane, represent 16 host lanes. m = 0, 1, …, M-1. M_max = 16. Actual M is module dependent.** | **0000h** |
| | | RO | 15~2 | Reserved | | 0 |
| | | RO/LH/COR | 1 | Lane TX FIFO Error Latch | 1: Latched. | 0 |
| | | RO/LH/COR | 0 | TX_HOST_LOL Latch | 1: Latched. | 0 |
| **Host Lane FAWS Enable Registers** | | | | | | |
| **A420** | **16** | | | **Host Lane m Fault and Status Enable** | **16 registers, one for each host lane, represent 16 host lanes. m = 0, 1, …, M-1. M_max = 16. Actual M is module dependent.** | **0001h** |
| | | RO | 15~2 | Reserved | | 0 |
| | | RW | 1 | Lane TX FIFO Error Enable | 1: Enable. | 0 |
| | | RW | 0 | TX_HOST_LOL Enable | 1: Enable. | 1 |
| **Host Lane Digital PRBS Registers** | | | | | | |
| **A430** | **16** | **RO** | | **Host Lane m PRBS TX Error Count** | **16 registers, one for each host lane, represent 16 host lanes. m = 0, 1, …, M-1. M_max = 16. Actual M is module dependent. This counter increases upon detection of each RX checker error when host lane TX PRBS checker is enabled. It stops counting when the TX PRBS checker is disabled. It uses an ad-hoc floating point number format with a 6-bit unsigned exponent and a 10-bit unsigned mantissa.** | **0000h** |
| | | | 15~10 | Exponent | 6-bit unsigned exponent. | 0 |
| | | | 9~0 | Mantissa | 10-bit mantissa giving better than 0.1% accuracy in bit counts. | 0 |
| **Host Lane Control Registers** | | | | | | |
| **A440** | **16** | | | **Host Lane m Control** | **16 registers, one for each host lane, represent 16 host lanes. m = 0, 1, …, M-1. M_max = 16. Actual M is module dependent.** | **0007h** |
| | | RO | 15~4 | Reserved | | 0 |
| | | RW | 3~0 | Signal Pre/De-emphasis | 4-bit unsigned number N represents the pre/de-emphasis applied.<br>Pre/De-emphasis = N * 0.5 dB, N = 0, …, 15.<br>The power on default is 3.5 dB with a value of 7 in this field. | 7 |
| **A450** | **48** | **RO** | | **Reserved** | | **0000h** |

3
4 END OF DOCUMENT (V1.4 R5)