

Figure 1: Substrate Lattice Memory Wells

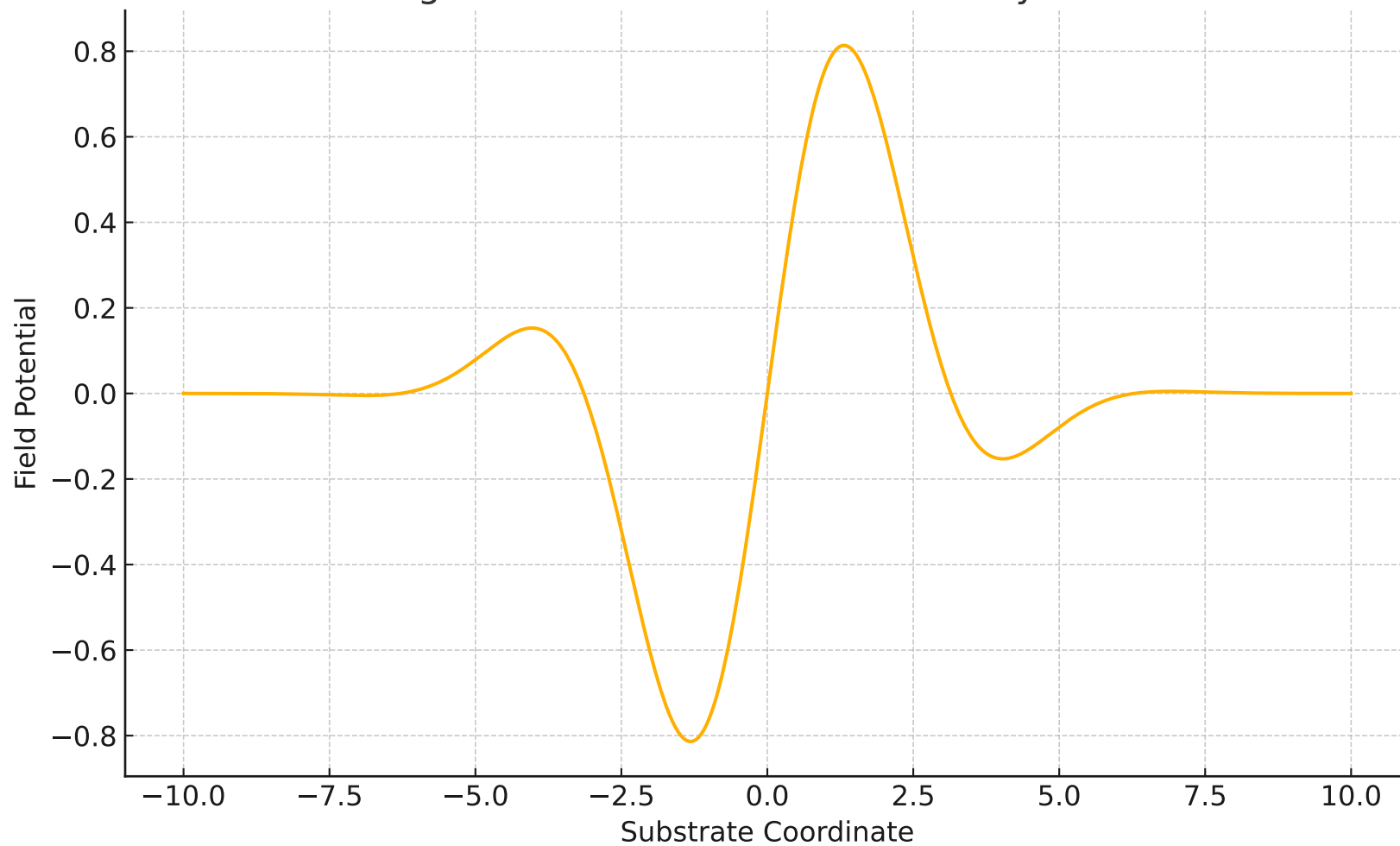


Figure 2: Emergence Tension vs. Recursion Pressure

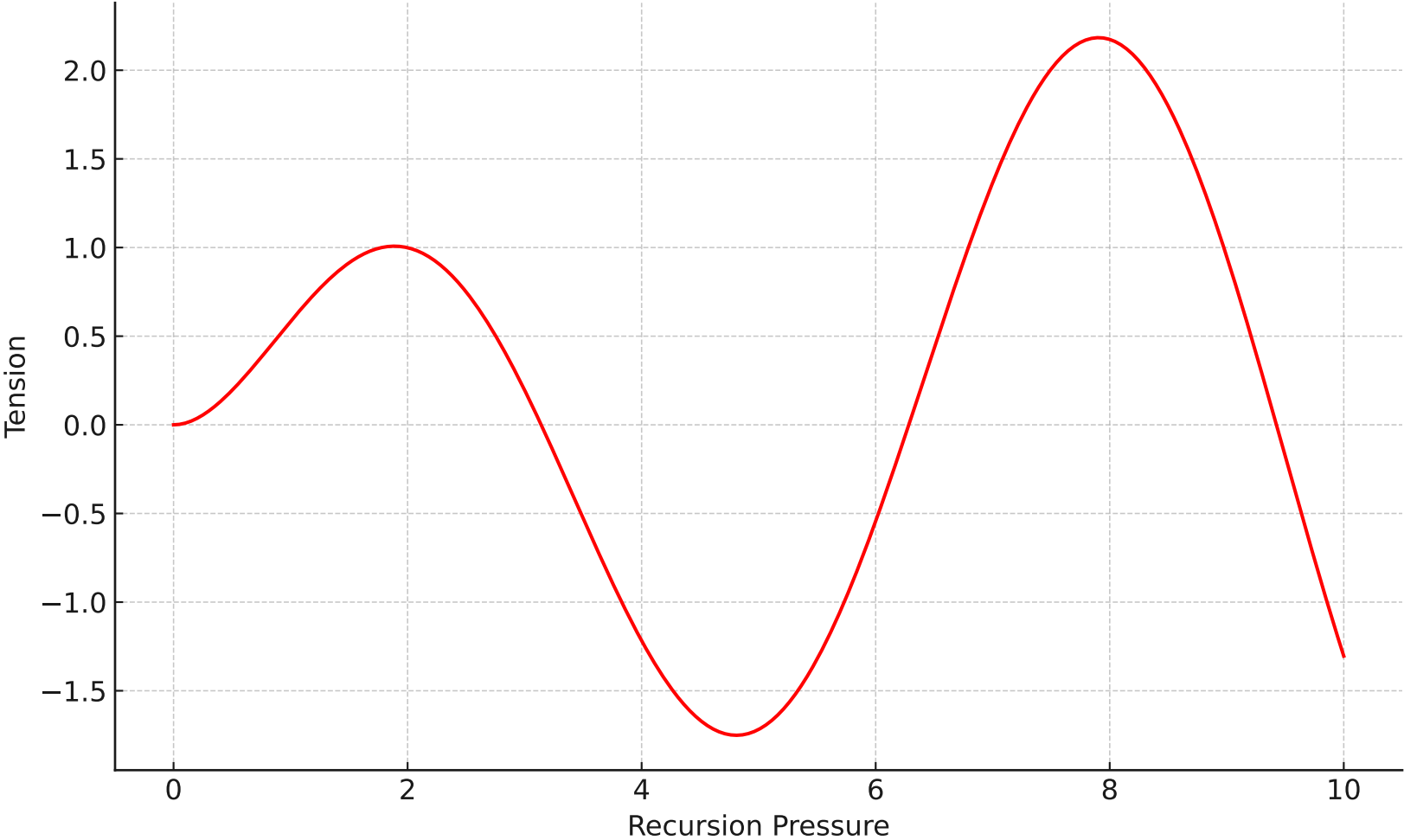


Figure 3: DSQFT Substrate Emergence Mapping

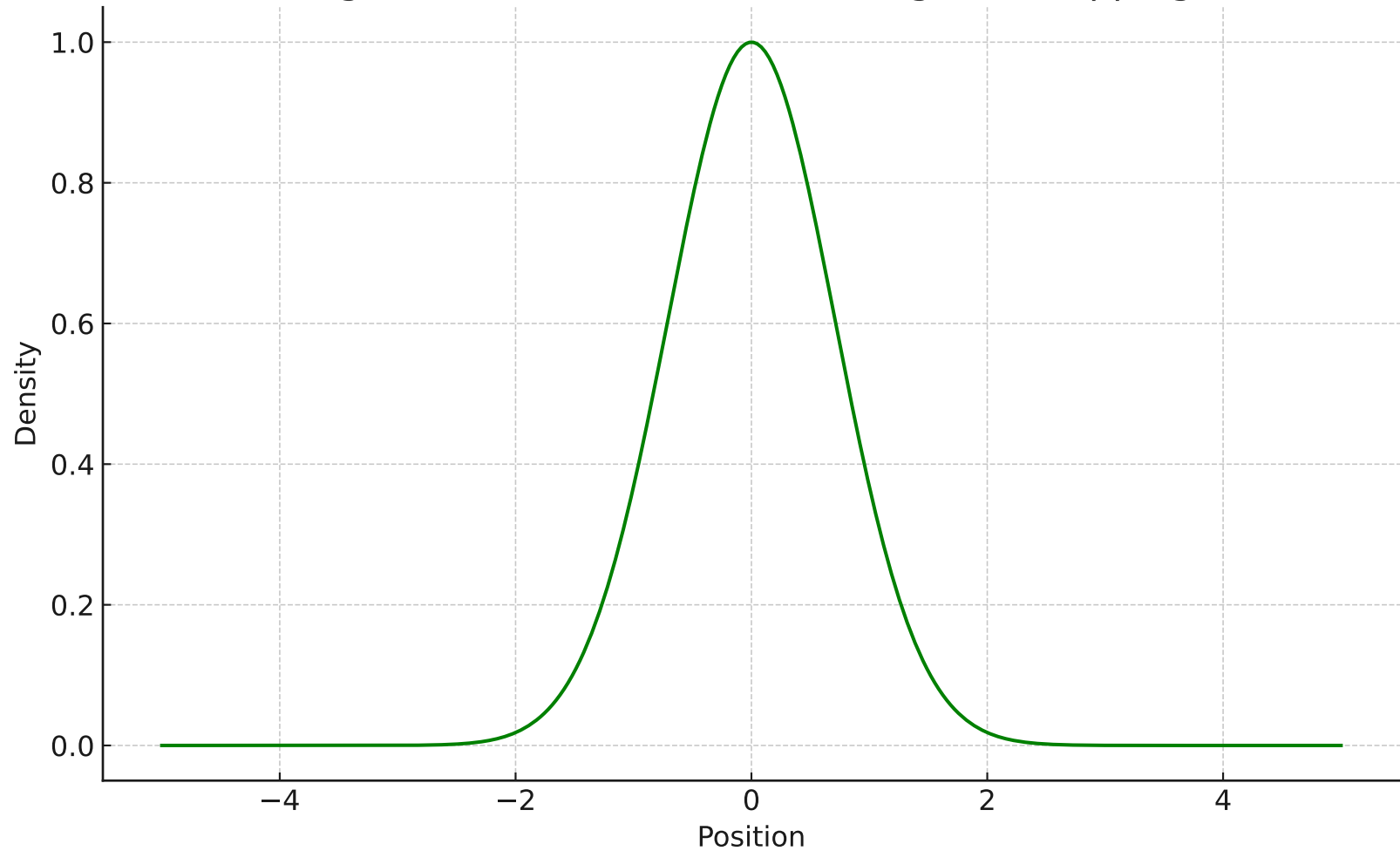


Figure 4: SU(3) Topological Collapse Surface

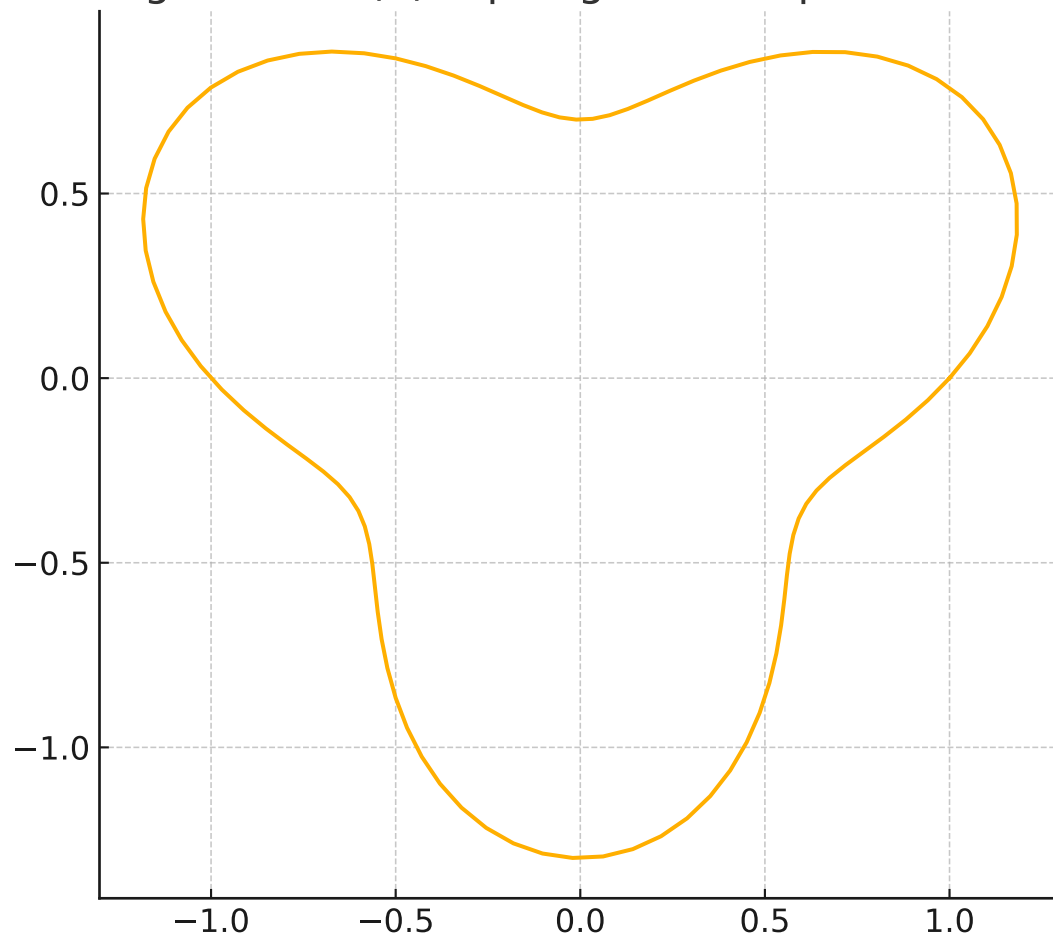


Figure 5: Mass Emergence Boundary

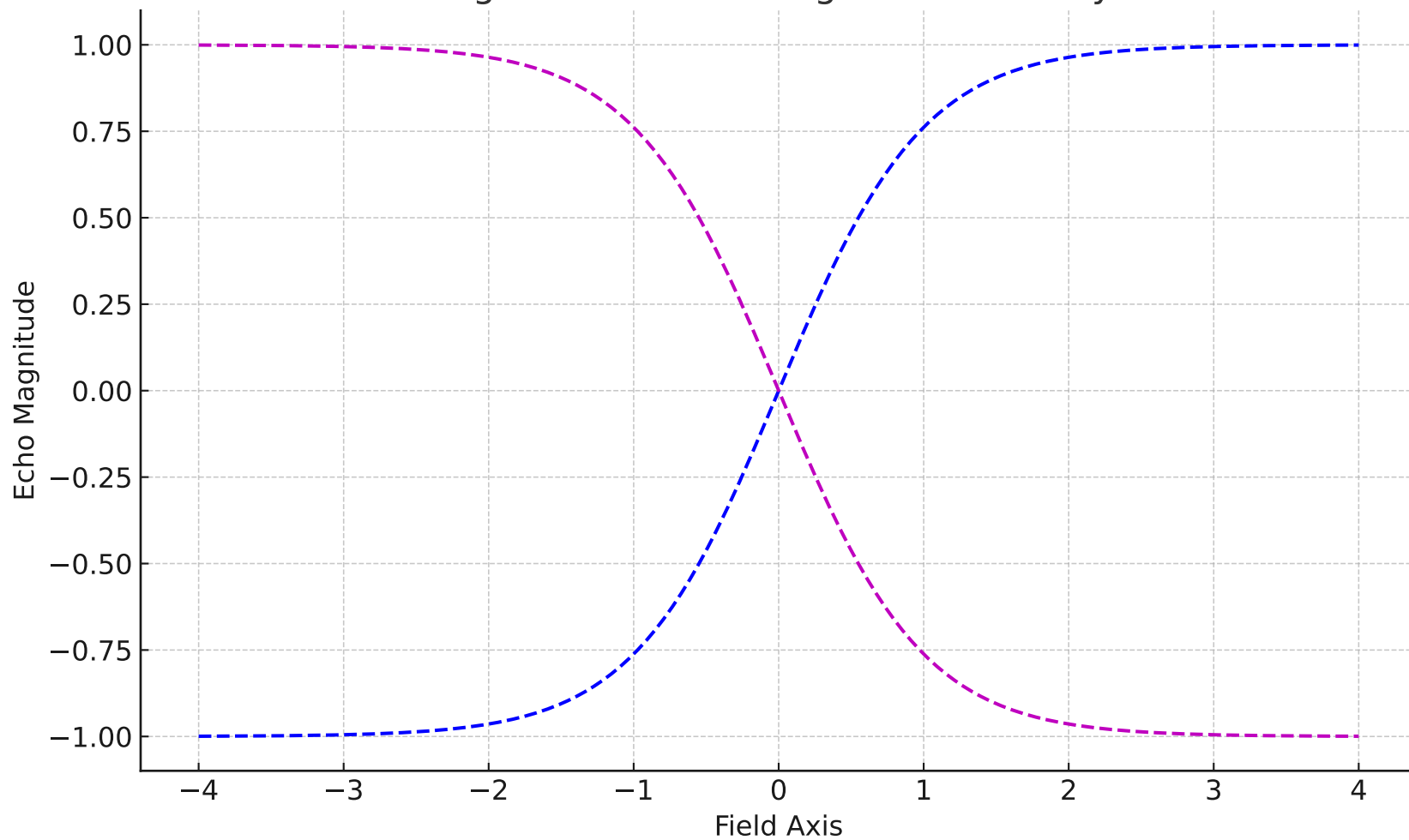


Figure 6: Dual-Symmetry Recursion Loop

