ruSolut
Data Investigation & Recovery Technology

Visual Nand Reconstructor

Chip-off data recovery of broken flash storage devices

1. Flash storage devices.
Structure and functions of flash memory and controller. Typical issues. Controller configuration and its influence on user's data. Chip-off solution for data retreval. Standard and uncommon memory chip packages. TSOP and BGA packages.

Practice: Discovering the different flash storage devices and NAND memory packages.

2. NAND flash chips.
Raw NAND and managed NAND. Memory chip pinouts and functions. Flash memory architecture and internal structure. Physical addressing. Crystals, Planes, Blocks, Pages and its sizes. Single and Multi-plane operations. Memory chip configuration. Chip ID, chip power, data bus. Async and DDR protocols. TLC-WL protocols. Memory chip reading modes. Reading physical image to file. Real-time chip access. Data transfer protocols. NAND chip defects.

Practice: Direct access to NAND and physical image extraction.

3. Physical image of flash memory chip.
Addressing and structure of physial image. Banks, Blocks, Pages, Data area, Spare area. Page structure. Bad Columns. Data and Spare areas. Spare area structure.

Practice: Bit error analysis and NAND power adjustment.

4. Flash controllers.
Controller types. Main functions. Read, Write, Erase operations. Virtual data transfer channel and data optimization. Data protection with ECC. Data transformations: Inversion, Scrambling (XOR). Virtual Block & Page allocation schemes. Flash Translation Layer (FTL). Block management.

Practice: Comparison of Inverted/Scrambled data with normal data. Page allocation.

5. Visual Nand Reconstructor.
Software concept. Case concept. Database. Workspace. Virtual operations. Elemens, parameters. Toolbar & Modes. Operatons with NAND chip. Automatic analysis modes. Dump Viewer and data vizualization modes. Hex viewer. Bitmap viewer. Structure viewer. Record viewer. Binary measurements in Bitmap and Structure viewer.

Practice: Physical image description. Bitmap viewer and Structure viewer.

6. Pattern analysis.
Bitmap usage for pattern analysis. Data patterns. Spare area paterns. Logical Block Number pattern. Logical Page Number pattern. Block Header pattern. ECC paterns. Scrambler (XOR paterns).
Virtual block size detection. Page structure analysis. Data area detection. Spare area detection.

Practice: Virtual block size, Page structure, Spare area structure analysis on different tasks with pattern recognition.

7. Physical image analysis and Data Recovery practice.
Three phases of image analysis (Physical image --> Virtual image --> Logical image).
First phase (Physical image)
- Bit error analysis in real-time chip access using Bitmap viewer
- Setting proper power levels for bit error minimization
- Physical image extraction
- Bad columns removal
- ECC detection
Second phase (Virtual image)
- Physical image structure analysis and description using Bitmap viewer and Structure viewer (Virtual bock size, Page structure). Automatic Data area analysis.
- Data transformations: Inversion and Scrambling (XOR) analysis using Bitmap viewer. Automatic Data transformation analysis.
- Virtual block and page allocation analysis: multi-plane allocation, multi-chip serial and parallel allocation. Automatic Page allocation analysis.
Third phase (Logical image)
- Spare area analysis using Dump viewer modes. Automatic Spare area analysis. SA markers extraction and analysis: LBN, LPN, Header, ECC, Bank number, Write counter.
- Setting up parameters of element "markers table" and translation table creation
- Translation table analysis: Block sorting and filtering. LBN chain integrity analysis: missing blocks and duplicated blocks.
- Block arrange mode and list creation: Main blocks, Replacement blocks, LOG blocks.
- Reconstruction of logical image

Practise: Dumps from different devices for logical image reconstruction and data recovery.