Basic CPLD Development Board

SPECIFICATIONS

• The VL-CPLD trainer is useful to realize and verify various digital designs

• User can construct VHDL / Verilog code and verify the results by implementing physically into the target device

Device

• Xilinx CPLD COOL RUNNER II XC2C64A in VQG100 Package

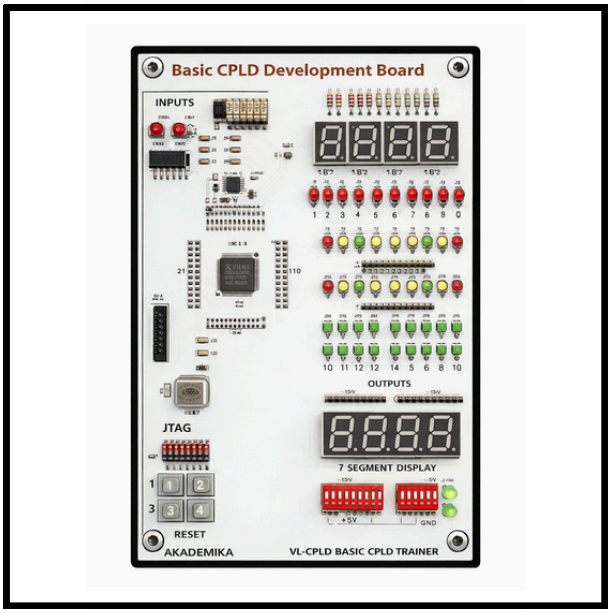
User interface

• 16 input switches with LED indication

• 16 output LEDS

• 2 X 2 matrix keyboard

• Four multiplexed 7- segment displays



CPLD configuration through

• USB port JTAG cable

Clock oscillator

• 4MHz

Power Supply

• +5V, GND

EXPERIMENTS

• I/O test

• Segment interface with keys

• Counter

• Half adder