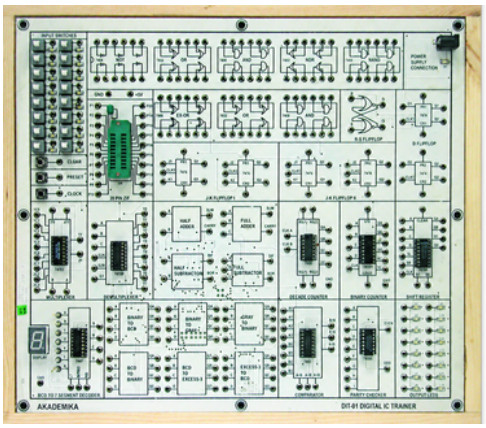
BEL-DIT

Digital IC Trainer Kit



FEATURES

- Single board system, capable of covering Basic Logic Gates , Universal Gates , Flip-flops Counters, Multiplexers and De-Multiplexer, Parity Generator/Checker and Code Converters
- Designed using CPLD Chip
- IEEE symbol of all components provided on the PCB.
- All Components are visible clearly on the top of the PCB.
- Mobile based Interactive e-Manual

SPECIFICATIONS

- On-board Power supply (7.5V,300mA) should be provided.
- Basic logic gate IC's:
  NOT (7404)
  OR (7432)
  AND (7408)
  NOR (7402)
  NAND (7400)
  EX-OR (7486)
- NAND and NOR gates as Universal Logic Gates.
- De-morgan’s theorem I & II
- Boolean Equation
- TTL to CMOS and CMOS to TTL Interface
- Half Adder, Full Adder, Half Subtractor, Full Subtractor
- Basic Flip-Flops:
  RS (using NOR)
  JK (7476)
  D (7474)
  MS-JK (7476)
  T (using JK)
- Counters
- Synchronous Binary Counter (74191).
- 4 Bit Ring Counter using (7476).
- Decade / BCD counter using 7490.
- Universal Shift register 74194.
- 9-bit parity Generator / Checker (74280).
- Multiplexer (74153) and Demultiplexer (74138).
- BCD to seven segment decoders (7447) & Seven segment display.
- 4-bit Comparator (7485).
- Binary to Gray, Gray to Binary, Binary to BCD, BCD to Binary, BCD to Excess 3, Excess 3 to BCD
- 16 switches to provide Logic 0 & 1 inputs.
- 16 LEDs to observe the output logic states.
- Manual clock, present and clear to observe the counter operation.
- 20 pin ZIF socket

EXPERIMENTS

- To verify the truth table and function of basic logic gates
- To verify NAND and NOR gates as universal logic gates
- To verify the De-Morgan's theorem I and II
- To verify the Boolean equation
- To study and verify working and truth table of half adder, full adder, half subtractor and full subtractor
- Design of half adder and half subtractor using multiplexer and de-multiplexer
- Study the behavior of basic flip-flops (RS, JK, MSJK, D , T)
- To study and design ripple/ asynchronous counter using JK flip-flop
- To study the synchronous binary counter
- To design 4-bits ring counter using JK flip-flop
- To verify decade / BCD counter
- To study universal shift register
- To study 8-bits parity generator / checker
- To study multiplexer and de-multiplexer
- To study BCD to seven segment decoder
- To study 4- bits comparator
- To study Binary to Gray, Gray to Binary, Binary to BCD, BCD to Binary, BCD to Excess-3, and Excess-3 to BCD converters
- To study 4-bits binary adder
- Study of TTL clock generation using NAND gate
- Study of de-bounce circuit using NAND gate