

SDR -MIMO

2x2 MIMO Software Defined Radio



FEATURES

- FPGA-based processing supports real-time implementation of communication algorithms.
- The reconfigurable platform allows students to modify signal-processing parameters and study concepts like OFDM, MIMO and different detection techniques.
- External clock synchronization supports coordinated operation with other SDRs in multi-device experiments.

SPECIFICATIONS

Core Hardware

- RF Transceiver: AD9363
- RF Channels: 2 Tx, 2 Rx with 70MHz-6GHz Freq range
- Reference Clock: 40 MHz VCTCXO, 0.5 ppm
- SoC: Xilinx Zynq-7010 (XC7Z010)
- FPGA Resources: ~28K Logic Cells
- RAM: 512 MB DDR3 & Flash Memory: 32 MB
- USB Interface: USB 2.0 with OTG
- Ethernet: Gigabit Ethernet
- Boot Options: Flash / MicroSD
- Power Supply: 5V $\pm$ 0.5V, 2A (microUSB)
- I/O Logic Level: 1.8V

AD9363 Signal Chain Specifications

- ADC/DAC Resolution: 12-bit, dual Σ - Δ per channel
- Max Sample Rate: 61.44 MSPS(theoretical); ~4–6 MSPS sustained
- Channel Bandwidth: 200 kHz – 20 MHz
- Tx Outputs: differential (TX1A/B, TX2A/B)
- Tx Attenuation Range: 90 dB (0.25 dB resolution)
- Tx EVM: $\sim$ 34 dB, Tx Noise Floor: $\sim$ 156 dBm/Hz
- Tx Monitor: 66 dB dynamic range, 1 dB accuracy
- Rx Inputs: differential / single-ended
- Rx Noise Figure: 2.5 dB @ 800 MHz, 3.0 dB @ 2.4 GHz
- Rx Gain Range: Up to 74.5 dB (1 dB steps)
- RSSI Dynamic Range: 100 dB
- LO Step Size: 2.4 Hz
- BB PLL Range: 700-1400MHz(from 10-80MHzreference)

- FIR Filtering: 128-tap (Tx interpolation / Rx decimation)
- Digital I/Q Ports: Two 12-bit parallel ports (P0, P1)
- Signaling Levels: CMOS 1.2–2.5V or LVDS 1.8–2.5V
- Aux ADC: 12-bit / Aux DAC: Two 10-bit
- Package: 144-ball CSP_BGA, 10 mm $\times$ 10 mm

Zynq-7010 FPGA/SoC Resources

- Processor: Dual-core ARM Cortex-A9, up to 667 MHz
- L1 Cache: 32 KB instruction + 32 KB data per core
- L2 Cache: 512 KB
- On-Chip Memory: 256 KB
- DMA Channels: 8 (4 dedicated to PL)
- Logic Slices: 4,400
- 6-input LUTs: 17,600
- Flip-Flops: 35,200
- Block RAM: 2.1 Mb
- DSP Slices: 80 (DSP48E1), XADC: Dual-channel, 12-bit

Required Software Stack

- libiio - the core driver/communication library Pluto uses
- libad9361-iio - helper library for the AD9361/AD9363
- GNU Radio (3.10.x with Python 3)

Computer Requirements

- Processor: Multi-core CPU with RAM 8GB Minimum
- USB 3.0 host ports and dedicated 5V/2A for Pluto+ Linux/Ubuntu for stable GNU Radio and SDR operation

EXPERIMENTS

- To study and verify the Alamouti STBC scheme for a 2 $\times$ 2 MIMO system.
- To study 2 $\times$ 2 MIMO spatial multiplexing with 16-QAM using Zero-Forcing (ZF) detection.
- To study V-BLAST SIC for successive detection of two 16-QAM streams.
- To study 2 $\times$ 2 MIMO using Maximum Likelihood (ML) detection for QPSK signals.
- To study SVD across MIMO
- To estimate channel matrix and calculate channel capacity
- To Study and Implement MIMO OFDM.
- To Study Waterfilling Power Allocation and NOMA.
- And many more based on the capacity of the hardware