

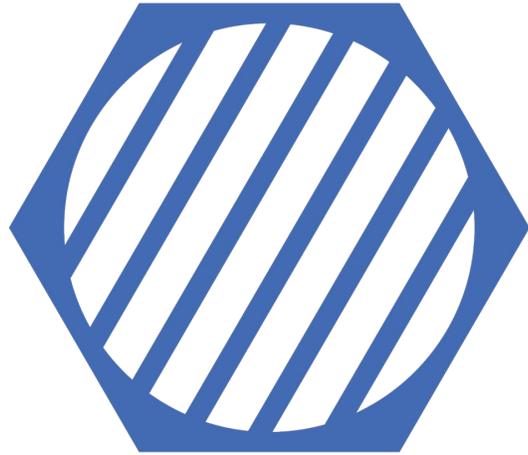
# SIXLINE

SEMICONDUCTOR

**The Carbon Upgrade for a  
Silicon World**



# Enables Next-Generation Carbon Electronics for AI and ALL High-Performance Electronics



**SIXLINE**  
SEMICONDUCTOR

- **SixLine produces semiconducting carbon never before possible commercially**
- **Strong industry engagement and LOIs**
- **Phased tech development**
  1. **Next gen wireless**  
Total Market: \$42B (Wireless Components) 
  2. **Faster AI/computing with lower energy usage**  
Total Market: \$14.4B (AI Materials) 

# WHY NOW?

## THE SILICON PERFORMANCE WALL



### Wireless Performance Limits

Advanced 5G, 6G demand is hitting the physical limits of GaAs and Si. We need higher frequency and better linearity.



### AI Energy/Processing Crisis

By 2040, ICT will consume 25% of global energy. Silicon efficiency has plateaued while AI demand explodes.

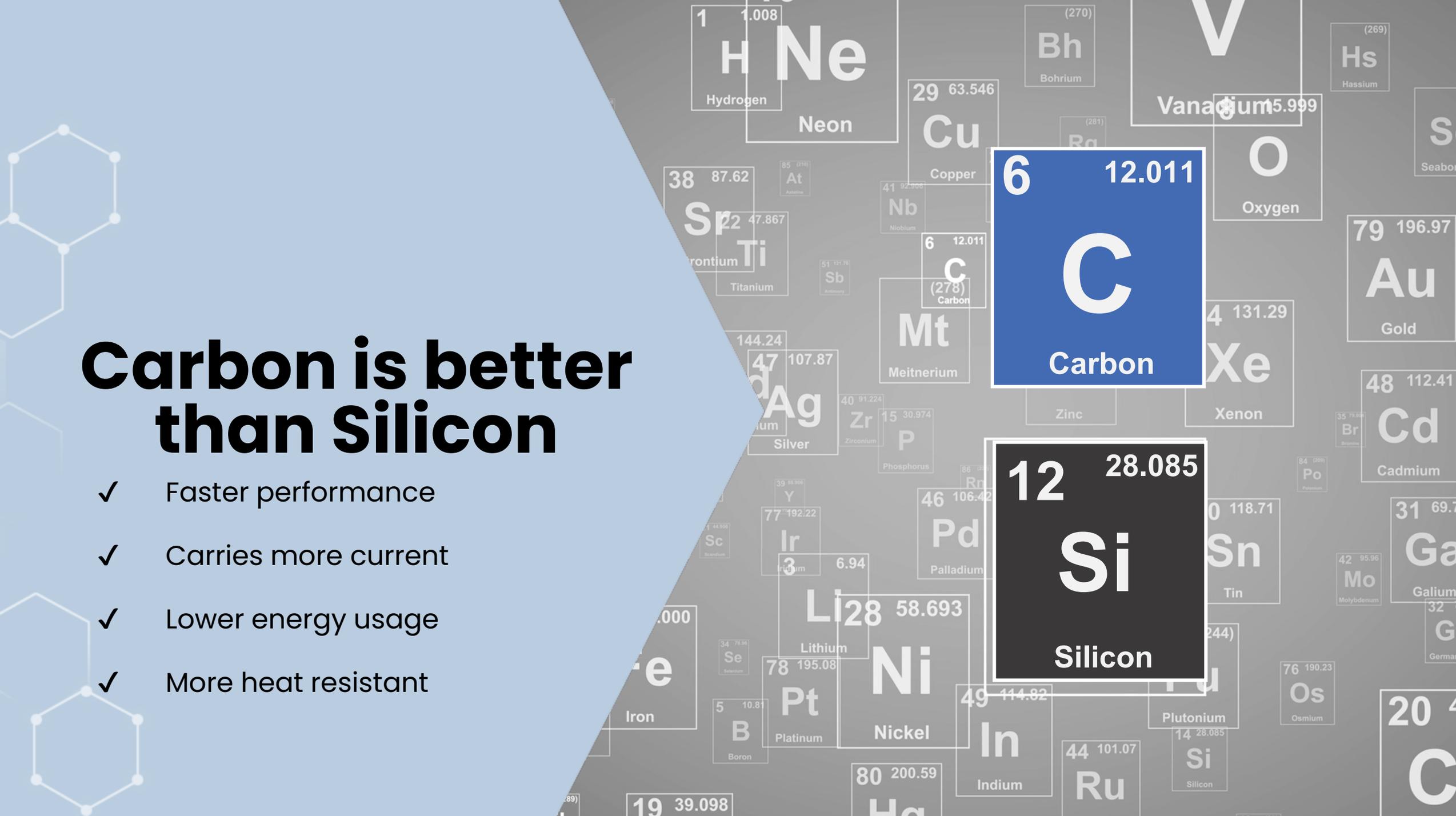


### The Bottleneck

Performance is stalled by power, heat, and lithography resolution. Current materials like Si and GaAs are limiting.

ADD AI NEEDS MORE CLEARLY

**The next paradigm shift requires a new material foundation**



# Carbon is better than Silicon

- ✓ Faster performance
- ✓ Carries more current
- ✓ Lower energy usage
- ✓ More heat resistant



# **The Breakthrough**

**SixLine Enables  
Semiconducting Carbon  
Never Before Possible**

# SixLine: Route to New Age Electronics for AI and ALL High-Performance Electronics

**5× FASTER  
PROCESSING  
SPEED**

**1000× LOWER  
ENERGY**

**10× HIGHER  
FREQUENCIES**

**Space/Defense**

**IoT**

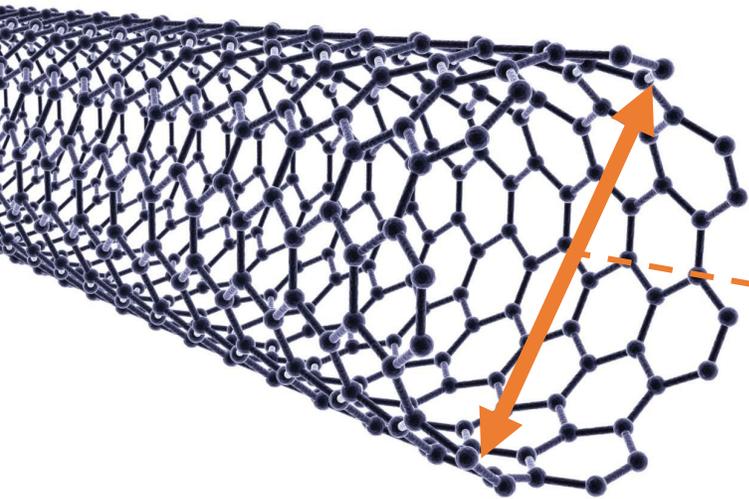
**Artificial  
Intelligence**

**Data Centers**

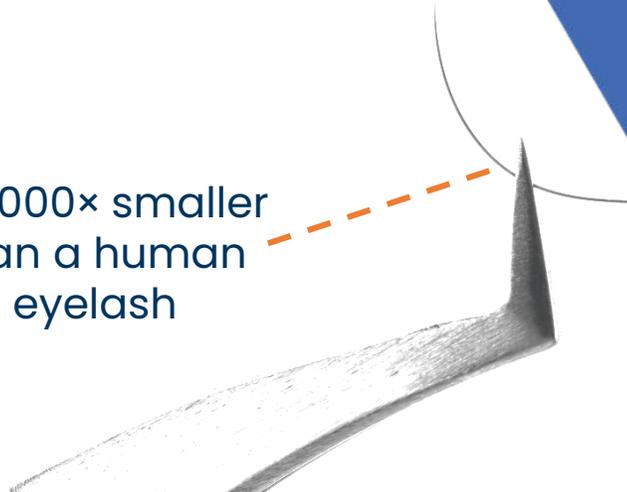
**Sensing**

# SixLine's Technology

Leveraging Carbon Nanotubes  
(CNTs) in Commercially  
Compatible Processes

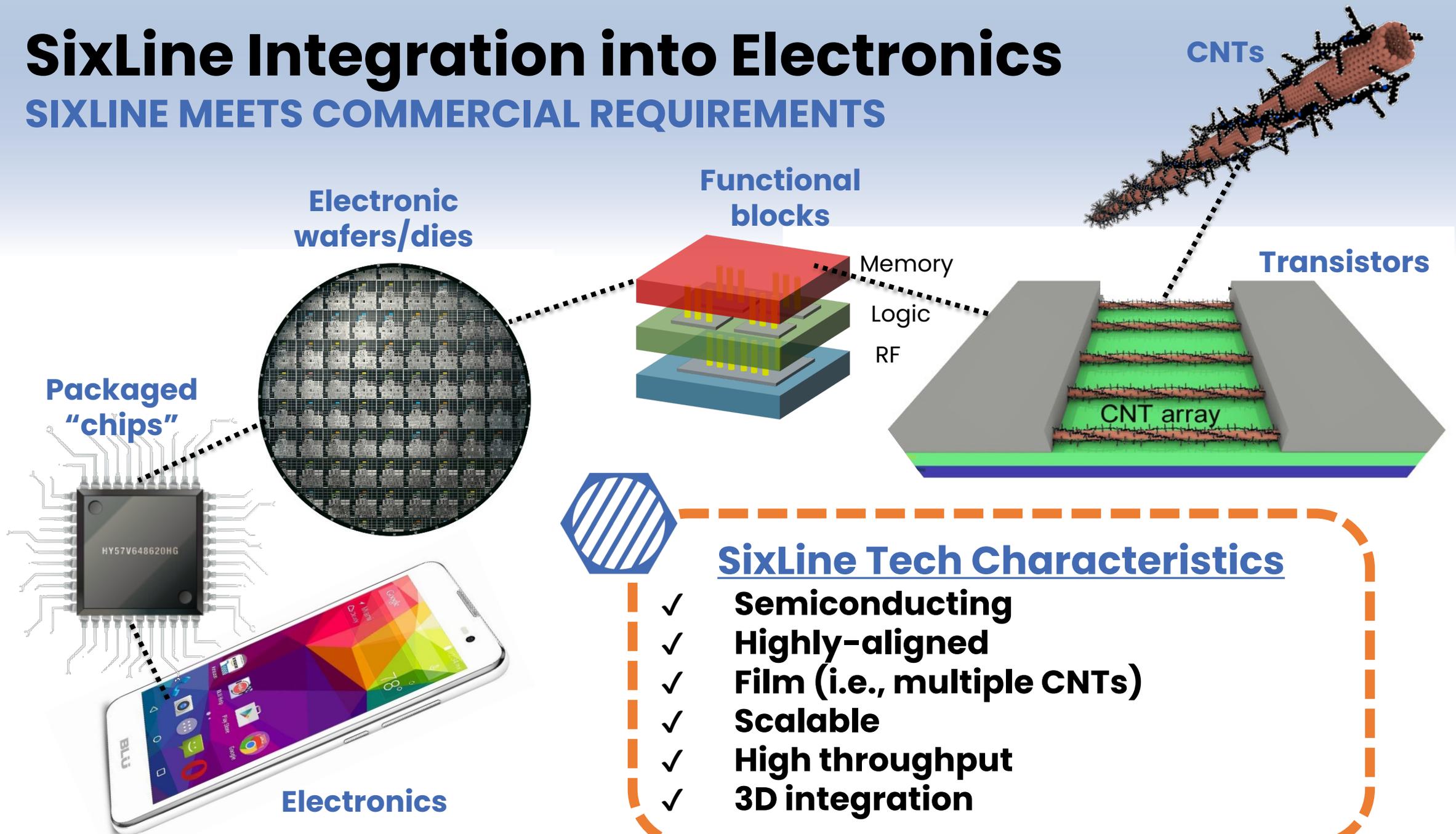


100,000× smaller  
than a human  
eyelash



# SixLine Integration into Electronics

## SIXLINE MEETS COMMERCIAL REQUIREMENTS

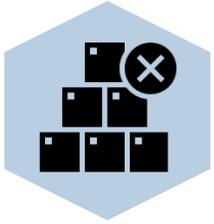


### SixLine Tech Characteristics

- ✓ Semiconducting
- ✓ Highly-aligned
- ✓ Film (i.e., multiple CNTs)
- ✓ Scalable
- ✓ High throughput
- ✓ 3D integration

# Previous Nanotube Tech Has Failed

## 30-YEAR CHALLENGE



**Poor control over organization**



**Low electronic quality**



**Lab benchtop scale**



**Slow processes**



**30-year  
challenge to  
create ideal CNT  
films**



# SixLine's Processes to Produce Semiconducting Carbon

## STRONG IP LIBRARY



IP protecting certain wrappers/removing wrappers

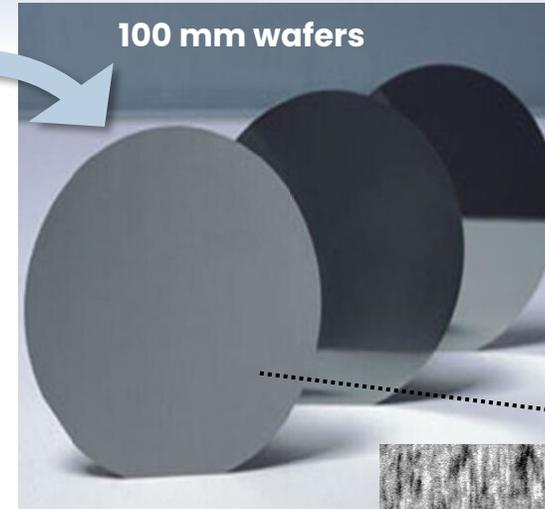
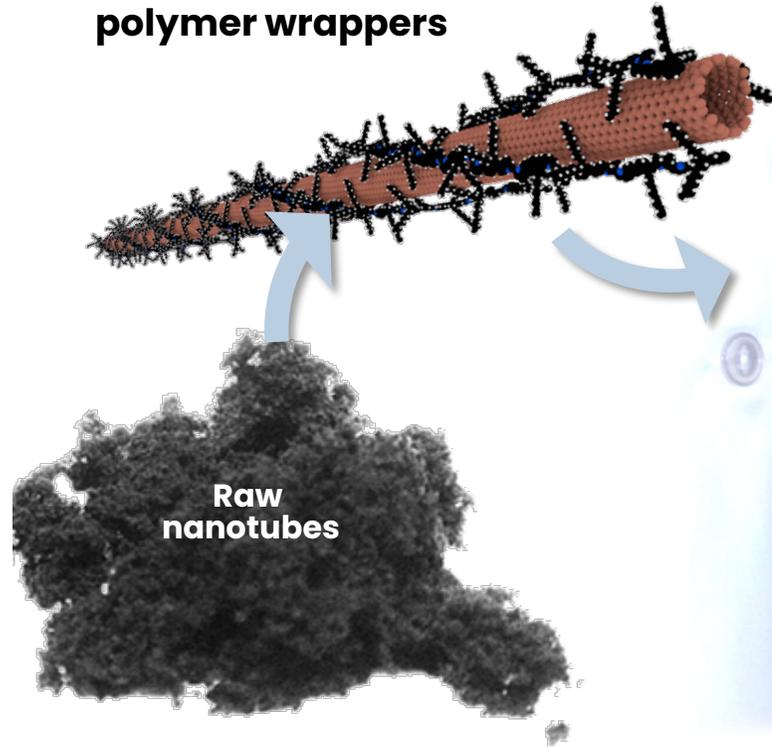
1) Isolate semiconducting nanotubes via removable polymer wrappers

2) Electronics-grade, high-purity semiconducting nanotube ink

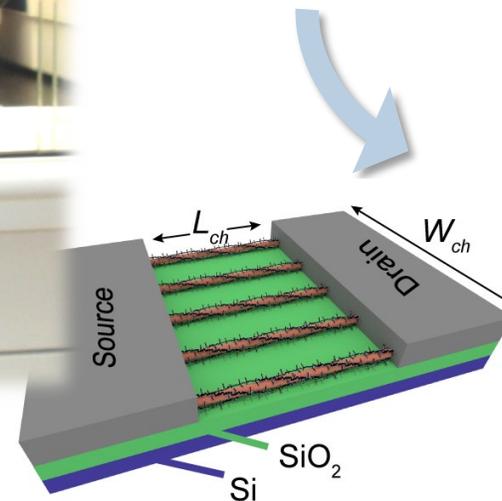
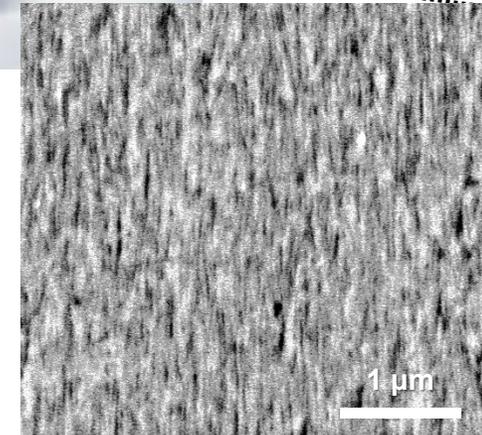
3) Scalable CNT alignment



SixLine has IP protecting alignment processes



High-performance devices



SixLine has IP claims protecting composition of matter of the nanotube films and nanotubes films integrated into transistors

7 patents with process and composition of matter protection

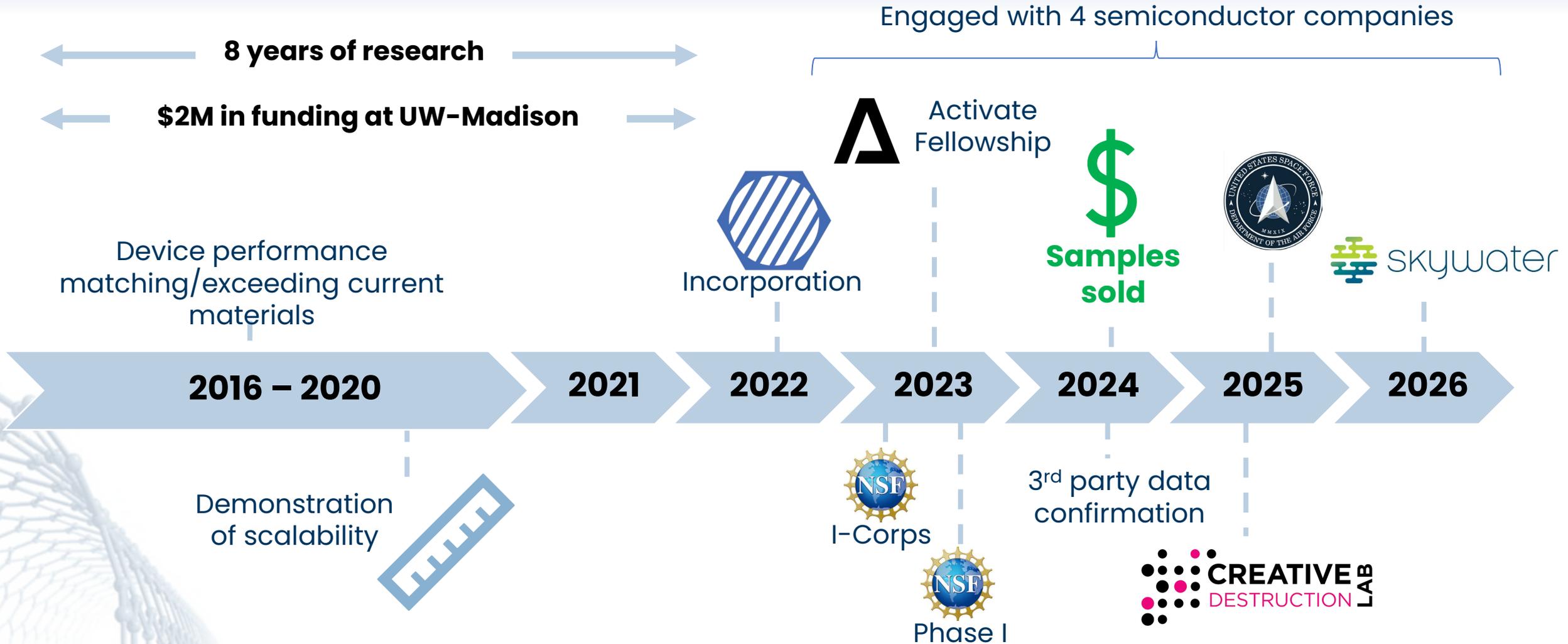
# SixLine SURPASSES Competitors

## SUPERIOR CNT FILM CHARACTERISTICS

		Other CNT Companies			
CNT Film Feature	 SixLine	 Carbon Tech Inc.	Aligned Carbon	NANTERO	 Peking Spinout
Density ( $\mu\text{m}^{-1}$ )	250	5 – 10	5 – 10	70	200
Alignment	$\pm 4^\circ$	$\pm 1^\circ$	$\pm 1^\circ$	$\pm 90^\circ$ (random)	$\pm 8^\circ$
Semiconducting Purity	>99.99% (likely >99.9999%)	>98%	>98%	>99.9999%	>99.9999%
Time to Coat 200 mm Wafer	~2 s/120 s	7 hr	7 hr	7 – 9 hr	6 hr
Temperature	Room	High	High	Room	Room

# Strong Technology and Company Traction

## BREAKTHROUGH SCIENCE DRIVEN TO COMMERCIALIZATION



# Strategic Roadmap to Market

## WIRELESS COMMUNICATION → AI/COMPUTING

### PHASE 1 (2026+)

#### Wireless Components

Targeting the \$42B RF components market. **Revenue through sales of high-performance RF switches and LNAs.**



### PHASE 2 (2029+)

#### AI & Computing

Solving the AI energy and speed barrier. Licensing process to tool manufacturers and **selling nanotube inks to chip fabrication facilities.**

# PHASE 1: WIRELESS

**Our films are near-spec for high-performance RF today.** We are currently scaling for fab integration.

- ✓ Partnering with commercial fabs (2026).
- ✓ Experimental RF devices match realistic simulations, providing roadmap to exceed incumbent Si and GaAs performance.
- ✓ Collaborate with tool manufacturers and work with contract manufacturers and fabrication facilities.



# PHASE 2: AI/Computing



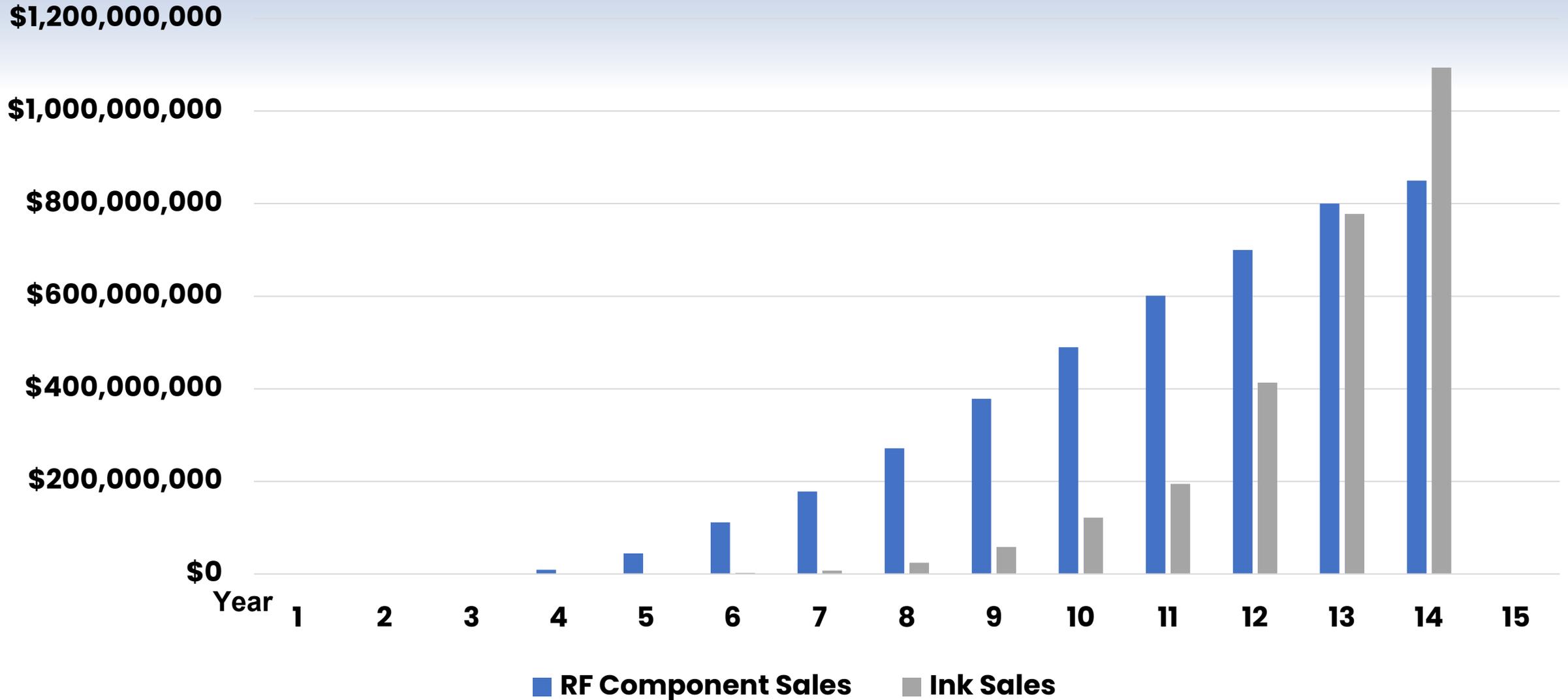
**The “razor-and-blades” business model for semiconducting carbon.**

As technology matures, SixLine moves to the ultimate prize: **The foundation of all future high-performance computing.**

We license our processes to tool manufacturers and sell proprietary high-purity inks directly into logic/computing fabs. **This is a recurring, high-margin revenue model at global scale.**

# Large Projected Revenues

WIRELESSS COMPONENTS → AI/COMPUTING MATERIALS



# Strong Management Team

## SIGNIFICANT MATERIALS, INDUSTRY, AND STARTUP EXPERIENCE



- Technology co-inventor
- 14 years technical research experience
- Extensive entrepreneurship training



**Katy Jenkins, PhD**  
*CEO, Co-founder*



- Expert in nanotube electronic devices
- Technology co-inventor
- Professor at UW-Madison



**Prof. Mike Arnold, PhD**  
*Chief Technical Advisor, Co-founder*



- >20 years startup experience
- Negotiated exit for Virent while serving as COO/CFO
- Commercialized nanotech products for superconductors and hypersonic applications



**Jeff Moore**  
*Strategy/Commercial Support*



- Expert in nanotube assembly and chemistry
- Technology co-inventor
- Professor at UW-Madison



**Prof. Padma Gopalan, PhD**  
*Technical Advisor*

Ongoing search for technical/industry advisors

# JOIN THE CARBON REVOLUTION

# \$1.1M

Pre-Seed Fundraise (\$725k remaining)

## Technical Milestones

Scale alignment to 200mm wafers; integrate into commercial fab; create initial prototype CNT RF switches.

## Pre-seed Unlocks

Multiple customers purchasing CNT wafers; strategic industry funding.

## The Future

Sets the stage for packaged RF components and entering AI/computing markets.

## OUR PARTNERS

Activate



Confidential  
Industry Partners



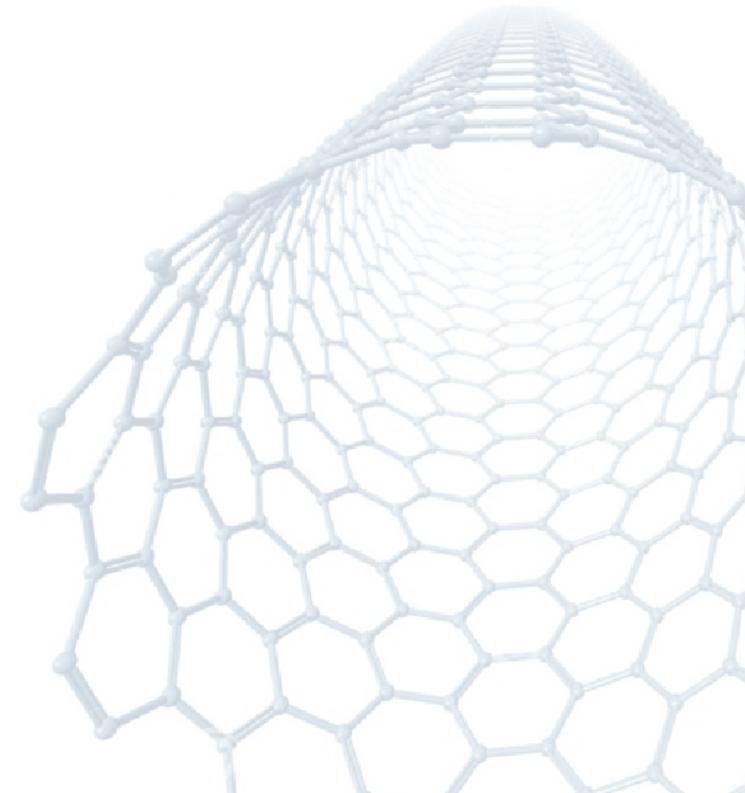
rpv

## OUR FUNDING



Activate

# Appendix



# SixLine's Technology Advantages

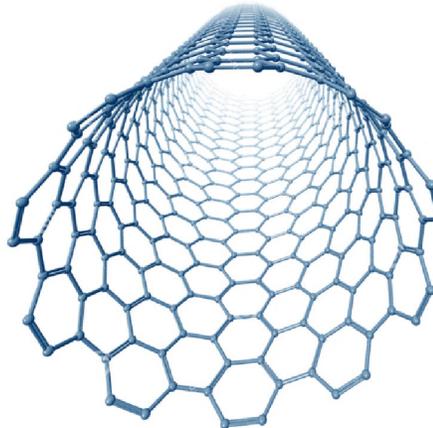
**SixLine enables necessary performance and integration for semiconductor electronics**

**SixLine's 1<sup>st</sup> Target:  
Radiofrequency (RF)**

CNT-Based RF Devices	CNT Device Property
<b>Faster, smaller, more energy efficient electronics, streaming more data with lower lag</b>	10× higher frequencies
	Larger data bandwidths
	Intrinsic linearity
	Direct integration with silicon logic



**SIXLINE**  
SEMICONDUCTOR



**SixLine's Longer-Term Market:  
Logic/Computing**

CNT-Based Logic Devices	CNT Device Property
<b>Faster electronics, with more computational power, and up to 1000× lower energy usage</b>	5-20× lower power usage (2D FETs)
	Enables 3D heterogeneous integration
	5× current density

**Nanotubes on industry roadmaps**

# Tech & Business Milestones

Extensive government grant funding planned in addition to equity funding rounds

**\$1.1M Pre-Seed**

**\$3-5M Seed**

**\$8M Series A**

**\$20M Series B**

**2030 Exit opportunity**

**2025**

**2026**

**2027**

**2028**

**2029**

**2030**

Hiring plan:  
Key hires

◆ 3 FTE  
(CEO, Engineer, Scientist)

◆ 4 FTE  
(Tech Director)

◆ 10-12 FTE  
(CTO, BD, PM, Device Designer, Lead Scientist, Scaling)

◆ 15-20 FTE  
(COO, Scientists/Engineers, Office Manager)

Capabilities/partnerships for equipment, device, manufacturer, raw material supply

⬡ (2)

⬡ (3)

⬡ (6)

▲ Start scoping contract manufacturers

▲ Commit contract manufacturers

**Tech Development for wireless manufacturing**

**RF Component sales**

• Process scalability

● 200 mm wafer

● 300 mm wafer

● Automated process tool

• Wireless/RF device performance

● RF switch FET  
Target:  
 $F_t = 100 \text{ GHz}$

● RF switch FET  
Target:  
 $F_t = 5 \text{ THz}$   
(informed by industry experts)

● **Component validation**  
Packaged RF switch  
 $F_t = 5 \text{ THz}$

**Development for computing**

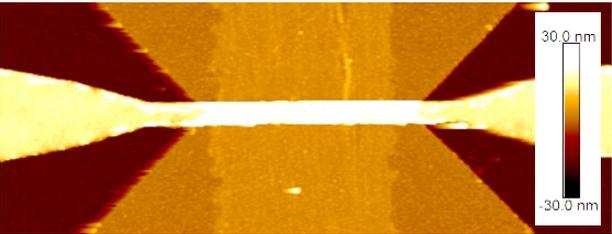
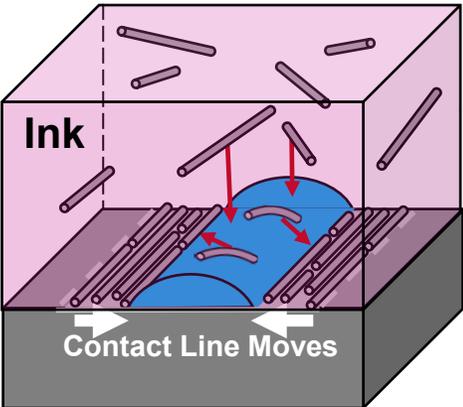
# Technical Approach & Current Progress

- **Multiple solution-based, room temperature alignment techniques**
- **Exceptional p-type device performance**
  - n-type can be achieved with gate stack control
- **High alignment and packing densities enable superior current densities, transconductance, at low applied bias**
- **Devices that challenge or exceed incumbent materials**

# Alignment Processes

## ShASAM-W

2D nanotube liquid crystals at liquid/liquid interfaces

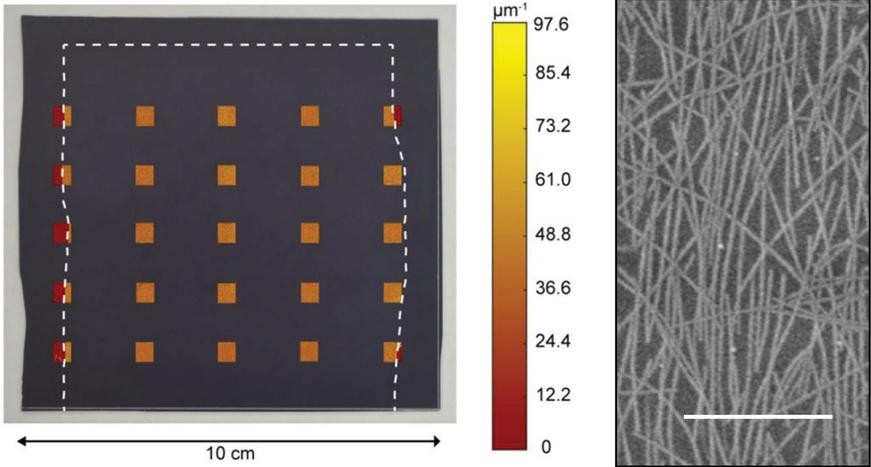
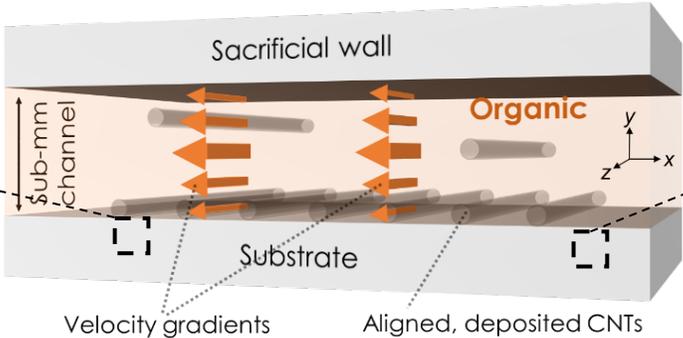


10 μm stripes, aligned with device patterns

**CNTs (aligned within  $\pm 4^\circ$ ) at  $200 - 250 \mu\text{m}^{-1}$**

## ShASAM

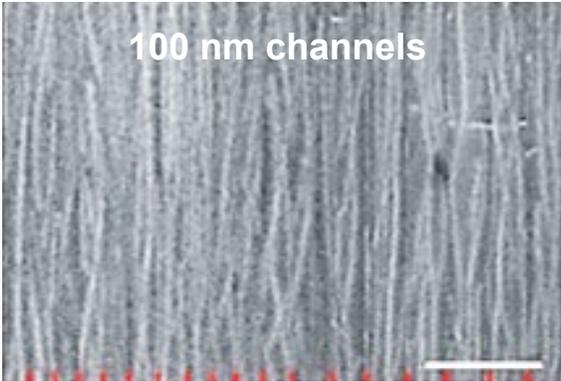
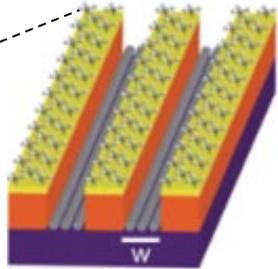
Application of shear on bulk ink, across substrate



**CNTs (aligned within  $\pm 20^\circ$ ) at  $\sim 70 \mu\text{m}^{-1}$**

## ShASAM-C

Application of shear on bulk ink, across substrate patterned with chemical/topographic channels

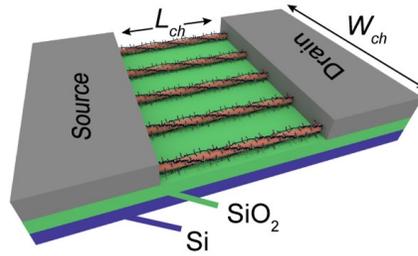
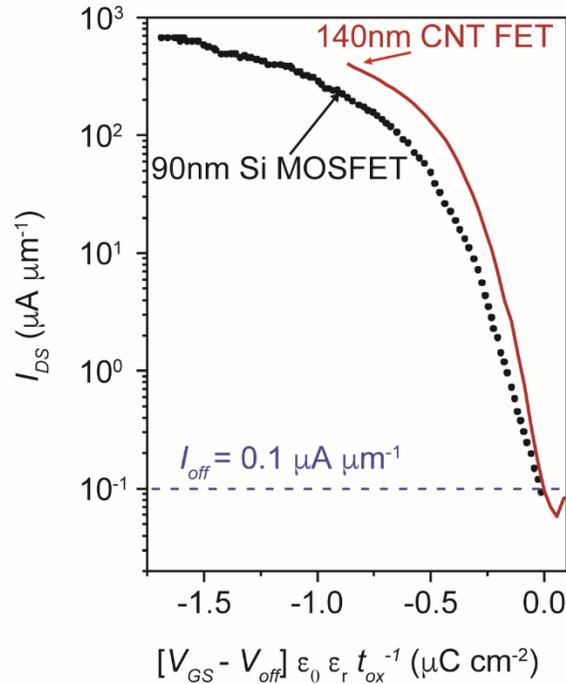


**CNTs (aligned within  $\pm 7^\circ$ ) at  $\sim 100 \mu\text{m}^{-1}$**

# Exceptional Gen 1 DC & RF Performance

Strong device performance from Gen I alignment technique with similar alignment as TaFISA

## DC device performance outperforms Si, GaAs



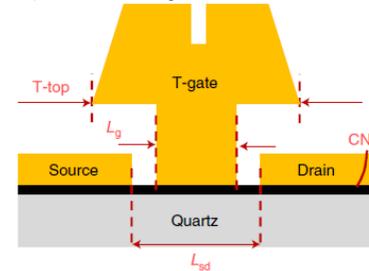
- 15 nm SiO<sub>2</sub>/Si back gate
- Pd top contacts

Data normalized by gating efficiency

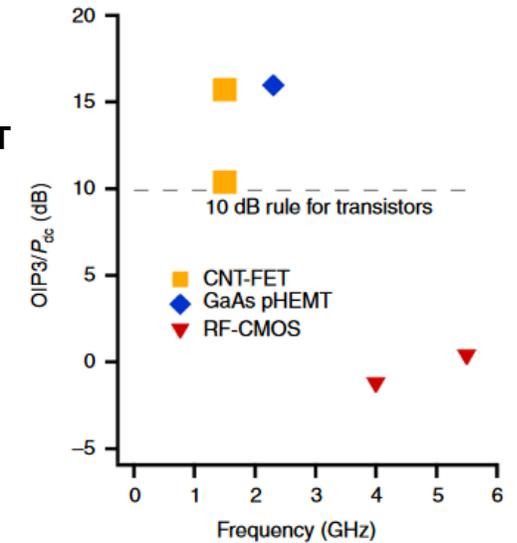
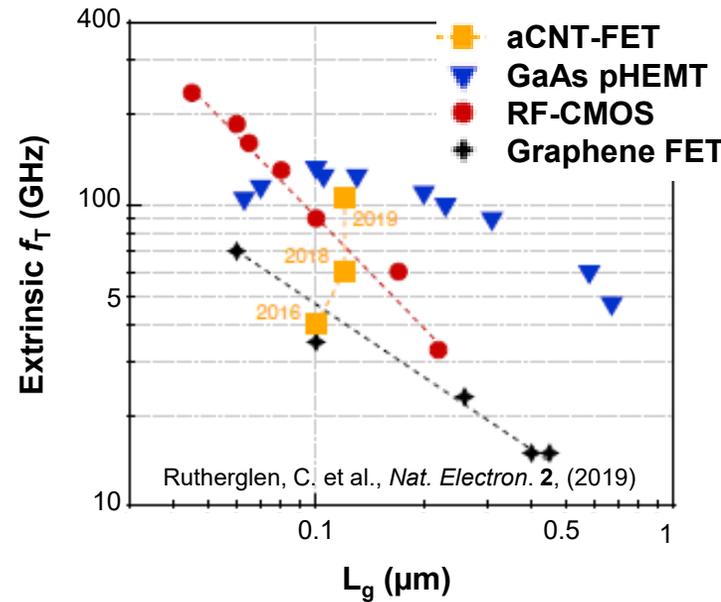
Brady G. J., et al. *Sci. Adv.* 2, e1601240 (2016)

## Nanotube RF performance of 100 GHz

Projected  $f_T > 300 \text{ GHz}$  for 60 CNTs/ $\mu\text{m}$  at 100 nm  $L_g$



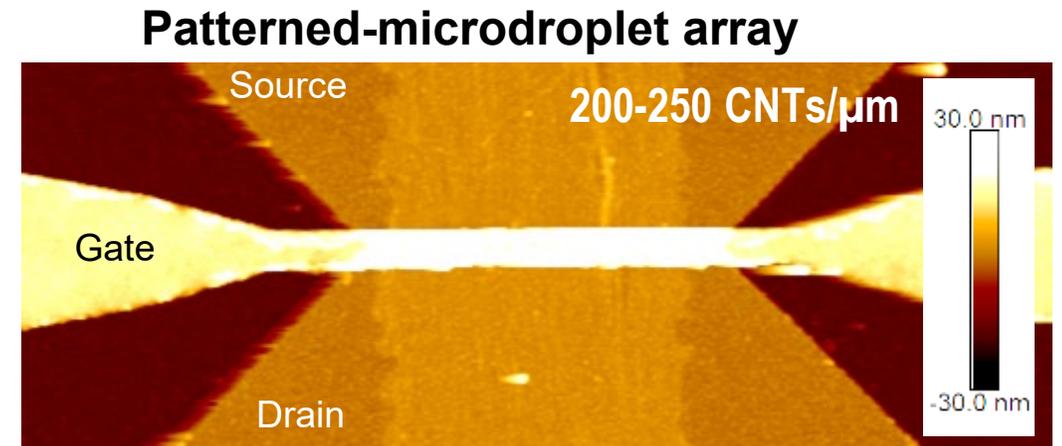
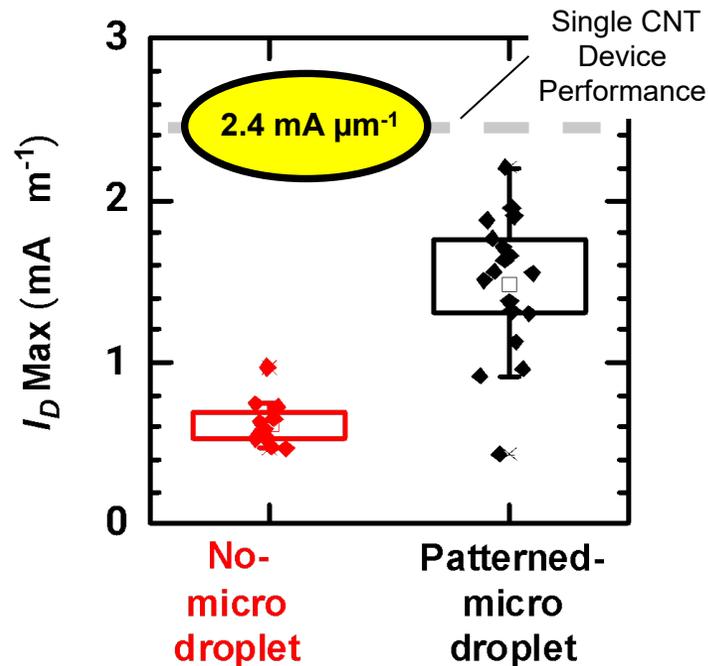
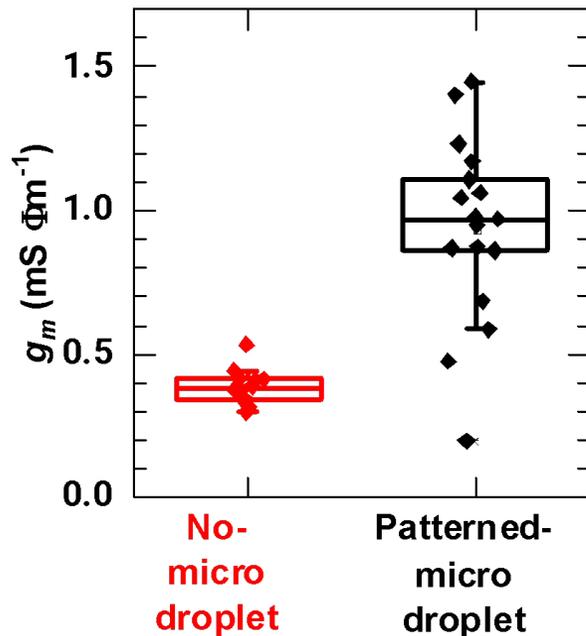
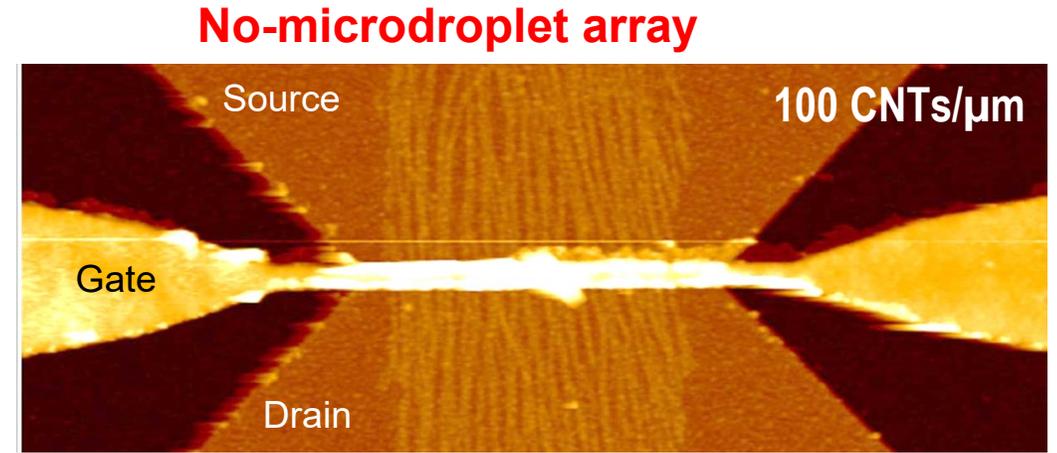
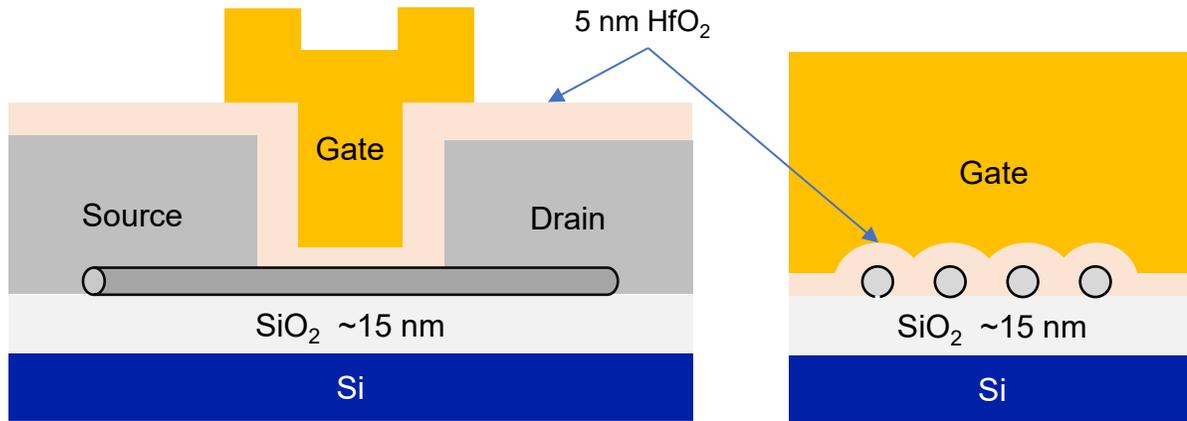
- T-gate
- Al<sub>2</sub>O<sub>3</sub> gate material
- Single-crystal quartz substrate
- Pd top contacts



Realistic projected nanotube performance significantly exceeds conventional materials

# High Density Nanotube Arrays

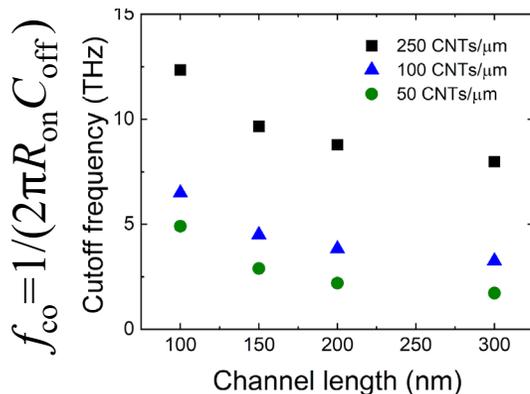
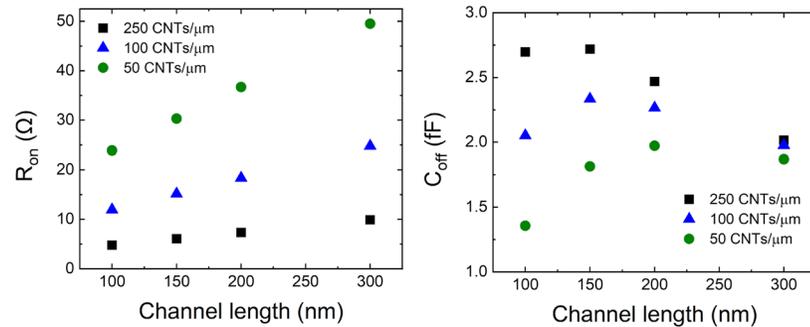
Locally patterned, ideal packing densities of aligned CNTs for high-performance electronics



## RF Switches

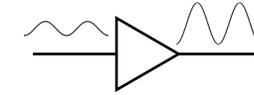
Low on-state resistance and off-state capacitance for THz RF switches

COMSOL simulations for CNT FET RF switches

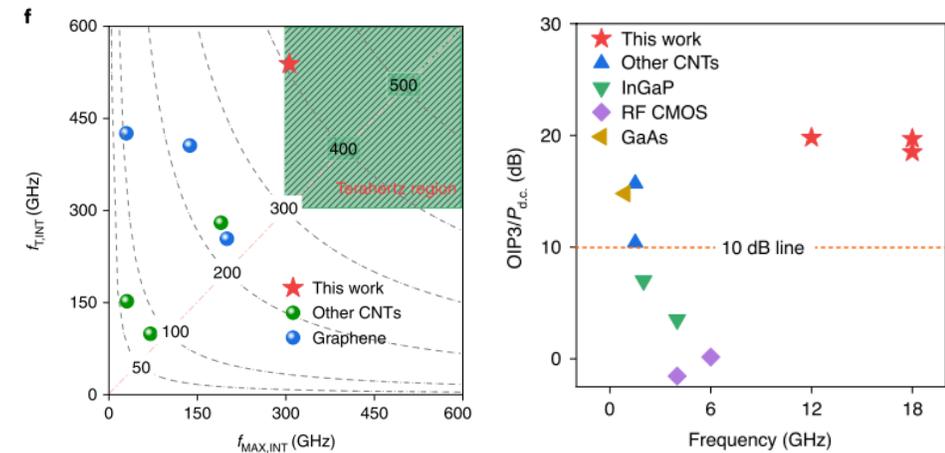


**CNT-based RF switches: 5-10×  
> R<sub>on</sub>C<sub>off</sub> cutoff frequencies  
compared to projected 22nm  
FDSOI (1 THz)**

## RF Amplifiers



Superior **electronic properties** and **low device parasitics** can lead to THz cutoff and maximum oscillation frequencies with high linearity for next generation low-power RF amplifiers



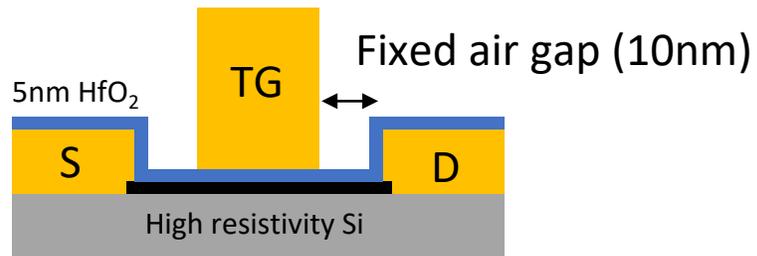
Shi, H., Ding, L., Zhong, D. *et al.* Radiofrequency transistors based on aligned carbon nanotube arrays. *Nat Electron* 4, 405–415 (2021)

**Peking University:**  $f_t = 551$  GHz and  $f_{max} = 1024$  GHz, respectively ( $L_g = 35$  nm)

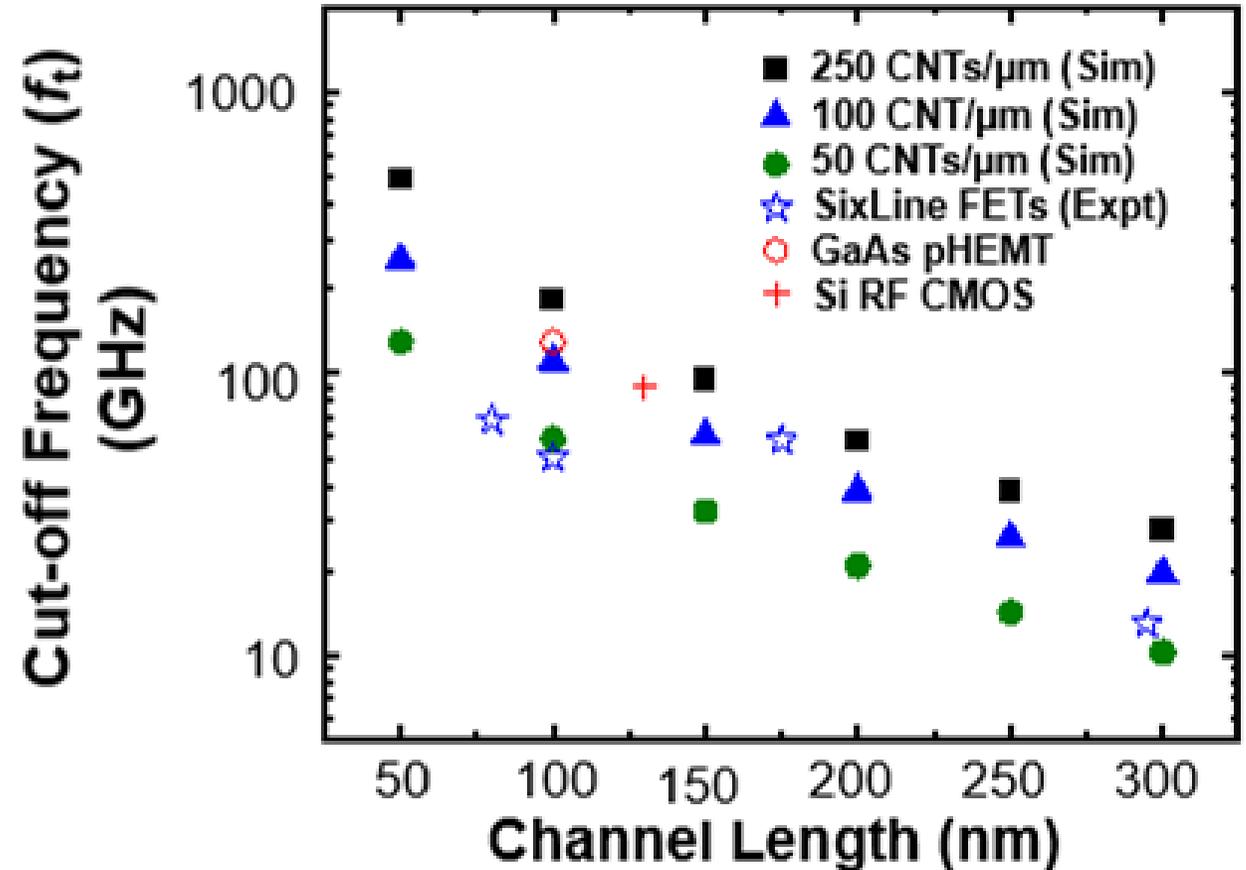
# CNT RF FET Performance

Recent initial experimental results (2025) match simulations—routes to significant performance improvement in progress

## Top gate (I-gate) FETs



Current I-gate and undoped architectures limit frequency performance by increasing resistances—improved architectures in progress



○ Chih-Sheng Chang, Chih-Ping Chao, J. G. J. Chern and J. Y. .  
-C. Sun, "Advanced CMOS technology portfolio for RF IC  
applications," in *IEEE Transactions on Electron Devices*

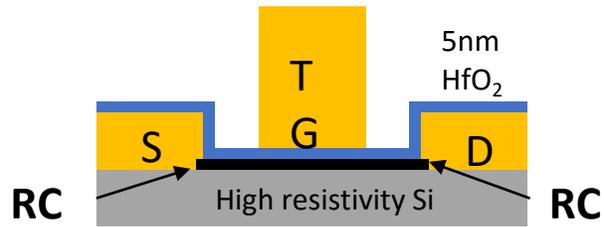
+ A. Bessemoulin, J. Tarazi, M. G. McCulloch and S. J. Mahon,  
"0.1-μm GaAs PHEMT W-band low noise amplifier MMIC  
using coplanar waveguide technology,"

# Next Steps for Improved Performance

## 1) Reduce contact resistance (2RC)

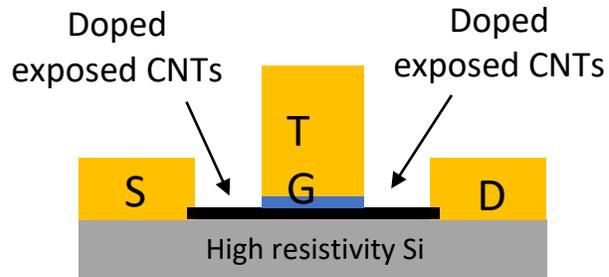
30k $\Omega$  /CNT  $\longrightarrow$  15k $\Omega$  /CNT

3x improvement



## 2) Dope ungated regions of CNTs

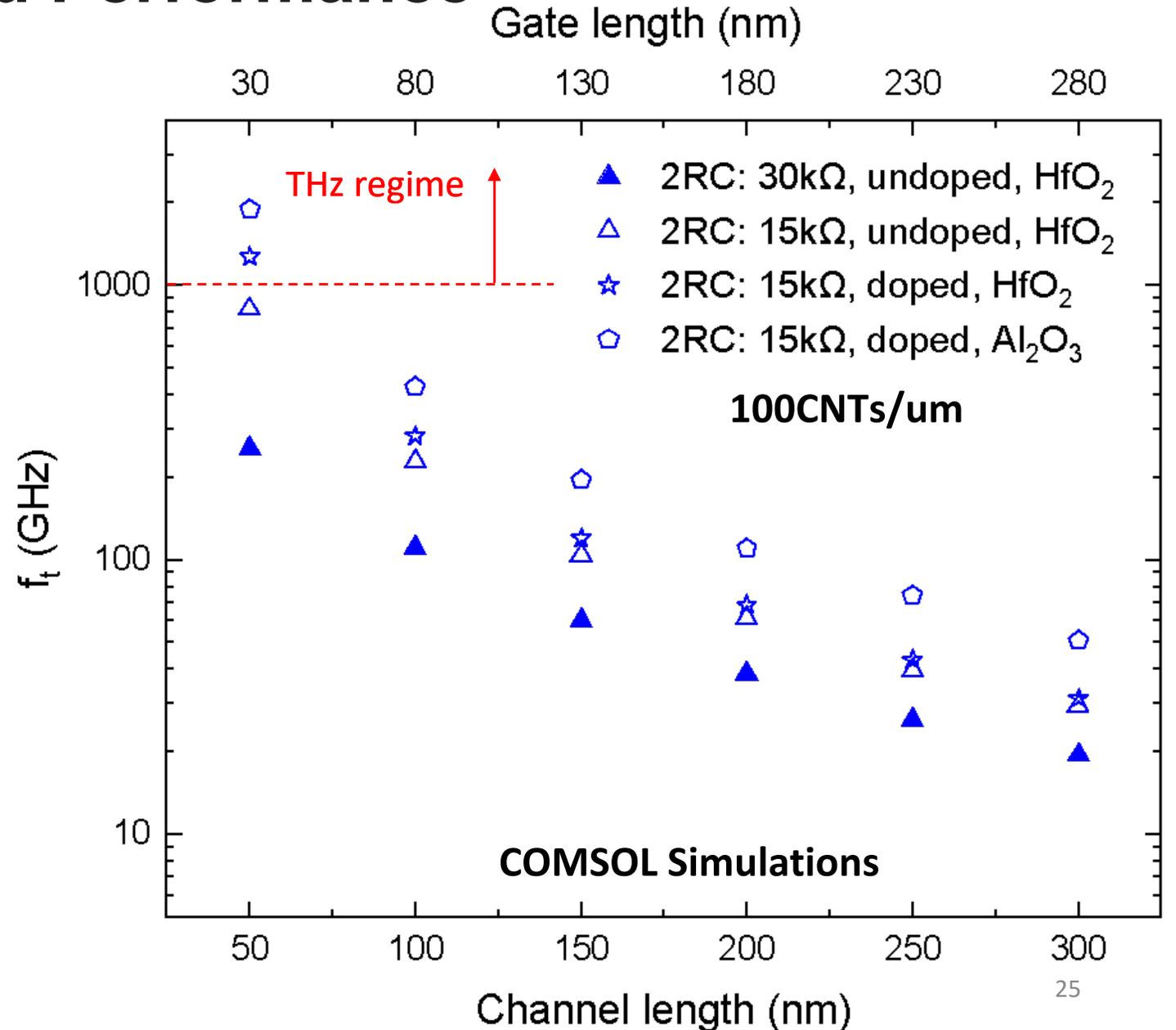
5x improvement



## 3) Use lower $\kappa$ gate oxide

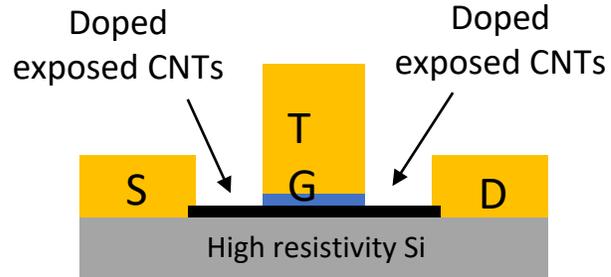
8x improvement

HfO<sub>2</sub>  $\kappa$ : 20  $\longrightarrow$  Al<sub>2</sub>O<sub>3</sub>  $\kappa$ : 7

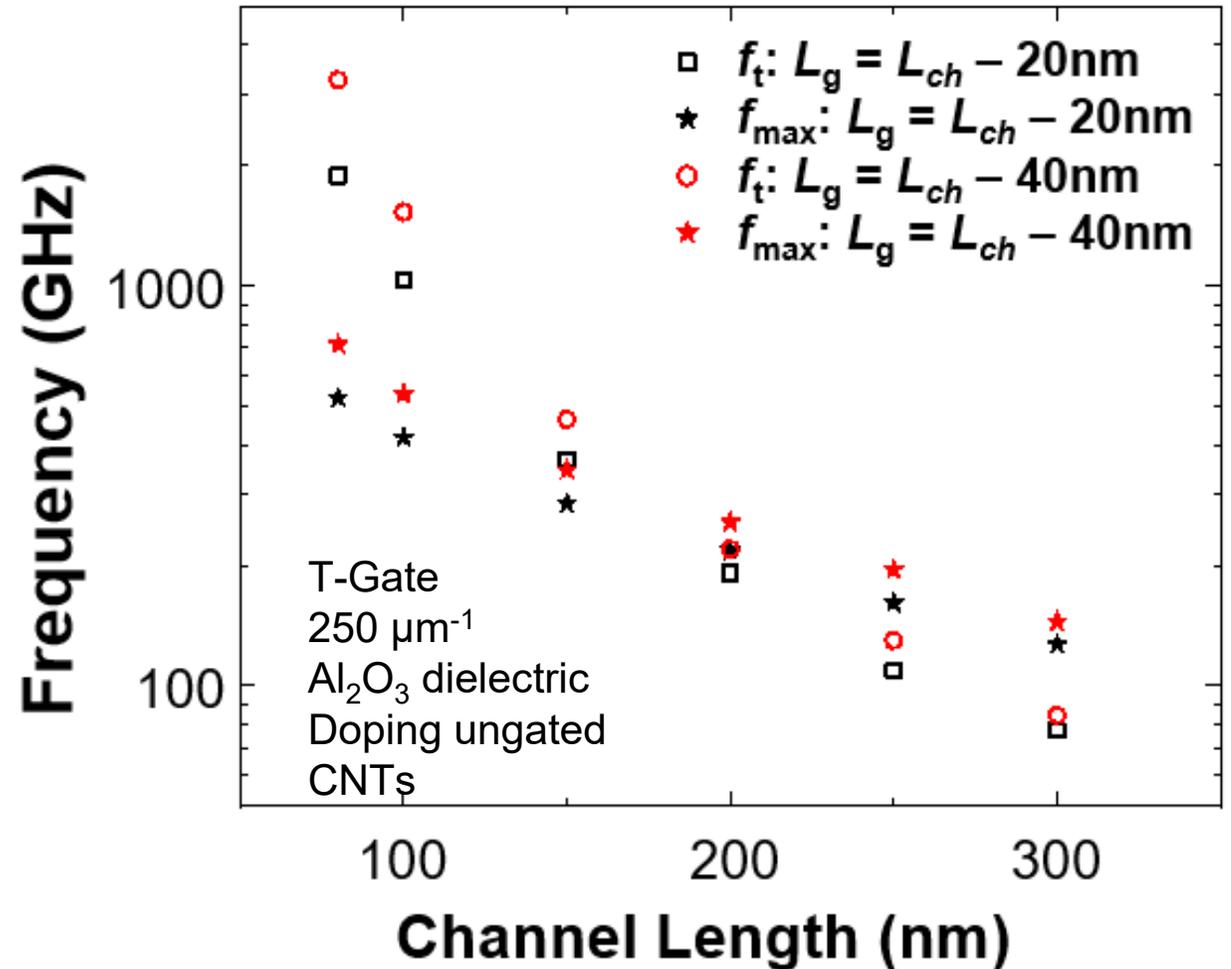
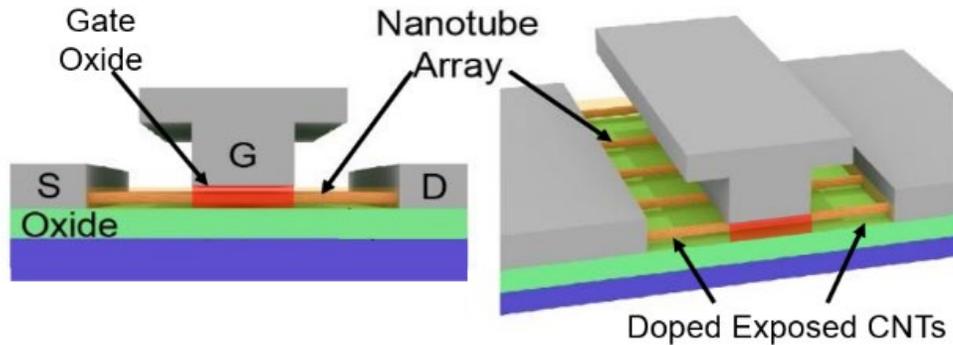


# Next Steps for Improved Performance: T-Gate

## I-Gate Architecture



## T-Gate Architecture



# Intellectual Property



IP licensed from UW patenting office (WARF), finalized in Q1 2024.

DATE	FILING TYPE	NUMBER	TITLE	INVENTORS	STATUS
2023	U.S. Patent Application	US P230360US01	“Patterned surface water assisted packing density and alignment enhancement of carbon nanotube arrays”	Michael Arnold, Sean Foradori	Filed
2022	U.S. Patent Application	US 17/591,711	“Selected-area deposition of highly aligned carbon nanotube films using chemically and topographically patterned substrates”	Padma Gopalan, Jonathan Dwyer, Katherine Jenkins, Michael Arnold	Filed
2021	U.S. Patent	US11631814	“Two-dimensional carbon nanotube liquid crystal films for wafer-scale electronics”	Michael Arnold, Katherine Jenkins, Padma Gopalan	Approved
2020	U.S. Patent	US10873026	“Alignment of carbon nanotubes in confined channels”	Michael Arnold, Katherine Jenkins, Gerald Brady, Padma Gopalan	Approved
2018	U.S. Patent	US10074819	“Floating evaporative assembly of aligned carbon nanotubes”	Michael Arnold, Padma Gopalan, Gerald Brady, Yongho Joo, Harold Evensen	Approved
2017	U.S. Patent	US9728734	“Aligned carbon nanotubes for use in high performance field effect transistors”	Michael Arnold, Padma Gopalan, Gerald Brady, Yongho Joo	Approved
2016	U.S. Patent	US9327979	“Methods for removing polymer coatings from single-walled carbon nanotubes”	Padma Gopalan, Michael Arnold, Yongho Joo, Gerald Brady, Matthew Shea	Approved