

OVERVIEW

This Serializer PHY is implemented in Global Foundries 22FDX CMOS technology. The IP macro offers 1x lane with data rate up to 12.5 Gbps and low power consumption (16mW at 12.5GHz), in a compact footprint (140x105 μm^2). By paring with additional macros/lanes and our Deserializer IP macro, a complete SerDes solution attaining an overall 100 Gbps+ can be achieved.

KEY FEATURES

- JESD204C-B12 semi-compliant
- Data rate up to 12.5Gbps per lane
- 1-lane per IP macro
- High-speed differential driver
- GF22FDX-/PLUS CMOS technology

TARGET APPLICATIONS

- SoCs requiring multi-Gbps data rates
- Radar Applications
- Satellite Communications
- Wireless Communications

DELIVERABLES

- GDSII layout
- Verilog (or SystemVerilog) model
- Integration support
- DRC, LVS reports
- Datasheet including characterization results
- CDL netlist for LVS
- LEF files
- Verification report

BLOCK DIAGRAM

