

OVERVIEW

This Deserializer PHY is implemented in Global Foundries 22FDX CMOS technology. The IP macro offers 2x lanes with data rate up to 12.5 Gbps per lane and low power consumption (36 mW at 12.5Gbps). Its compact footprint makes it an excellent choice for SoC designs that require ultra-high data rates such as A/D and D/A converters. By pairing with additional macros/lanes the overall achievable data rate can exceed 100 Gbps.

KEY FEATURES

- JESD204C-B12 semi-compliant
- Data rate up to 12.5Gbps per lane
- 1-lane per IP macro
- GF22FDX-/PLUS CMOS technology

TARGET APPLICATIONS

- SoCs requiring multi-Gbps data rates
- Radar Applications
- Satellite Communications
- Wireless Communications

DELIVERABLES

- GDSII layout
- Verilog (or SystemVerilog) model
- Integration support
- DRC, LVS reports
- Datasheet including characterization results
- CDL netlist for LVS
- LEF files
- Verification report

BLOCK DIAGRAM

