AIX-PLL-12P5G-GF 22FDX

OVERVIEW

This PLL is implemented in Global Foundries 22FDX CMOS technology. It offers ultra-low jitter (600fs-rms at 12.5GHz) and low power consumption (5.3mW at 12.5GHz), with an operational range from 6GHz to 12.5GHz. Its ultra-compact footprint makes it an excellent choice for SoC designs that require multiple clock domains. As an integer-N PLL, it provides designers with the flexibility to optimize clock domains across the entire system.

KEY FEATURES

- Output frequency: 6GHz-12.5GHz
- Small area: 95x85 um^2
- Low jitter: 600fs rms-jitter at 12.5GHz
- Low power: 5.3mW at 12.5GHz
- Reference clock: 50MHz
- Programmable integer divider
- GF 22FDX CMOS technology
- Silicon Proven

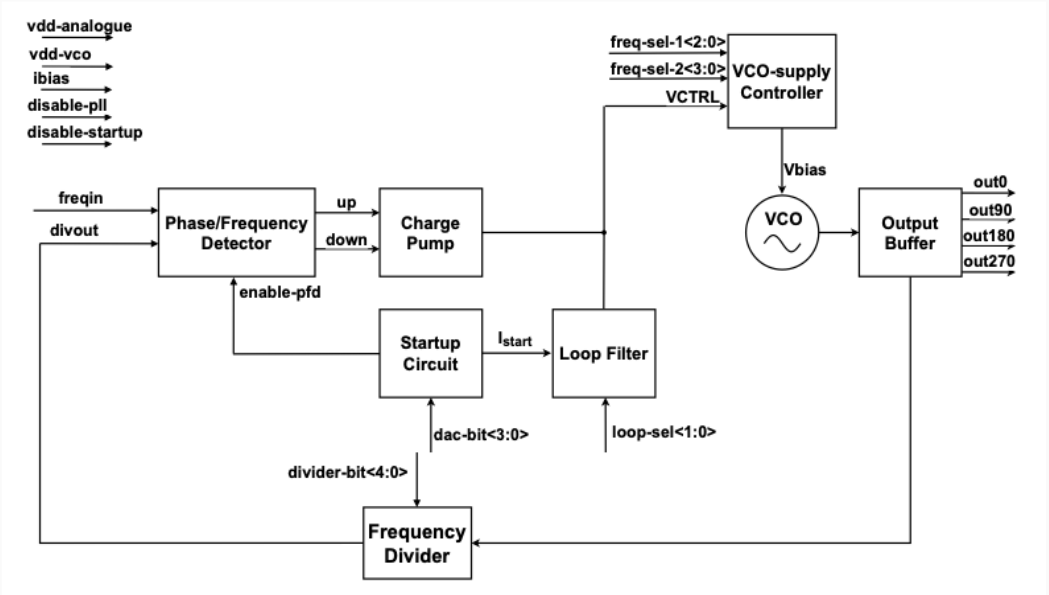
TARGET APPLICATIONS

- SoCs requiring multiple-clock domains
- ADC and DAC
- High-speed SerDes

DELIVERABLES

- GDSII layout
- Verilog (or SystemVerilog) model
- Integration support
- DRC, LVS reports
- Datasheet including characterization results
- CDL netlist for LVS
- LEF files
- Verification report

BLOCK DIAGRAM



Contact us at **ip@incirt.de** for more information.