

## OVERVIEW

This PLL is implemented in Global Foundries 22FDX CMOS technology. It offers a wide tuning range (from 5GHz to 7.5GHz) and low power consumption (6mW at 7.5GHz). Its ultra-compact footprint makes it an excellent choice for SoC designs that require multiple clock domains. As an integer-N PLL, it provides designers with the flexibility to optimize clock domains across the entire system.

## KEY FEATURES

- Output frequency: 5GHz-7.5GHz
- Small area: 120x80  $\mu\text{m}^2$
- High SFDR: 55dBc at 7.5GHz
- Low power: 6mW at 7.5GHz
- Reference clock: 500MHz
- Programmable integer divider
- Programmable charge pump
- GF 22FDX CMOS technology

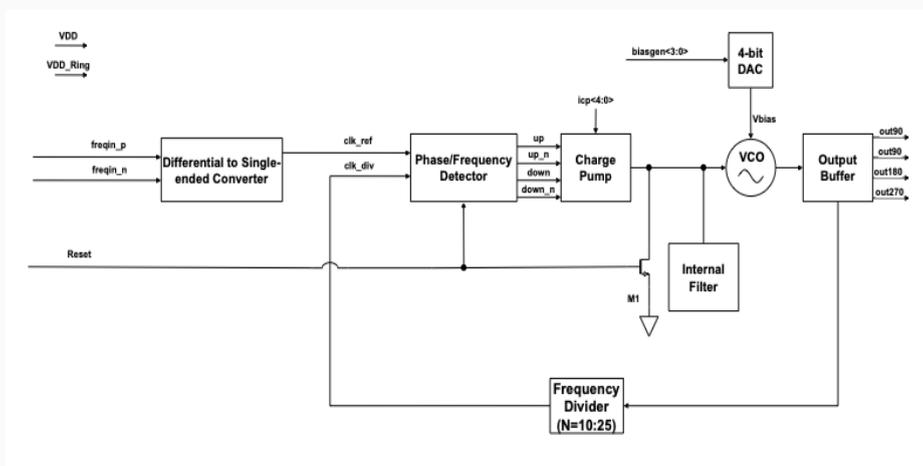
## TARGET APPLICATIONS

- SoCs requiring multiple-clock domains
- ADC and DAC
- High-speed SerDes

## DELIVERABLES

- GDSII layout
- Verilog (or SystemVerilog) model
- Integration support
- DRC, LVS reports
- Datasheet including characterization results
- CDL netlist for LVS
- LEF files
- Verification report

## BLOCK DIAGRAM



Contact us at [ip@incirt.de](mailto:ip@incirt.de) for more information.