

OVERVIEW

This PLL is implemented in Global Foundries 22FDX CMOS technology. It offers a wide tuning range (from 3.0GHz to 4.0GHz) and low power consumption (4.5mW at 4.0GHz). Its ultra-compact footprint makes it an excellent choice for SoC designs that require multiple clock domains. As an integer-N PLL, it provides designers with the flexibility to optimize clock domains across the entire system.

KEY FEATURES

- Output frequency: 3.0GHz - 4.0GHz
- Small area: 120x125 μm^2
- Low jitter: 3ps-rms jitter at 4.0 GHz
- Low power: 6mW at 7.5GHz
- Reference clock: 125MHz
- Programmable integer divider
- Outputs with different phases (0° , 90° , 180° , and 270°)
- GF 22FDX CMOS technology

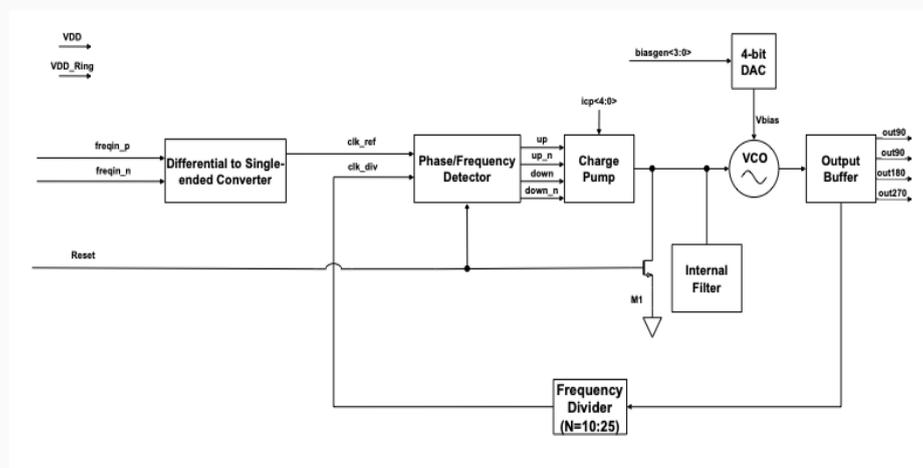
TARGET APPLICATIONS

- SoCs requiring multiple-clock domains
- ADC and DAC
- High-speed SerDes

DELIVERABLES

- GDSII layout
- Verilog (or SystemVerilog) model
- Integration support
- DRC, LVS reports
- Datasheet including characterization results
- CDL netlist for LVS
- LEF files
- Verification report

BLOCK DIAGRAM



Contact us at ip@incirt.de for more information.