Surface Preparation Advances for Die Stacking with Hybrid Bonding

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Abstract

Die-to-wafer (D2W) hybrid bonding is a platform technology that can be used across a wide spectrum of products in the semiconductor industry. One target application is stacked DRAM, High Bandwidth Memory (HBM) module, which plays a key role in propelling advancement in high performance computing (HPC). Fabrication of the thin die for stacking involves a temporary bonding process. Effective removal of carrier wafers and temporary bonding adhesive from the device surface is important in successful die stacking with hybrid bonding. This study reports Adeia's progress in developing a high yield, environmentally friendly process of cleaning thin die surfaces for D2W hybrid bonding.

Key words

Hybrid bonding, D2W, stacking, 3D, temporary bonding/debond, adhesive residue, Cu loss in cleaning, surface preparation

I. Introduction

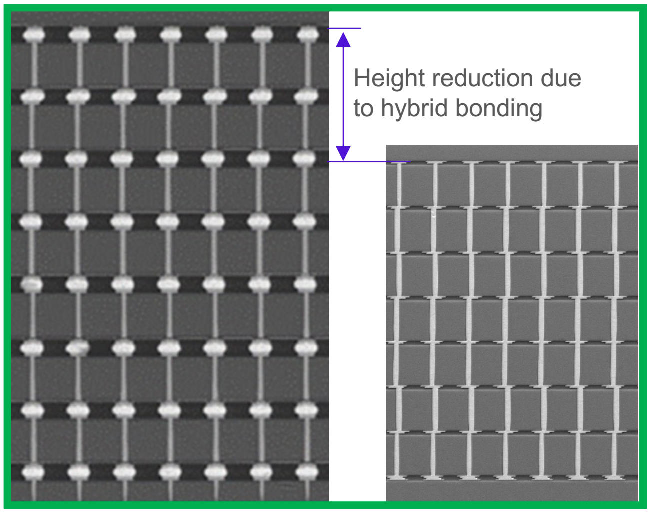
Die-to-wafer (D2W) hybrid bonding is a platform technology that can be used across a wide spectrum of products in the semiconductor industry [1]. Stacked DRAM High Bandwidth Memory (HBM) is a prime candidate for D2W hybrid bond interconnect with the enhanced thermal and electrical performance. Demand for HBM has increased sharply due to the important role it plays in the advancement of AI technologies. Hybrid bonded 8-die and 16-die stacks have been demonstrated [2]--[4]. Figure 1 shows a side-by-side comparison of an 8-die stack assembled with solder microbump and hybrid bonding. The solder assembly results in 8 solder/underfill layers each approximately 20μm thick between the dies. These thick solder/underfill layers are eliminated with hybrid bond interconnect. The results are reduced stack height, improved thermal, electrical and reliability performance.

An engineering challenge for high-volume manufacturing (HVM) of hybrid bonded HBM is die stacking yield, which is sensitive to the cleanliness and topography of the thin die surface. Thin die fabrication involves the use of temporary bond adhesives and carrier wafers for wafer backside processing.

Traditional wafer debond methods include chemical release, thermal slide, mechanical peeling, and laser release (YAG laser or UV laser). Photonic debonding [6], [7] is a new debonding method that can potentially simplify the debonding process and reduce cost.

After the carrier wafer is removed, the adhesive layer must be removed. Commonly used methods include mechanical peeling and organic solvent dissolution. For years, the criteria for cleanliness is based on requirements for a solder reflow process. With the 20μm thick solder and underfill layer between dies serving as a buffer for particles, the solder reflow process is more tolerant towards residues left on the surface. In addition, the solder reflow process is not sensitive to metal variation in the nanometer range that can result from the adhesive removal process.

Now, with hybrid bonding being an all-solid, molecular scale bonding, a pristine dielectric surface with shallow and uniform recess in the metal are desired. To achieve void-free bonding and formation of interconnect at anneal temperatures between 200ºC-350ºC, these specifications are preferred. Therefore, it imposes much more stringent requirements for surface cleanliness and Cu topography control during cleaning. In this study, we evaluated two processes for the removal of a thermal plastic adhesive: A solvent dissolution process compatible with soldering, and a new, non-solvent process.

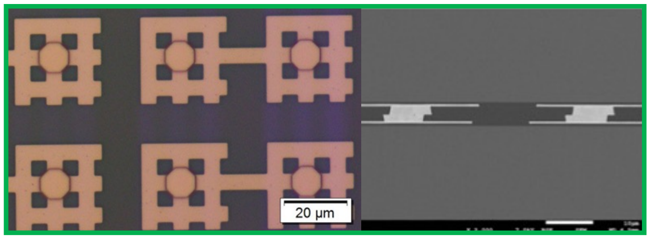


(a) (b)

Figure 1: Height comparison of an 8-die stack assembled with: a) a solder micro-bump [5] and b) a hybrid bonded 8-die stack [2] with the same die thickness.

II. Experimental Procedures

We conducted two rounds of temporary bond/ debond (TB/DB) and cleaning experiments using a thermal plastic adhesive. The glass carrier wafer with a non-organic light absorption layer (LAL) was developed by the photonic debonder equipment supplier [6]. Two types of wafers were bonded in each round: silicon wafers with thermal oxide on the surface and daisy chain test wafers with Cu pads embedded in a silicon oxide layer. Figure 2 shows a surface and cross-sectional image of the daisy chain design used for the atomic force microscopy (AFM) and die-to-wafer (D2W) hybrid bonding studies. The die size is 8mm x 12mm with a Cu pad diameter of 10µm, and the bonding pitch is 40µm. Adeia has accumulated hundreds of lots of D2W bonding data with this test vehicle. The baseline oxide roughness and Cu recess of the daisy chain wafers were measured before the temporary bonding experiments commenced.



(a) (b)

Figure 2. Surface optical image (a), and cross-sectional image (b) of the daisy chain wafer design used for AFM and D2W bonding study, with circular bond pads in the top layer and grid-shaped pads and lines in the RDL layer.

Wafer bonding for both rounds was carried out by our partner. For the first round of study, the adhesive was removed using a solvent dissolution process compatible with soldering. There were limitations in chemical cleaning choices simply because it was completed within the partner's facility. Round 1 study was limited to full-thickness wafers only.

Round 2 of the study was conducted after Adeia installed a photonic debonder in our facility. Bringing the debonding capability in-house allowed us to develop environmentally friendly, organic solvent-free residue-cleaning procedures. Round 2 study was more rigorous and incorporated wafer thinning, dicing, and D2W bonding evaluations.

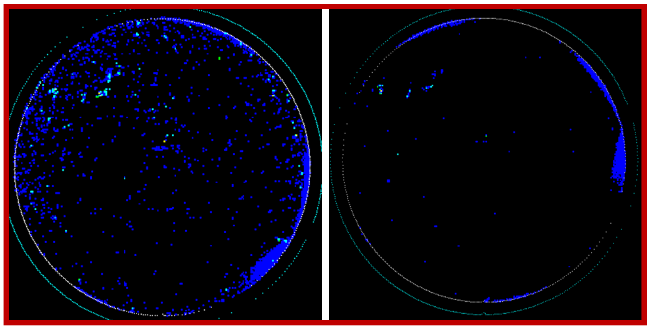
The surface cleanliness of the oxide wafers after removing the adhesive layer was evaluated using a Surfscan bare wafer surface defect inspection system. Sequential measurements were conducted following different process steps. To correlate surface residue level to bonding interface voiding, oxide wafers from Round 1 and Round 2 were bonded to clean oxide wafers at different cleaning process steps. One pair was bonded before additional cleaning at Adeia. A second pair was bonded after additional cleaning at Adeia. Bonding interface voids were measured using C-mode scanning acoustic microscopy (CSAM).

The impact on Cu loss was determined by sequential AFM measurement on the daisy chain wafers after various process steps.

III. Results and Discussion

The oxide wafers from the Round 1 study after adhesive removal by solvent cleaning were examined by Surfscan. Measurements were carried out in both particle and haze modes. For this group of wafers, the haze mode visualized the residue better than the particle mode. As shown in Figure 3a, the blue and green areas depict contaminated areas across the wafer surface. The excessive residue prevented the collection of meaningful oxide roughness and Cu recess data by AFM on the daisy chain wafers at this step.

A non-solvent cleaning procedure developed by Adeia removed significantly more residue, and the surfscan measurements show the residue signature on the wafer as shown in Figure 3b. At this step, the particle mode captured more details on the surface contaminants. The parameters best correlated to direct bonding interface voids are the particle counts between 5-28µm in size and the area contaminated with particles >28µm in size.



(a) (b)

Figure 3: Haze image of a Round 1 oxide wafer after solvent removal of the adhesive (a), and after further cleaning by Adeia (b). The blue areas at the wafer edge are artifact produced by the Surfscan tool.

Figure 4 compares the surface contaminant levels of the oxide wafers from Round 1 and Round 2 studies. The Adeia cleaning procedure used in Round 2 reduced the 5-28µm size particle count by 90%, from 48 to 5, and the area contaminated with >28µm size particles by 65%, from 0.844mm^2 to 0.292mm^2. The process can be further optimized to minimize surface contamination.

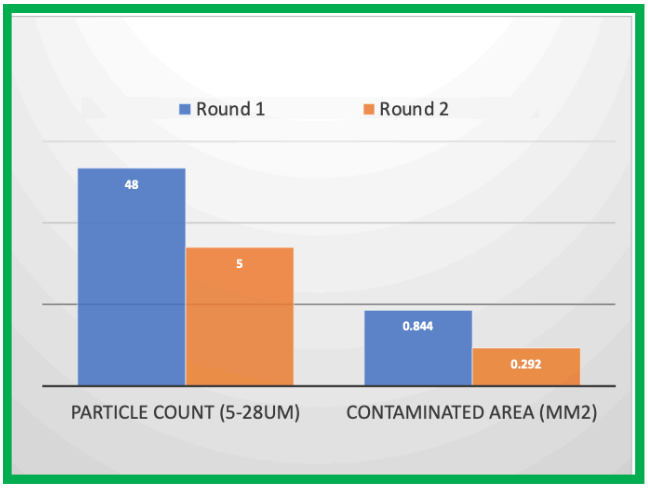


Figure 4: Comparison of particle counts (5-28µm size) and contaminated area (>28µm) for Round 1 and Round 2 after cleaning at Adeia.

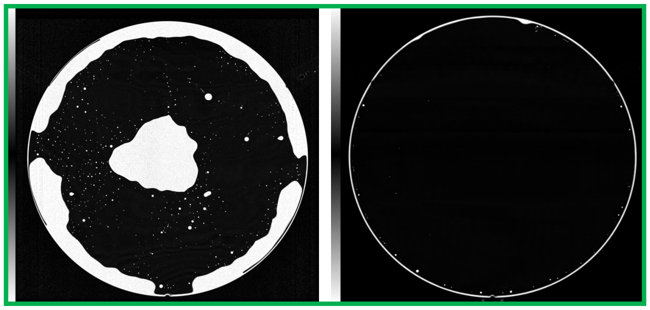
The daisy chain wafers with Cu bond pads were cleaned using the same procedure before the final AFM measurement. The data were compared to the baseline data collected before the TB/DB experiment to deduce the amount of Cu lost through the entire temporary bonding/ backside grinding/ debond/ adhesive removal/ residue cleaning procedure. The oxide roughness showed no change from the baseline for both Round 1 and Round 2 wafers, indicative of a good cleaning process. The Cu recess change after the Round 2 process is consistent with the Adeia baseline process established over the years. However, for the daisy chain wafers in the Round 1 study, the Cu pads showed significantly deeper Cu recess than Adeia's baseline process. The extra Cu loss from the Round 1 processing ranged from 24 to 35nm, with an average of 30nm. Since the major difference in the two processes is the solvent dissolution step used to remove the adhesive, it is likely to have a much higher Cu removal rate than the Adeia non-solvent process.

One of the oxide wafers from the Round 1 study was bonded to a clean oxide wafer after the solvent removal process to determine the quality of the surface for bonding. The temporary bond residue left after the solvent cleaning resulted in massive interface bonding voids, as shown in Figure 5a. This example demonstrates Surfscan is an effective metrology tool for properly evaluating temporary bond residue removal for hybrid bonding. Although the Adeia cleaning procedure removed the majority of the surface residue (Figure 3), the additional 24-35nm Cu loss caused by the solvent cleaning step is much less likely to be successful in manufacturing, as it is apt to create an open circuit failure for hybrid bond interconnect. Unfortunately, the solvent cleaning procedure that is compatible with solder microbump assembly is not compatible with hybrid bonding.

In contrast, the bond quality of the Round 2 oxide wafer was void free, indicating an ultra-clean perfectly bonded interface between the wafers , as shown in the CSAM in Figure 5b.

With the encouraging results obtained at the full-thickness wafer evaluation in Round 2, we thinned a subset of the wafers to 65µm thickness and conducted debond, cleaning, and D2W hybrid bonding studies. The electrical continuity yield after a 300°C anneal is 95%, consistent with our process of record on the same test vehicle over the years. The electrical continuity indicates clean interfaces between the die and wafer. Figure 6 shows a representative CSAM image. All the void-free dies passed the electrical continuity test. As expected, the one voided die failed the electrical test. The void created here was identified as particulate not associated with temporary bond residue. The results validated the compatibility of the Adeia cleaning process with hybrid bonding to maintain cleanliness and Cu recess control throughout the die preparation process.

The result from this preliminary study is very promising. Further studies are planned to optimize the removal process of this adhesive material and expand the scope of the study to address more adhesive materials.



(a) (b)

Figure 5: CSAM image of the bonding interface of oxide wafers: a) wafer with adhesive residue from Round 1 study, (b) Wafer cleaned with the Adeia non-solvent cleaning process from Round 2 study.

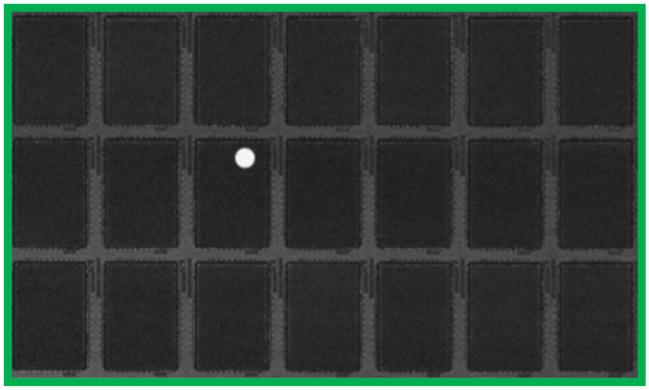


Figure 6: CSAM image of the 65um thick dies bonded to a host wafer.

IV. Conclusion

Surface particle measurement and Cu recess measurement conducted on wafers that were exposed to temporary bonding process using a thermoplastic adhesive, debonded, and cleaned with two different cleaning solutions. The off-the-shelf organic solvent cleaning process, which is compatible with a soldering process resulted in massive interface voiding in direct bonding and show excessive Cu loss, making it incompatible with hybrid bonding.

A non-solvent, environmentally friendly adhesive residue cleaning process developed at Adeia enhanced surface cleanliness and eliminated excess Cu removal. The dies subjected to the Adeia cleaning process showed both high void-free bonding yield and high electrical test yield.

The results highlight the need to methodically test the device surface after the TB/DB processing for surface cleanliness and surface topography for any hybrid bonding assembly. Surfscan, CSAM, and AFM are all effective metrology tools to evaluate the surface quality of pre-bond and post-bond device surfaces for hybrid bonding.

Acknowledgment

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