Hybrid Bonding: To Be or Not To Be?

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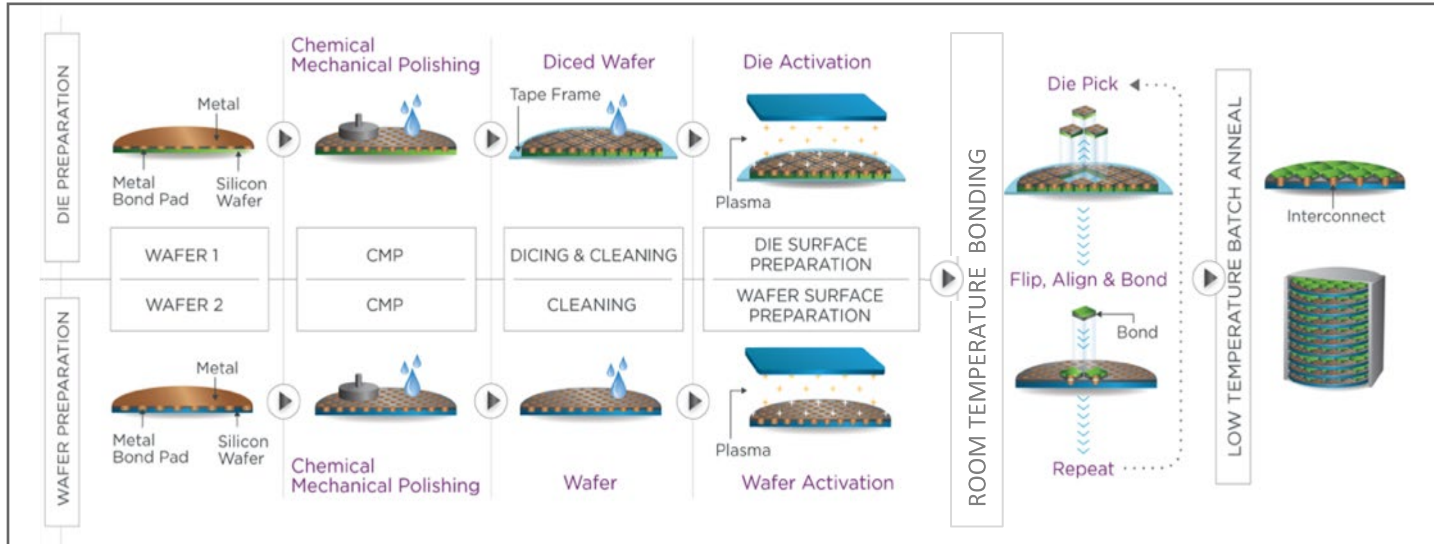
Key Metrology for Improved Yield and Throughput



Assumptions

- High yield BEOL
- Lithography
- Etch
- Plate

Pre- Bond Metrology

- Surface Topography[1,2]
- Surface Defects[3]
- Grain Structure
- Wafer and Die Warp

Post Bond Metrology

- Bond Energy[4]
- Bond Voids
- Electrical Connectivity

Must Haves

- Reliable metrology tuned to performance
- Establish a "health of the line" protocol for all process steps

Wants

- Improved Nanoscale Topography[1]
  (KGD processes more sampling/higher yield)
  - Accurate & Fast for High Volume
  - Interferometry ~1000x Faster than AFM[1]
  - Fine pitch (optical techniques and accuracy)
- Surface Defect Detection[2]
  - Large-area automated detection: ML

Stretch Goal

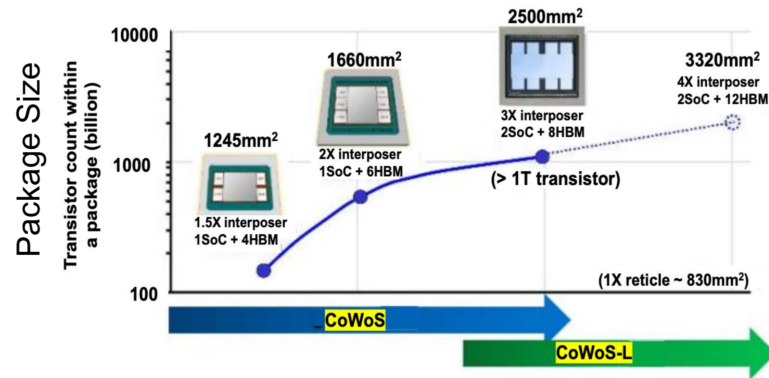
- Rework Hybrid Bonding
  - High-cost Die / Stack Replacement
  - Bond Energy Engineering

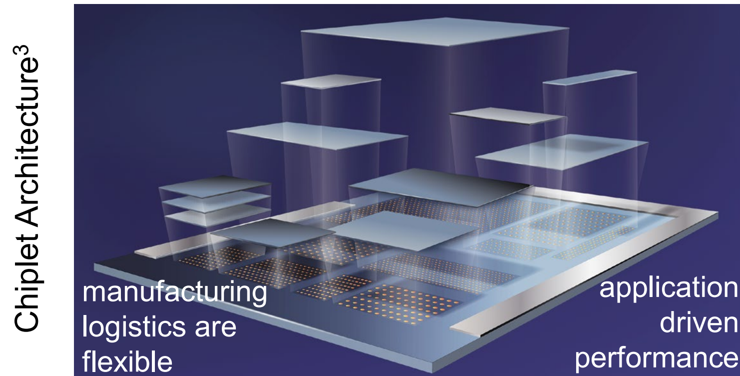
1. Bongsub Lee et al., "High-Throughput Characterization of Nanoscale Topography for Hybrid Bonding by Optical Interferometry," ECTC 2024.
2. Bongsub Lee et al., "Nanoscale Topography Characterization for Direct Bond Interconnect," ECTC 2019.
3. Oliver Zhao et al., "Deep Convolution Neural Networks for Automatic Detection of Defects which Impact Hybrid Bonding Yield," ECTC 2024.
4. Bongsub Lee et al., "Mechanical Strength Characterization of Direct Bond Interfaces for 3D-IC and MEMS Applications," ECTC 2018
5. G. Gao and L. Mirkarimi, "Hybrid Bonding Process-Ch. 3; *Direct Cu Bond Interconnection for Advanced Semiconductor Technology*, edited by Dongkai Shangguan CRC Press, 2024.

2.5 & 3.5D Packaging Evolution with Hybrid Bonding

Package Trends

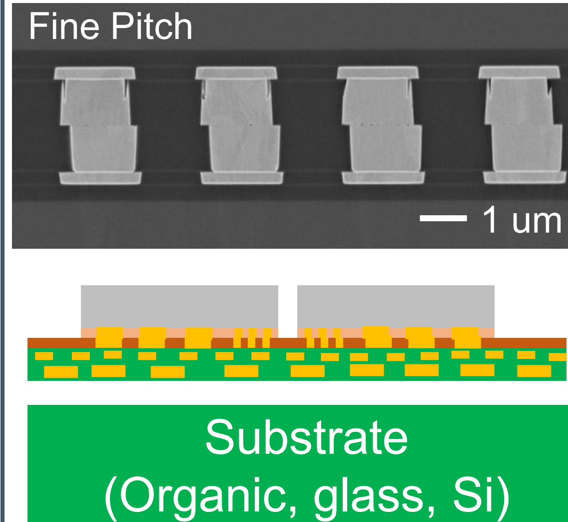
- Package size is >3x reticle size. [1]
- Heterogenous integration with high I/O density
- Chiplet architecture for application optimization



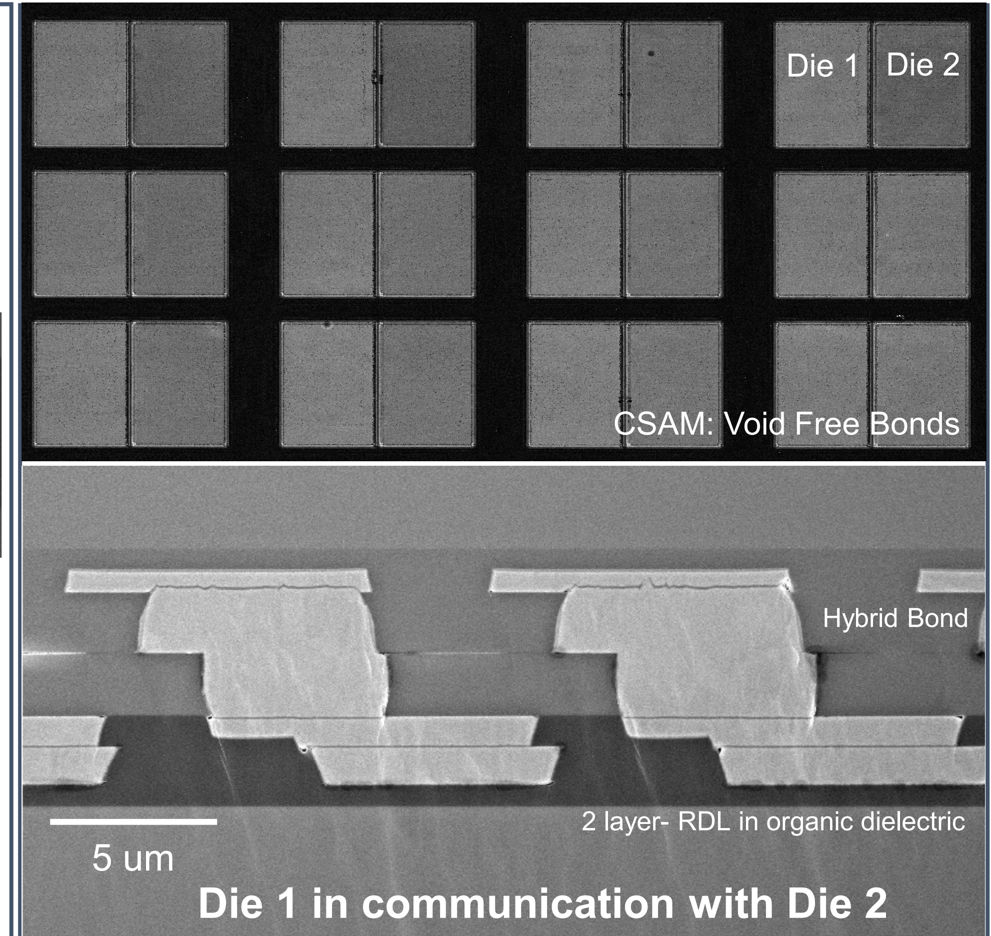


Solving Challenges

- Ultra-high bandwidth, inter-die communication with D2W pitch down to 1um.[2]
- System simplification
  - Bond die directly to substrate
  - Bridge die replace interposer



Hybrid Bonded Die to Organic RDL[4]



1. Hu, et al, "CoWoS Architecture Evolution for Next Generation HPC on 2.5D System in Package", ECTC 2023.
2. Theil, et al, " Recent Development in Fine Pitch W2W Hybrid Bonding with Cu Interconnect", IWLPC 2019.
3. L. Mirkarimi et al, "Hybrid Bonding Technology for Chiplets", Tutorial Session C, Chiplet Summit 2022, Santa Clara, January 2022.
4. Adeia, unpublished.

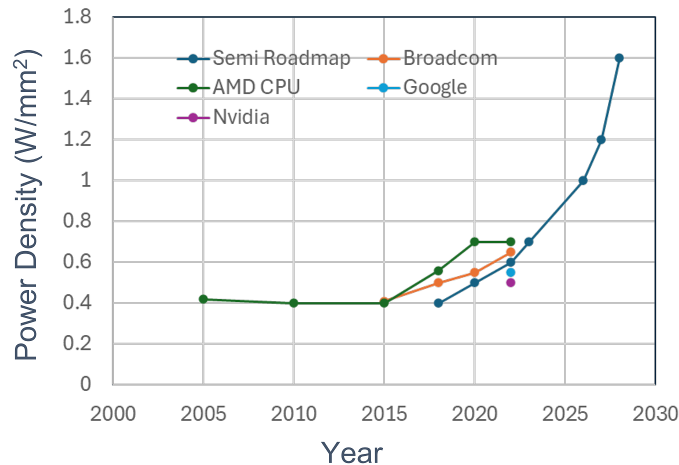
Thermal Solutions for High Power Density Chipsets

IEEE ELECTRONICS PACKAGING SOCIETY

ECTC — The 2025 IEEE 75th Electronic Components and Technology Conference

The Challenge

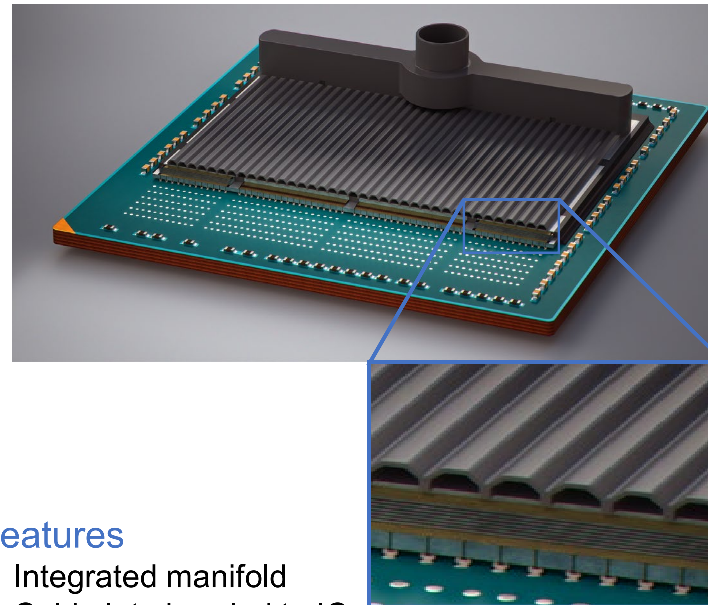
Power Density Roadmap



- AI workflows and large language models are driving the high-power densities in ICs.
- New cooling technologies are emerging (micro-jetting, immersion, and others…)[1,2]

Hybrid & Direct Bonding Solutions

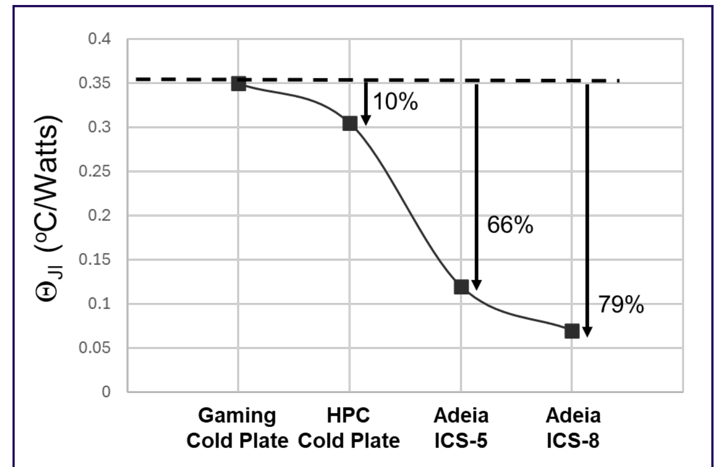
Integrated Cooling Solution[3,4]



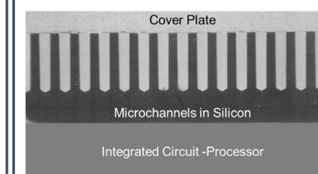
Features

- Integrated manifold
- Cold plate bonded to IC
- Eliminate TIM, reduce thermal resistance
- Inexpensive fab process
- Custom design to manage heat map
- Improved thermal performance design
- Tested to 3W/mm^2 power density

Thermal Resistance Reduction



Improved performance over standard TIM based solutions: Gaming and HPC cold plates had silver based and PTM7950 TIMs, respectively.



Early μchannels[5] issues solved with this approach.
- -excessive pressure drop
- -integration

1. M. Walsh, et al., "Embedded microjets for thermal management of high power-density electronic devices", IEEE Trans. Compnts, Pckg. and Man.Tech., vol. 9, no.2, pp. 269–278, Feb. 2019.
2. L.J. Lieu et al, "An Energy-efficient Si-integrated Micro-cooler for High Power and Power-density Computing Applications", ECTC, p.1025-1029. May 2024.
3. R,Zhang et al, "Revolutionary Cooling Solution for Hot Chips", iTherm 2025, May 26th (2025); Session TII-06, Tate Ballroom A2 (11AM)
4. Adeia Booth- ECTC 2025, Booth # 308.
5. D.B.Tuckerman and R.F.W. Pease, IEEE Electronic Device Letters, EDL-2, No. 5, May 1981.

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