

In-memory Analog Computing

Current x time.
Intelligence at the edge.

A programmable current-pulse architecture for parallel vector-matrix multiplication, designed to reduce data movement in AI inference.

The difference is in the cell

Each Programmable Current Pulse Cell (PCPC) combines a programmable current amplitude with an input-controlled pulse duration to perform multiplication through charge generation. Cell contributions are accumulated in parallel along each row, enabling parallel vector-matrix computation with the potential for low-latency inference.

01 REFERENCE-DEFINED WEIGHTS

Local circuitry selects a shared global reference to set each cell's current amplitude.

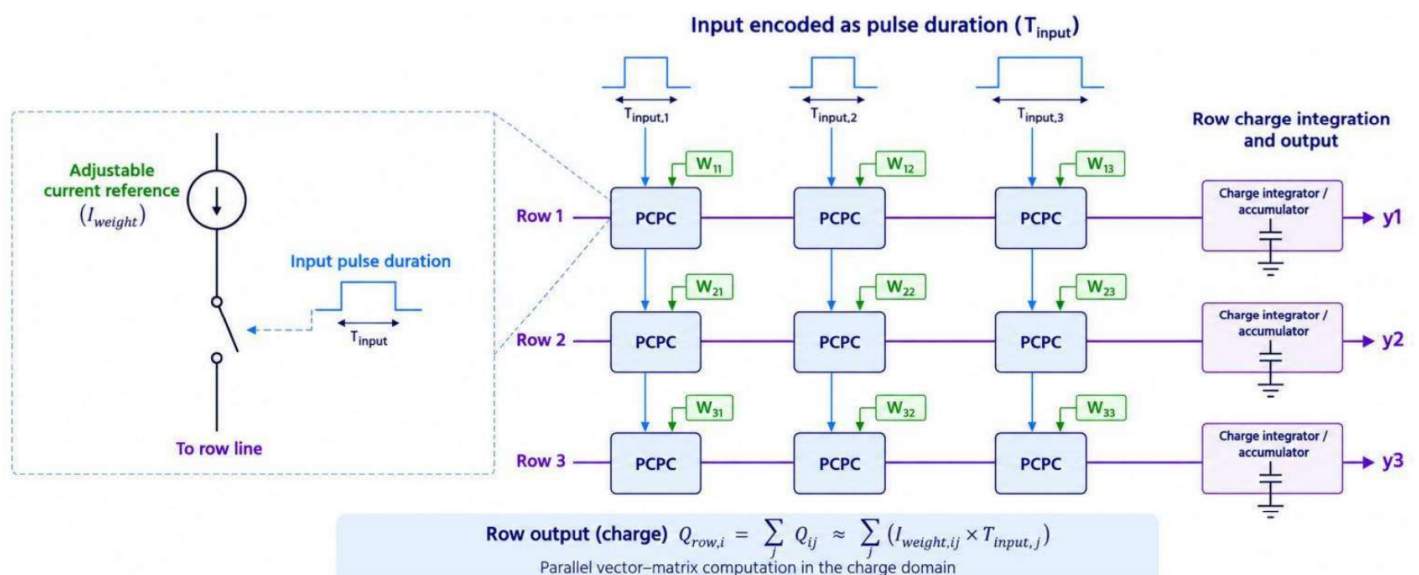
02 TIME-ENCODED INPUTS

Column input pulses control delivery time. Each cell contributes charge $Q = I \times t$.

03 CHARGE-DOMAIN SUMMATION

Row integrators combine cell contributions in parallel to form the output vector.

PCPC ARCHITECTURE



A CMOS path to analog AI

Built on standard CMOS circuitry without relying on memristive devices, PCPC offers a flexible hardware foundation for ANN, CNN, and SNN implementations, subject to appropriate network mapping and peripheral circuitry.

Explore architecture integration and joint development