

28A, Quad Output, DC-DC Step-Down Power Converter Chiplet

Features

- Four independent outputs
- 8 phase buck converter with integrated power switches and power inductors
- Wide loop bandwidth: 10MHz
- Differential point-of-load (PoL) sensing
- Gang operation: up to 32 devices in parallel
- Automatic phase shedding
- Telemetry: Input Voltage, Output Voltage, Output Current and Temperature
- Fault response: UVLO, OVP, UVP, OCP, OCP Warn, VRHOT, and OTP
- 1 MHz PMBus 1.3 compliant serial interface
- 50 MHz AVSBus 1.4 compliant serial interface enabling Dynamic Voltage Scaling (DVS)

Applications

- GPUs, TPUs, ASICs and FPGAs
- Data center processors

General Description

The Fe1728 is a quad output power convert chiplet. Each of the 4 outputs are able to act completely independently to a maximum of 7A each, or they may be combined to allow for higher currents. The Fe1728 is a 8-phase interleaved buck converter with a fully integrated powertrain, including power inductors. The Fe1728 integrates digital interface, power management, voltage control and powertrain circuitry (including power FETs, inductors and capacitors) all in a single device. The Fe1728 delivers precise voltage, fast transient response, and high bandwidth regulation. A high switching frequency powertrain drives Ferric's magnetic composite integrated inductor technology; delivering high efficiency, high-quality power in a small footprint and volume to reduce board area, layout complexity, and component count.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
VIN Voltage Range	V_{IN}	$AVDD18 \geq V_{IN}$	1.6	1.8	2.0	V
Output Voltage Range	V_{OUT}	$V_{IN} \geq 1.8V$	0.25		1.5	V
Output Voltage Resolution	$V_{OUT,RES}$			1.7		mV
Total Steady State Output Current	$I_{OUT,TOT}$				28	A
Number of Output Domains	$N_{DOMAINS}$		1		4	Domains
Total Powertrain Phases	N_{PHASES}				8	Phases
Width	W		2.950	2.990	3.030	mm
Length	L		5.010	5.050	5.090	mm
Area	A			15.1		mm ²
Thickness	T		0.705	0.725	0.745	mm
Current Density (TDC)	$j_{max,TDC}$				1.9	$\frac{A}{mm^2}$
DC Line Regulation	$\left(\frac{\Delta V_{OUT}}{V_{OUT}}\right)_{Line}$	$V_{IN}=[1.6,2.0]V$		± 0.5		%
DC Load Regulation	$\left(\frac{\Delta V_{OUT}}{V_{OUT}}\right)_{Load}$	$I_{OUT}=[0,28]A$		± 0.5		%
Switching Frequency	f_{SW}		25	31	100	MHz
Thermal Resistance Junction to Top	$\Theta_{JC,TOP}$			0.1		$\frac{^{\circ}C}{W}$
Thermal Resistance Junction to Bottom	$\Theta_{JC,BOT}$			3.9		$\frac{^{\circ}C}{W}$