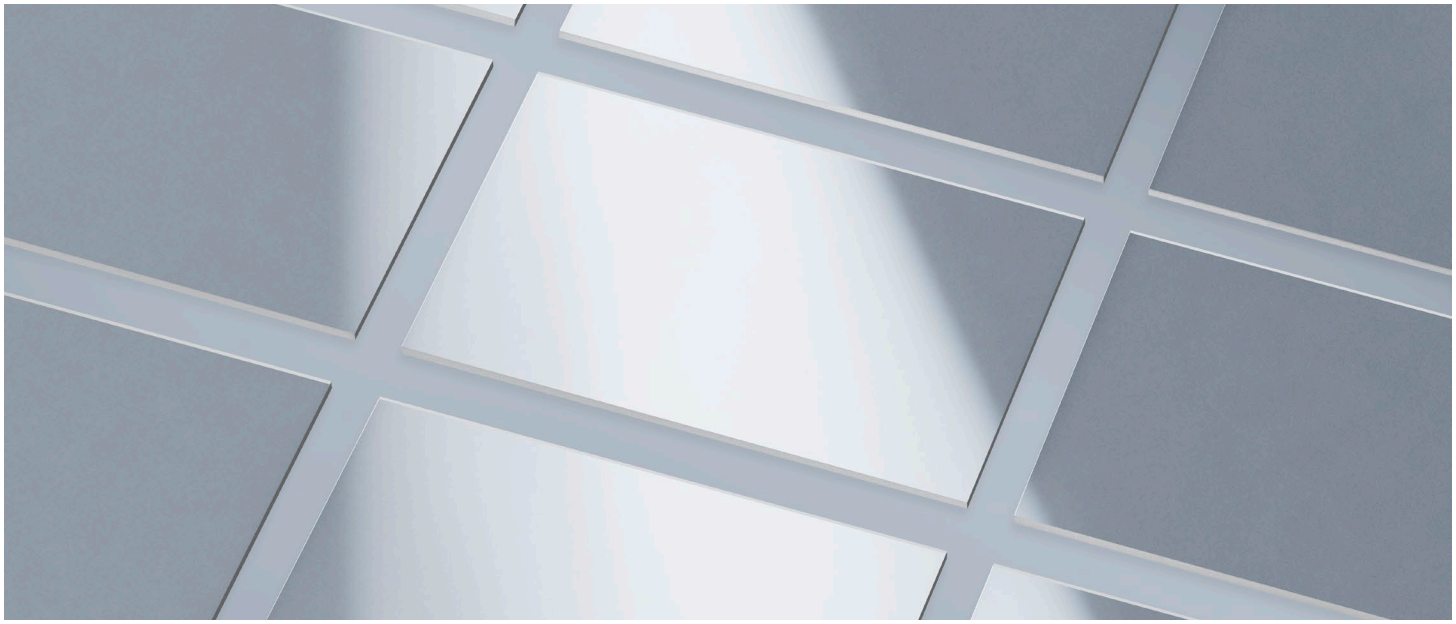
Fab-Bondable Single-Crystal Diamond (SCD) Chip Substrates

The ultimate in thermal performance.

Single-crystal diamond (SCD) plates up to ASML reticle limit size. Trimmed to chip size within ±0.025 mm. Surface finished for chip wafer bonding. Three grades of isotropic thermal conductivity.

Flatten frontside hotspots and boost backside cooling capacity for an enhanced thermal envelope.

Scale power and/or reduce peak temperature accelerated chip failure mechanisms for extended lifetime.



Representative SCD chip substrates.

THERMAL GRADES

1,800 W/mK

2,200 W/mK

2,800 W/mK

QUALITY & DELIVERY

Manufactured under an ISO 9001 (July 2027) quality system with cleanroom particle control.

Each part ships cleaned and inspected to the specifications on page 2, with a certificate of conformance.

FORMAT	TTV	CLEANROOM	QUALITY
33 × 26 mm	≤5 µm	Class 100	ISO 9001

CATEGORY	PROPERTY	UNIT	SPECIFICATION
DIMENSIONS	Length	mm	33 ±0.025
	Width	mm	26 ±0.025
	Thickness: 300 µm product bins	µm	290 / 300 / 310, each ±5
	Thickness: 650 µm product bins	µm	640 / 650 / 660, each ±5
	Total thickness variation (TTV)	µm	≤5
FLATNESS	Bow	µm	−4 to +4
	Warp	µm	≤5
	Front-side flatness	µm	≤4 (200 µm edge exclusion)
	Back-side flatness	µm	≤4 (200 µm edge exclusion)
ROUGHNESS	Front-side Sa (20 × 20 µm)	nm	≤80†
	Back-side Sa (20 × 20 µm)	nm	≤80
PHYSICAL	Density	g/cm³	3.52 ±0.1
	In-plane thermal conductivity @ RT, mean by grade	W/mK	1800 / 2200 / 2800 (σ = 80)
	Cross-plane thermal conductivity @ RT, mean by grade	W/mK	1800 / 2200 / 2800 (σ = 80)
	Carat weight, by thickness	cts	4.5 (300) / 9.8 (650)
DEFECTS	Edge chipping, front and back side	ea	0, size >100 µm
	Material crack	ea	0
	Surface scratch	ea	0
SURFACE CONTAMINATION	Particle count — ≥1 µm	ea	<5
	Particles >25 µm	ea	0
PACKAGING & SHIPPING	Packaging format	—	Tape-in-frame carrier
	Final clean & pack	—	Class 100 cleanroom cleaned & sealed

†Polished surface finish (Sa ≤0.5 nm), for SAB/PAB bonding, available upon request in limited production. Volume allocation with 12-month lead time.
Certificate of conformance (CoC) supplied with each part.

DIE BONDING

PROCESS	SURFACE FINISH
Thermo-compression bonding (TCB)	STANDARD
Sintering	STANDARD
Metallic adhesives	STANDARD
Plasma-activated bonding (PAB)	POLISHED
Surface-activated bonding (SAB)	POLISHED

Reference bonding processes available from DF operable on tier-1 semiconductor bonding equipment at suitable chip pressure and temperature ranges.

SKUs

THERMAL GRADE	300 µm	650 µm
1,800 W/mK	SCD-1800/300	SCD-1800/650
2,200 W/mK	SCD-2200/300	SCD-2200/650
2,800 W/mK	SCD-2800/300	SCD-2800/650

Order standard formats at www.df.com/buy. Ships to qualified chip companies in batches of 25. All variants 33 × 26 mm. Pricing upon request. Custom thicknesses, sizes and surface finishes are available upon request in R&D quantities.