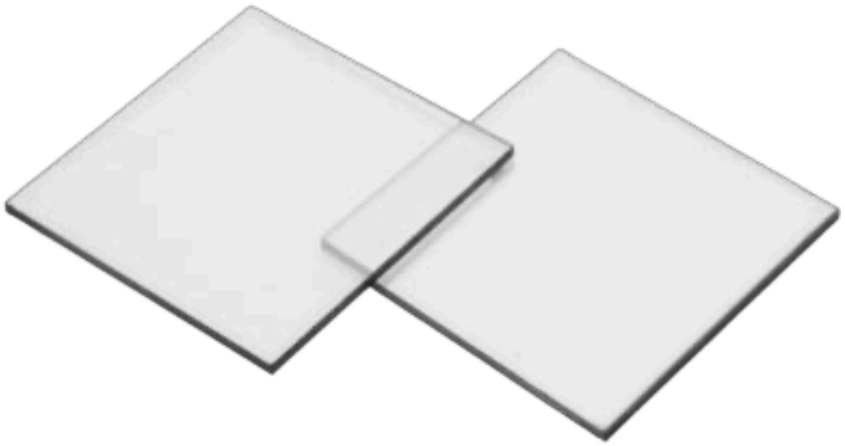
FOR R&D LABS

DF SCD Semi Substrate

Semiconductor substrates for labs developing diamond transistors or bonded transistor devices.

Single-crystal diamond (SCD) substrates with a sub-nanometer polished, low-subsurface-damage surface for epitaxy and device fabrication. Supplied to MOSFET and transistor development labs in 18 × 18 mm, 300 µm format.



18 × 18 mm SCD substrates, 300 µm.

FRONT-SIDE ROUGHNESS	THERMAL CONDUCTIVITY	BREAKDOWN VOLTAGE	FORMAT
Sa ≤0.5 nm	>2,000 W/mK	4,200 V	18 × 18 mm

Use it for all-diamond transistor development, epitaxy, bonding process qualification and thermal test vehicles. Compatible with the epitaxy and bonding processes listed on page 2.

CATEGORY	PROPERTY	UNIT	TEST METHOD	MIN	TYPICAL	MAX
MATERIAL	Material	—	—		Single crystal diamond	
	Crystallographic orientation	°	XRD		[100] ±6	
	Mass density	g/cm³	Gravimetric		3.52	
THERMAL	Thermal conductivity, at RT	W/mK	ASTM E1461-13		>2000	
	Thermal expansion coeff., −50 to 15 °C	µm/m°C	TMA		0.58	
	Thermal expansion coeff., 5 to 35 °C	µm/m°C	TMA		1.04	
	Thermal expansion coeff., 65 to 120 °C	µm/m°C	TMA		1.53	
	Heat capacity, at RT	J/gK	DSC		0.520	
MECHANICAL	Young's modulus	GPa	ASTM E2309, 2658, E4-21		>1000	
ELECTRICAL & OPTICAL	Bandgap (optical)	eV	UV-Vis		5.2 ±0.1	
	Breakdown voltage‡	V	—		4,200	
DIMENSIONS	Length	mm	Non-contact		18 ±0.050	
	Width	mm	Non-contact		18 ±0.050	
	Thickness	µm	SEMI 1530[a]		300 ±25	
	Carat weight‡	ct	—		1.7	
FLATNESS	Total thickness variation (TTV)	µm	SEMI 1530[a]	3.4	4.1	5
	Bow	µm	SEMI MF1390[b]	−1.50	0.60	1.39
	Warp	µm	SEMI MF1390[b]	1.7	2.5	4.3
	Front-side flatness	µm	ISO 1101[b]	2.2	4.2	6.3
	Back-side flatness	µm	ISO 1101[b]	2.9	4.3	6.3
ROUGHNESS	Front-side roughness (Sa)	µm	ISO 25178	0.00015	0.00035	0.00050
	Back-side roughness (Sa)	µm	ISO 25178	0.044	0.048	0.081

[a] Edge exclusion of 500 µm applied. [b] Edge exclusion of 190 µm applied. Values are typical unless min and max are given.
‡ From the df.com product listing; test method not stated.

PROCESS COMPATIBILITY

PROCESS
Epitaxy, all-diamond transistors
Plasma-activated bonding (PAB)
Surface-activated bonding (SAB)
Metallic thermo-compression bonding (TCB)
Sintering

All processes listed are compatible with the Semi surface finish: polished and additionally lapped for minimal subsurface damage (Sa 0.35 nm typical). Reference bonding processes available from DF operable on tier-1 semiconductor bonding equipment at suitable chip pressure and temperature ranges.

SKUs

PRODUCT	FORMAT	SAMPLES
DF SCD Semi Substrate	18 × 18 mm, 300 µm	5-UNIT BUNDLE

Order samples at df.com/buy. Orders in five-unit bundles include a handling fee which covers our significant overhead for small volumes. Contact DF Sales for volume pricing and wafer sizes.