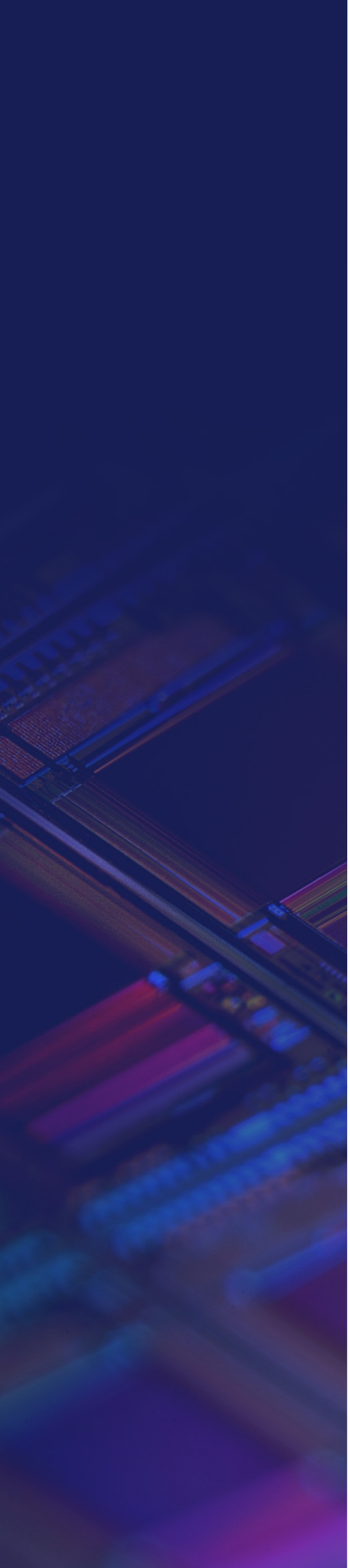


2026 SEMICONDUCTOR INNOVATION REPORT

Gaps, opportunities, and strategic recommendations for Europe

hello tomorrow consulting



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EXECUTIVE SUMMARY

In the past few years, the chips powering AI, electrified transport, and advanced defence have become the assets that nations, corporations, and investors are actively competing to control.

Europe has a unique position in this competition. The continent hosts some of the most structurally irreplaceable companies in the global value chain, such as ASML's monopoly on EUV lithography, Arm's processor architecture omnipresent in smartphones, or Infineon, STMicroelectronics, and NXP's anchor positions in global automotive and industrial supply chains. Yet despite these strengths, Europe still underperforms in converting innovation into broader industrial leadership.

There are a few contradictions throughout the ecosystem. Europe manufactures roughly 10% of the chips it consumes. It holds no domestic capacity for leading-edge logic yet 33% of European semiconductor startups are targeting the compute market. It captures only 7% of global semiconductor startup funding despite producing 25% of the ventures. Only 6% of European semiconductor startups progress past Series A, against 24% in the US and 37% in China.

This challenge has important implications on Europe's positioning strategy. An initial policy response had centred on manufacturing ambition with the first Chips Act targeting a doubling of Europe's global production share to 20% by 2030. However, the structural advantages of TSMC, Samsung, and Intel in leading-edge fabrication have compounded over decades, and are not straightforwardly replicable through policy. It's too late for Europe to join the competition directly in these mature domains.

More promising opportunities lie in the domains where transistor scaling has ceased to be the defining performance lever: compound semiconductors, integrated photonics, quantum hardware, advanced packaging, etc.

Global competitive positions in these areas are still being established, Europe's research institutions are world-class within them, and a generation of startups is already building commercially credible companies across each.

The Chips Act 2.0, proposed by the European Commission in June 2026, begins to reflect this, introducing demand-side measures alongside supply-side investment for the first time. It is a meaningful correction, but one that will take years to implement.

The more immediate challenge lies in closing the gap between laboratory validation to commercial scale, and this requires stronger connections between Europe's research base, startup ecosystem, and industrial incumbents.

Europe already possesses many of the assets needed to build leadership positions in emerging areas, and the competitive window of opportunity is open now. Whether Europe converts its scientific strengths into long-term industrial champions or sees them absorbed into non-European corporate stacks depends largely on how deliberately, and how early, Europe's industrial base chooses to engage.



CHAPTER 01

SILICON, THE WORLD'S MOST STRATEGIC ASSET

- → Semiconductors have become a strategic asset class nations and corporations now compete to control, yet Europe manufactures only ~10% of the chips it consumes and holds no domestic capacity at leading-edge nodes.
- → The Chips Act 2.0 introduces demand-side measures for the first time to improve European competitiveness, but policy alone can hardly close a gap built over decades by Taiwan, South Korea, and the US.
- → Europe's opportunity lies beyond Moore's Law, in the areas of materials, architecture, and integration, where the global landscape is still evolving and the continent's research is world-class.

In October 2025, Nvidia surpassed Microsoft and Apple to become the most valuable company in the world, reaching a market capitalisation of $5 trillion [1].

This milestone was a signal that semiconductors had crossed from industrial component to primary driver of global value creation.

The chips that power artificial intelligence, electrified transport, advanced manufacturing, and modern defence are now no longer background infrastructure. They are the asset class that nations, corporations, and investors are now competing to control.

Purpose-built Application Specific Integrated Circuits (ASICs) are designed and customised for a very specific, singular task, such as managing power in electric vehicles or directing data traffic in high frequency communications infrastructure. Neural Processing Units (NPUs) run AI at the edge on smartphones.

Central Processing Units (CPUs) and Graphics Processing Units (GPUs) sit at the heart of hyperscale data centres training Large Language Models (LLMs). Demand is ubiquitous, and the global semiconductor market is projected to reach $1 trillion by 2030 [2].

This shift is visible across every major industrial vertical and access to advanced chips has consequently become a matter of economic resilience and national security for every developed economy.

EUROPE'S LEGACY AND CURRENT PARADOX

Europe holds an interesting position in the value chain. The Netherlands-based ASML is the world's sole provider of Extreme Ultraviolet (EUV) lithography machines, the equipment without which no leading-edge chip can be manufactured.

In some respects, Europe holds structural chokepoints in the global supply chain, and benefits from decades of accumulated intellectual property.

Yet in some of the most critical or rapidly expanding segments, Europe holds only peripheral positions. In fact, Europe's manufacturing footprint accounts for approximately ~10% of global semiconductor production, down significantly from prior decades, and that production is concentrated almost entirely in mature nodes above 22nm, serving automotive and industrial markets [3].

Europe has no domestic capacity to manufacture the leading-edge logic chips based on nodes smaller than 7nm. This strategic market is dominated by Taiwan with TSMC, as well as South Korea with Samsung, and the US with Intel, and is increasingly dependent on American IP at every stage of the chip design.

The European Chips Act has identified this gap, targeting a doubling of Europe's global market share to 20% by 2030 [3]. The target is ambitious and increasingly contested.

Industry stakeholders are questioning the execution, pointing to a funding framework that is fragmented across national and EU programmes, an approval process too slow for the pace of technological change, and a supply-side focus that does not always align with where European demand actually sits [4].

Replicating East Asian volume fabrication at speed is a capital-intensive race that Europe entered late. Taiwan and South Korea built their structural advantages over decades and will not be easily displaced.

Chips Act 2.0, the second iteration of this strategy proposed by the European Commission in June 2026, represents an acknowledgement of that constraint, introducing demand-side measures alongside supply-side investment for the first time [5].

OPPORTUNITIES BEYOND MOORE'S LAW

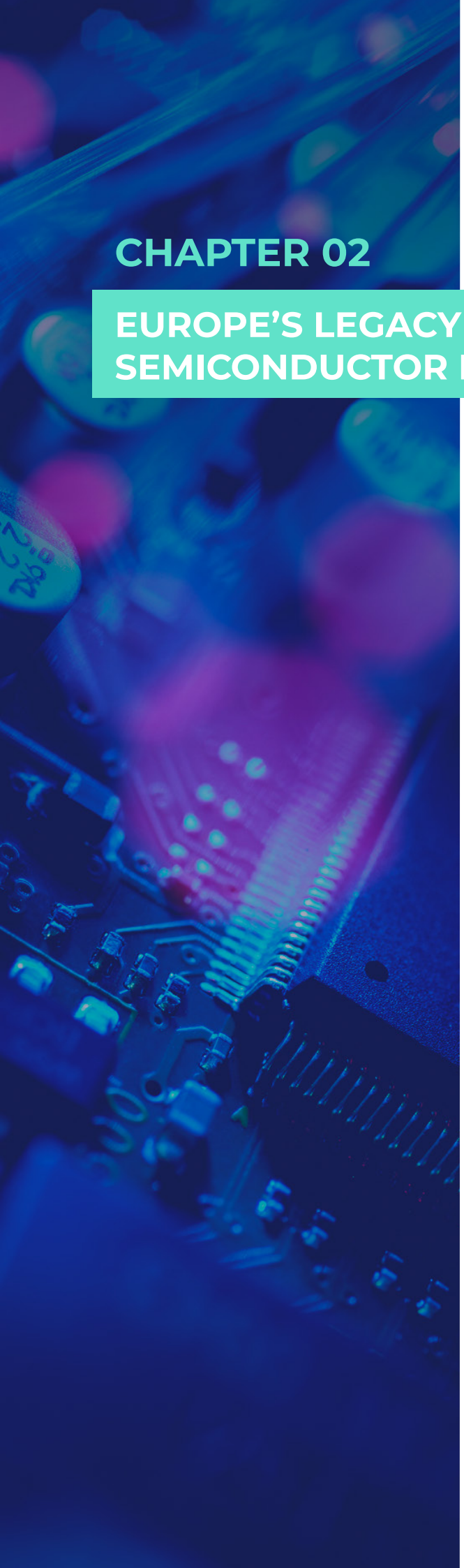
A more tractable opportunity lies in the shift that is already reshaping the industry from within. For decades, semiconductor performance advanced through a single mechanism referred to as Moore's Law, the observation that transistor density doubles roughly every two years.

By 2025, that cadence has slowed. Shrinking transistors further is becoming economically prohibitive. Furthermore, at atomic scales, the benefits miniaturisation deliver are increasingly undermined by quantum effects, heat dissipation, and signal leakage [6].

The industry's response is to pursue performance through new materials, novel architectures, and advanced integration techniques rather than simply making things smaller. This is the More than Moore paradigm.

For Europe, this is a genuine strategic opening. The continent already holds credible foundations in the domains where More than Moore performance gains are being pursued, such as in compound semiconductors, integrated photonics, heterogeneous packaging, neuromorphic computing, and quantum devices.

These are areas where global competitive positions are still being established, where Europe's research institutions are world-class, and where a generation of deep tech startups is already building. The question is how Europe can convert that scientific foundation into industrial scale.



CHAPTER 02

EUROPE'S LEGACY POSITION IN THE SEMICONDUCTOR LANDSCAPE

- → Europe's strongest position by far is its global monopoly on EUV lithography and precision optics, sitting in the enabling layer. However, it faces strategic vulnerabilities due to its reliance on foreign compound materials and design software, as well as its near-total outsourcing of back-end packaging and testing.

- → The continent's manufacturing base is firmly established in well-developed, mature sectors serving the automotive and industrial markets, rather than in the AI accelerators and custom silicon that are driving the industry's fastest growth.

- → The continent's most defensible path is to strengthen its capabilities in key domains where it already has a strong research base, such as compound semiconductors, integrated photonics, heterogeneous packaging, neuromorphic computing, and quantum devices.

Examining Europe's standing in the semiconductor value chain reveals how its leverage is concentrated at the enabling layers where equipment and materials make semiconductor manufacturing possible.

Its Integrated Device Manufacturers (IDMs) hold sturdy positions in the markets they serve. But across design software, leading-edge logic, packaging, and the compound materials central to its own strategic ambitions, Europe is a net importer of capability.

Policy has been structured to address some of these domestic gaps, but there could be a stronger case for reinforcing the positions Europe already holds and prioritising the domains where no geography has yet established dominance, rather than entering races where structural leads are measured in decades.

The semiconductor value chain is deeply segmented, globally distributed, and can be broken down into sequential stages comprising of distinct technological and process elements that define where innovation occurs and where dependencies lie.

Figure 1 represents these stages from the bottom up, where end markets are represented as the major drivers of chip production. Europe's place within this value chain provides a clear picture of potential leverage points and critical dependencies.



Figure 1. The global semiconductor value chain and major end-use markets. Key legacy companies are presented in their respective sub-section.

PREREQUISITES

Raw materials

Chips are fabricated from a set of physical inputs, including silicon wafers, specialty gases, and process chemicals. In conventional substrate and process materials, Europe holds a respectable position.

Siltronic ranks among the top five global silicon wafer producers. Soitec leads in engineered silicon-on-insulator substrates, which are critical for Radio Frequency (RF) and power applications. Merck KGaA supplies photoresists and high-purity process chemicals.

Air Liquide and Linde are major providers of the specialty gases used throughout the fabrication sequence. This anchors European companies in the supply chains of virtually every leading-edge fab, providing robust leverage in the materials that underpin conventional silicon manufacturing.

However, a more exposed picture lies upstream in compound semiconductor materials. China controls approximately 98% of global gallium supply, around 60% of germanium, and roughly 70% of silicon carbide feedstock [7].

These are not legacy industrial inputs. Gallium nitride and silicon carbide are critical substrate materials for the power electronics, RF devices, and wide-bandgap semiconductors that sit at the centre of a More than Moore strategy.

China demonstrated its willingness to use this position as a policy instrument when it imposed export controls on gallium and germanium in 2023 [8]. For Europe, this is the raw materials dependency that carries the highest strategic risk, precisely because it is most acute in the domains where Europe excels and can viably build.

Equipment

Today, Europe's strongest position in the entire semiconductor value chain lies in the machinery used to manufacture chips. Indeed, ASML holds the global monopoly on EUV lithography machines, a structural chokepoint Europe holds nowhere else in the chain. Zeiss, which supplies the precision optics for that machinery, is among the critical names underpinning it.

Oxford Instruments and ASM International add further European presence in Atomic Layer Deposition (ALD) and epitaxy systems, critical for atomic-scale film deposition at advanced nodes. The concentration of this strength in a small number of companies is worth noting, but the nature of the leverage is substantial.

Electronic Design Automation (EDA)

Electronic Design Automation tools do for chip design what CAD software does for architecture, allowing engineers to design, simulate, and verify complex circuits before they are physically built. These tools are tightly coupled to the foundry ecosystem because each process node (e.g., TSMC's N3 or Intel's 18A) requires certified design flows co-developed between the EDA vendor and the foundry [9,10].

Europe expresses a near-total dependence on the American EDA software, which is a structural chokepoint. Synopsys and Cadence Design Systems together dominate the global EDA market, with Siemens EDA the only European-owned player of note but not at comparable scale.

This entrenchment is reinforced by decades of accumulated IP, deep foundry co-development relationships, and high switching costs, meaning there is likely no credible near-term European alternative.

IDEATION

Intellectual Property

In the semiconductor domain, IP often refers to the reusable processor architectures and circuit blocks that chip designers license and incorporate into their own designs rather than engineer from scratch. The UK's Arm processor architecture has been historically the backbone of most smartphones produced globally, and is now expanding into data centres, automotive, and IoT at pace.

However, the company's acquisition by the Japanese SoftBank in 2016 [11] raised questions on whether the enterprise can still be considered European asset, and whether the company's direction, its licensing terms, and roadmap priorities remain shaped by European interests. For now, Europe's most valuable IP position is one it does not own.

In the meantime, RISC-V, the open-source instruction set architecture that allows processor design without proprietary licence fees, offers a genuine sovereignty alternative and is gaining meaningful traction in embedded and IoT applications. Europe has invested accordingly, with roughly €270 million directed at RISC-V chip development [12].

Nonetheless, Arm's ecosystem advantage in high-performance computing is deep and will not be displaced on a short time horizon.

Chip Design

Chip design is a domain where Europe has no presence among the global elite. Typically carried out by "fabless" companies (those that don't own fabrication facilities), this process involves architecting a chip's logic and functionality.

The leading fabless chip designers produce forefront compute architectures on the latest nodes, while Europe, with no presence amongst them, does output significant chip design activity in automotive, industrial, medical, and power management applications, mostly at more mature nodes [13].

These are durable markets with strategic relevance, but they are also lower-margin, slower-growth segments where the dominant players are incumbent IDMs, not startups.

The segments generating the highest semiconductor revenue growth in 2026 are AI accelerators, custom silicon for hyperscalers, and high-bandwidth networking chips, which are all almost entirely American and Taiwanese domains [14].

In fact, according to a more recent study by ZVEI, demand for GPUs and CPUs will increase to seven times the level of 2025 by 2040, with memory increasing to three times [15]. Europe is not designing for these markets, despite most capital and talent currently flowing into this space.

MANUFACTURING

FEOL & BEOL

Front-end and back-end-of-line manufacturing (FEOL & BEOL) involves building transistors into the silicon wafer and connecting them with layers of metal wiring to create functional circuits.

This is where the industry's most capital-intensive competition occurs.

As of 2026, Europe has no leading-edge logic capacity and, on any realistic near-term trajectory, is unlikely to build it. TSMC, Samsung, and Intel are the only vendors manufacturing at the nodes below 7nm, and their structural advantages in process expertise, supplier ecosystems, and accumulated yield knowledge represent decades of compounding investment that cannot be replicated quickly or cheaply.

The most significant near-term addition to European manufacturing capacity is ESMC, a joint venture between TSMC, Bosch, Infineon, and NXP located in Dresden, due to begin production at 12nm from approximately 2027 [16]. Although ESMC is a meaningful expansion of continental capacity, it is still a mature node facility, and its foundry expertise is anchored in Taiwan rather than developed domestically.

Essentially, Europe's manufacturing base sits entirely in IDMs operating at these mature nodes, typically 22nm and above, producing the power management, automotive, and industrial chips that its existing corporate base demands.

These are not negligible markets, and Infineon, STMicroelectronics, NXP, Bosch, and X-FAB hold strong positions within them. Yet mature node IDM capacity does not meet the needs of the types of silicon architecture driving the industry's fastest growing segments.

The European Chips Act 2030 manufacturing targets address the segment where Europe's hand is weakest but may struggle to materialise against rivals who have been operational for decades.

OSAT

Assembly & Packaging

Europe has almost no presence in semiconductor assembly and packaging at commercial scale, i.e., the post-fabrication work of cutting dies from a wafer, encasing them, and preparing them for integration into devices. In fact, the US-headquartered Amkor is the only high-volume Tier 1 OSAT operating on the continent.

Historically this was treated as a back-end commodity step, and Europe's decision to outsource it entirely to Asia was the rational at the time.

Today, however, advanced packaging, encompassing flip-chip bonding, fan-out wafer-level packaging, stacking, has moved from a finishing step to a primary performance lever.

As transistor scaling slows, how dies are integrated and interconnected is increasingly where system performance is bolstered. Chiplet architectures, which allow heterogeneous dies from different process nodes or materials to be combined in a single package, depend entirely on packaging sophistication. Europe's near-total outsourcing of this capability is therefore a growing vulnerability amongst the many domains where Europe lags.

Testing

The final verification stage before a chip ships covers both wafer-level probe testing to identify defective dies before packaging, and final test after packaging to validate the complete device under operating conditions. Both functions are served by specialist equipment manufacturers and by contract test houses providing outsourced testing services.

The equipment market is dominated by Advantest in Japan and Teradyne in the US, with Cohu serving analogue and mixed-signal segments, while testing services are mostly concentrated in Asia.

Europe has no meaningful presence in either. Of all the back-end gaps covered, this is the least strategically acute since testing is globally competitive and not easily weaponised. Even so, the lack of European players in this field completes the picture of a continent that has systematically outsourced the entire back end of the value chain.

The value chain analysis makes clear why meeting the European Chips Act's manufacturing targets is an extremely difficult proposition.

The dominant players in leading-edge logic and assembly have built their structural advantages over decades securing the capital, process expertise, and supplier relationships involved, which are not replicable through policy ambition alone.

The more productive question is where Europe can build positions that are genuinely defensible. The evidence points to the segments where the continent already holds research depth and where global competitive positions are still being established.

These are the technologies that deliver performance through means other than transistor scaling and that are based on fundamentally disruptive innovations. Examples include compound semiconductors, integrated photonics, heterogeneous packaging, neuromorphic computing, and quantum devices.

Several of these domains are approaching industrial maturity, and European research excellence within them gives the continent a credible position in each.



CHAPTER 03

PROFILING EUROPE'S INNOVATION PIPELINE

- Europe accounts for around a quarter of the world's semiconductor startups, yet it attracts only 7% of global funding. Furthermore, the continent's startup-to-scaleup conversion rate is critically low, with only 6% reaching the post-Series A scaleup phase compared to 24% in the US and 37% in China.

- Europe's hubs of excellence are geographically concentrated, but this strength is specialised rather than integrated, lacking the full-stack density that lets Silicon Valley or Shenzhen convert research into champions.

- Innovation is heavily concentrated in specialised fields, such as quantum devices, photonics & optoelectronics, and advanced sensors. European startups disproportionately target the telecommunications, medical, and defence sectors, while automotive, one of its most well-established sectors, is underserved by new ventures.

- The European pipeline stalls at the transition from laboratory to commercial scale, with 78% of projects stuck at TRL 1–5 compared to 54% in the US and 24% in China.

Europe accounts for roughly a quarter of the world's semiconductor startups identified in the dataset underpinning this report, a figure that sits comfortably alongside the US and ahead of most other tracked regions. However, it is worth noting that comparison likely understates ecosystems like China's, where state-funded ventures are less publicly disclosed.

In practice, this volume of European semiconductor startups rarely converts into durable competitiveness since the continent captures only a fraction of the funding its peers attract, converts few of those startups into scaleups, and exits many of its most promising companies to non-European acquirers.

Mapping where Europe's technology bets are concentrated, evaluating whether early promise turns into commercial scale, and examining the structural forces behind that gap reveals an uneven picture.

WHAT EUROPE'S STARTUPS ARE BUILDING

All three major geographies express a similar split with the ideation segment of the value chain dominating startup positioning: 68% of European, 73% of American, and 66% of Chinese semiconductor startups concentrate in chip design and IP. This is to be expected as fabless design offers significantly lower entry barriers, requiring orders of magnitude less capital investment than manufacturing.

Figure 2 maps startup counts across all value chain sub-segments for the three major geographies, which reveals distinct specialisation patterns that reflect each ecosystem's broader industrial structure. All three regions cluster roughly half their startups in chip design. The divergences appear below that where Europe's most distinctive feature is a disproportionate concentration in manufacturing, likely reflecting the volume of spinouts from Europe's process-development research institutions.

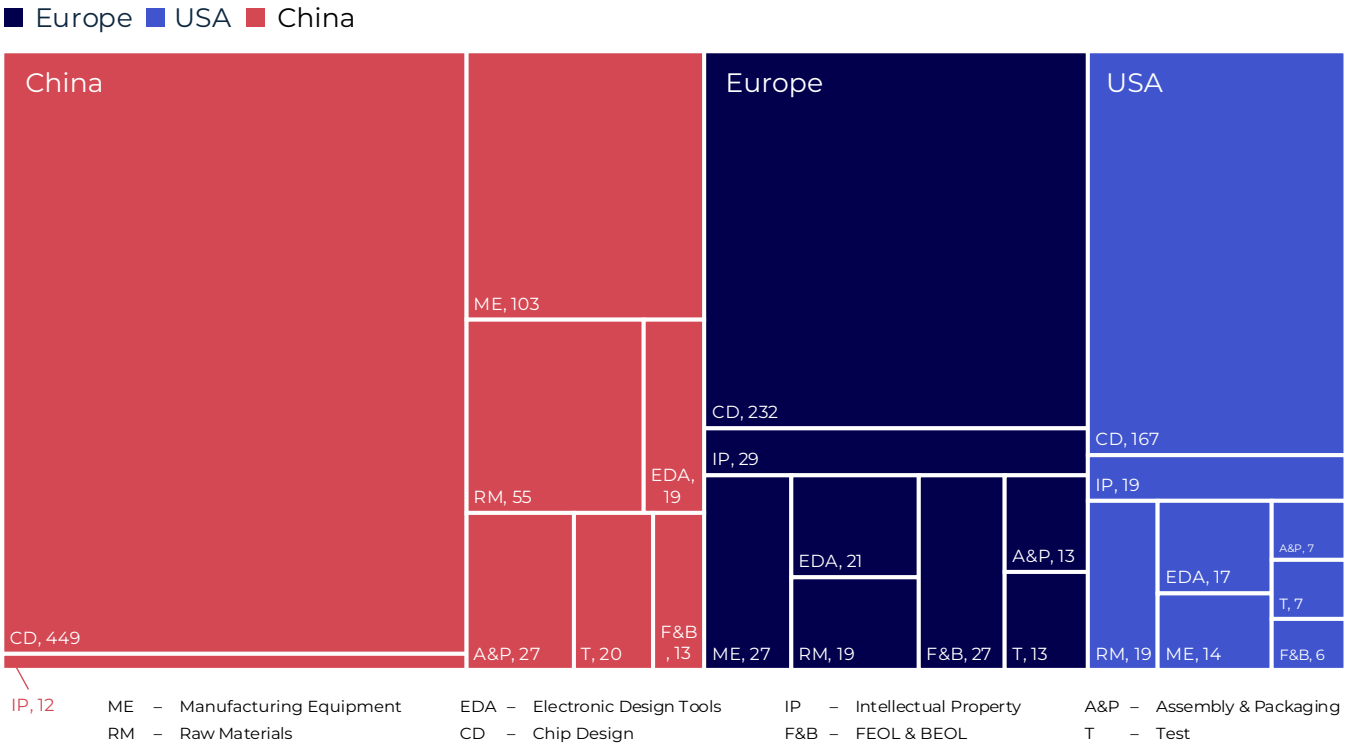


Figure 2. Europe, the USA & China's share of global startups by value chain sub-segment.
Source: Hello Tomorrow analysis based on data from Dealroom, Crunchbase, and Hello Tomorrow proprietary database.

China's differentiator is more pronounced with disproportionate concentrations in manufacturing equipment, raw materials, assembly and packaging, and testing, consistent with an ecosystem deliberately built across the broader manufacturing stack.

The US distribution is the flattest of the three, which likely understates true American activity. US startups transition to scaleups or are acquired more quickly than their counterparts elsewhere, a dynamic explored further below, pulling a significant share of activity out of the database before capture. Further insight comes from the composition of each region's startup profile through investigating what they are designing and to what purpose.

Figure 3 shows the proportion of each geography's startups that list a given end market as a target, where individual startups can appear across multiple categories. It is worth noting that Defence & Aerospace industry illustrates the limits of the available data: for instance, only 3% of Chinese startups in the database are tagged to the category, which almost certainly reflects China's opacity around defence-oriented ventures rather than the sector's true scale.

It is likely that similar dynamics apply, to a lesser extent, in other geographies where state-linked defence activity is not publicly disclosed. More interestingly, a profile is revealed of each geography that well reflects their respective incumbent markets. Large fractions of China's startup base target consumer electronics (30%), automotive innovations (36%), and industrial components (39%), mirroring China's current and target capabilities in those segments.

By a large margin, the US is hyper-focused on compute capabilities (45%), the largest standout share of all markets in all geographies and clearly resulting from the last few decades of development in cloud data storage, compute-as-a-service, and as of the late 2010s and early 2020s, AI infrastructure driven by domestic hyper-scalers.

The US and China's profiles resemble each other's structures, along with most other geographies in the dataset, yet Europe stands apart. Europe's telecom and communications infrastructure (21%), medical technology (13%), and defence technology (18%) sectors are proportionally more addressed than its automotive counterpart (13%).

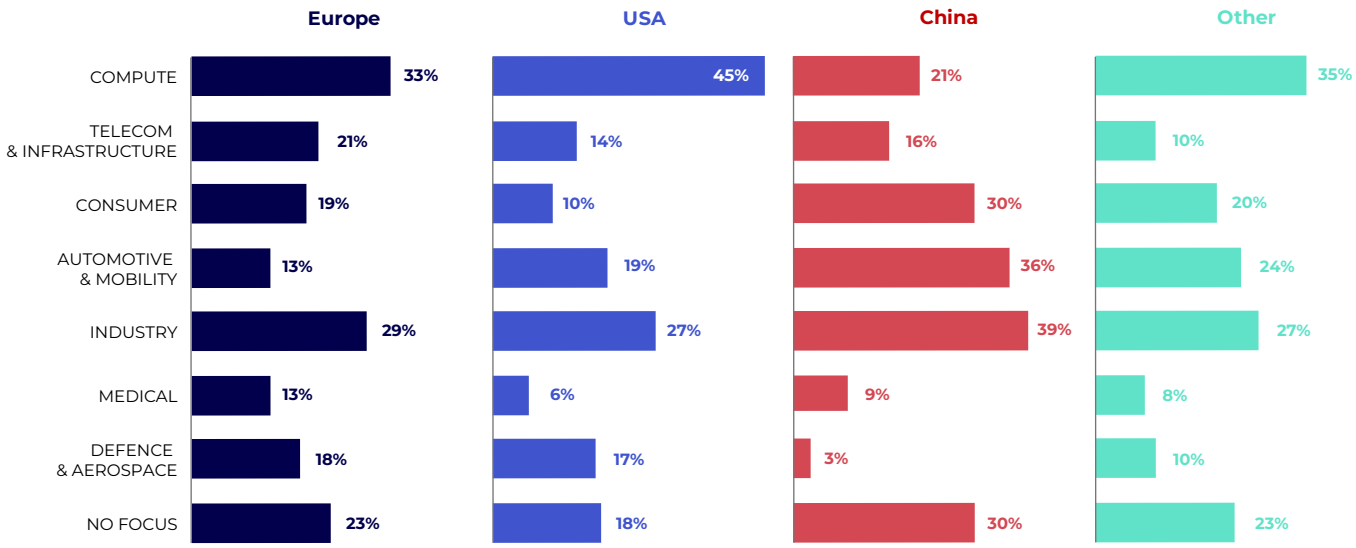


Figure 3. Distribution of markets targeted by a geography's semiconductir startups.
Source: Hello Tomorrow analysis based on data from Dealroom, Crunchbase, and Hello Tomorrow proprietary database.

Startup focus often follows industry pull, yet in Europe's case, one of its most well-established sectors is underserved. This is partly reflective of a shift in European R&D priorities, given the continent's public sector is heavily involved in funding grants [4].

Horizon Europe and the European Innovation Council's (EIC) have directed substantial funding toward quantum, photonics, and defence-adjacent technologies, while post-2022 defence budgets across member states have grown considerably [17,18].

On the automotive side, the EV transition has introduced uncertainty about which semiconductor architectures will dominate, making it aharder market for startups to commit to, and one where Europe's established IDMs already fill much of the existing demand. Beyond public funding priorities, Europe's overrepresentation in Telecom, Medical, and Defence also reflects where its startups originate. Research institution and university spinouts working in quantum, photonics, and RF naturally orient toward these sectors as their first customer base.

For example, a quantum sensing startup finds its earliest revenue in defence and metrology; a photonics company finds it in data centre interconnects and medical imaging. Essentially, Europe's research-led formation model shapes what its startups build and which markets they enter first. Understanding where Europe's startups concentrate by technology domain adds a second layer to this picture, revealing the capabilities the ecosystem is accumulating.

EUROPEAN HUBS OF EXCELLENCE

Europe's strengths are specialised rather than integrated. Certain technological disciplines stand out as areas of focus for Europe and concentrate within specific geographies.

Cambridge and the Nordic cluster excel in quantum hardware. Grenoble and Eindhoven drive photonics. Silicon Saxony holds the continent's manufacturing depth. This specialisation is a structural feature that, although cultivates innovation, does not carry the full-stack density of a Silicon Valley or Shenzhen, where chip design, manufacturing, packaging, and systems integration coexist within close proximity.

Figure 4 illustrates Europe's share of global semiconductor startups in specific technology domains, comparing these shares to a 25% average. Quantum devices (48%), sensors & actuators (38%), and photonics & optoelectronics (32%) are standout technology domains that merit examination, with simulation & design (33%) above the baseline but less instructive, as software-based tooling carries lower barriers to startup formation and the commercial market is already mature.

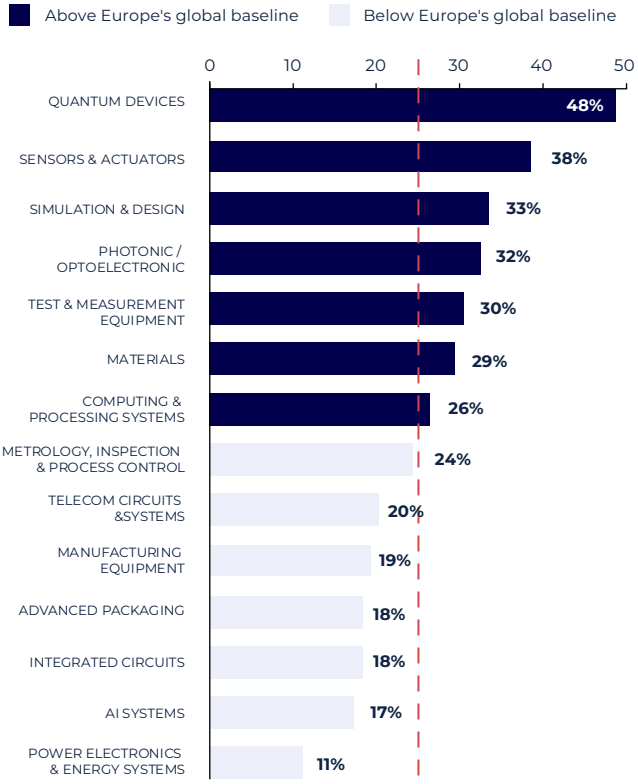


Figure 4. Europe's share of global semiconductor startups by technology domain.The dashed line marks Europe's overall global share across all semiconductor domains (25%).
Source: Hello Tomorrow analysis based on data from Dealroom, Crunchbase, and Hello Tomorrow proprietary database.

Quantum devices

Europe's heavy position in quantum technologies reflects decades of publicly funded research at institutions including Cambridge, Oxford, TU Delft, and ETH Zurich, seemingly beginning to produce commercially credible companies. IQM (Deep Tech Pioneer – 2019)1 in Finland, which builds custom superconducting quantum systems for research laboratories, became the first listed European quantum company in 2026 [19]. Pasqal (Deep Tech Pioneer – 2019) in France, developing neutral atom quantum processors, received a €30 million EIC STEP Scale Up award in 2025 alongside IQM; both have since reached valuations of $2 billion and $1.8 billion respectively in 2026 [20–22].

Quantinuum, co-headquartered in the UK and the US, went public on the Nasdaq in June 2026 at a valuation of approximately $17.6 billion, leveraging a hybrid approach combining its parent companies' trapped-ion quantum hardware on Honeywell's side and Cambridge Quantum's software expertise [23].

Riverlane, also UK-based, and Alice & Bob (Deep Tech Pioneer – 2019) in France, are similarly targeting qubit error correction at scale. In quantum networking, WeLinQ (Deep Tech Pioneer – 2022), a French spin-out from the CNRS, is networking multiple quantum processors into larger entangled clusters for quantum scale-out.

Other startups of note are SemiQon in Finland, developing cryo-optimised silicon quantum chips using CMOS processes, Quantcore, a University of Glasgow spinout in the UK, producing niobium-based superconducting components that require less cooling than conventional alternatives, and QuiX Quantum in the Netherlands, who in 2026 delivered on a €15 million deal to provide the German Aerospace Centre with fault-tolerant photonic quantum computing racks [24–26].

As some of these companies begin to scale, a particular vulnerability is introduced across the hub in that most of them remain pre-revenue and dependent on grant funding, as is the nature of the quantum computing sector today.

Sensors & actuators

Europe's sensor and actuator startup portfolio is its closest position to near-term revenue as it benefits directly from proximity to Infineon, Bosch, and STMicroelectronics, which function simultaneously as customers, co-development partners, and natural acquirers for emerging companies.

Innatera (Deep Tech Pioneer 2024), a Netherlands-based startup developing neuromorphic spiking neural processors for sensor-edge applications, is scheduled to feature inside consumer-grade smart home and wearable devices in 2026 [27].

Paragraf, a Cambridge University spinout from the UK and the first company to mass-produce graphene-based electronic devices using standard semiconductor processes, develops graphene Hall Effect sensors already deployed across automotive, aerospace, and quantum computing applications, and raised over €120 million across three rounds, as of late 2025 [28]. QuantumDiamonds (Deep Tech Pioneer – 2022), a TUM spin-out in Germany developing diamond-based quantum sensors, secured a €76 million grant in June of 2026 to aid in setting up a quantum chip inspection facility in Germany [29].

Europe's sensor hub is also where the overlap between semiconductor hardware and application markets is tightest as startups benefit from a credible route to revenue through Europe's automotive & industry IDMs.

1. A Deep Tech Pioneer is a designation given to early-stage startups that have applied to the Hello Tomorrow Challenge and have been officially recognised as the most promising science- and technology-driven ventures.

Photonics & optoelectronics

Europe's position in photonics is similarly grounded in decades of public research investment. CEA-Leti in Grenoble, imec in Leuven, and Fraunhofer institutes across Germany have sustained world-class integrated photonics programmes that have generated a steady pipeline of spinouts. The continent's central role in building the optical telecommunications infrastructure of the 1990s also left a lasting base of component expertise that newer startups have been able to draw on.

In photonics, Scintil Photonics, a French fabless startup that emerged from the CEA-Leti research ecosystem, closed a $58 million Series B in 2025 with participation from NVIDIA [30]. iPronics in Spain, developing software-defined photonic engines for AI data centres, raised a €20 million Series A in 2025 backed by Bosch Ventures [31].

Q.ANT in Germany closed a round of more than €80 million in late 2025, the largest photonics funding round in Europe to date, building on its Thin-Film Lithium Niobate platform for photonic computing [32]. Akhetonics, another German startup developing an all-optical general-purpose processor to process and store data, targeting AI and HPC applications, raised €6 million in seed funding in late 2024 [33].

Other companies pushing the sector forwards include Lumai and Olix in the UK, the former commercialising hybrid optoelectronic AI inference servers and the latter building Optical Tensor ProcessingUnits (OTPUs) that bypasses High-Bandwidth Memory (HBM) through photonics to deliver inference workloads, EFFECT Photonics in the Netherlands, focusing on indium phosphide photonic integration, and Pixel Photonics (Deep Tech Pioneer – 2024) in Germany, developing single-photon detection components relevant to both quantum and classical sensing.

As photonics moves from data transfer to in-light compute, new market use cases are emerging that could, if adopted, promise substantial growth of the sector where Europe is well positioned. Some of the other figures are surprising given the continents research expertise and IDM base. Power electronics & energy systems, for example, is curiously underrepresented by European share, and despite a below-average 17% in AI Systems, the continent does produce important startups.

Axelera AI (Deep Tech Pioneer – 2022) in the Netherlands, Fractile in the UK, and SpiNNcloud in Germany are each building competitive positions in AI inference and neuromorphic processing, approaching the problem from architectures that diverge from the GPU-centric model dominant in the US. What further distinguishes Europe's approach, as much as its technology, is where these companies emerge from.

Figure 5 highlights Europe's principal semiconductor corridors and some of the exceptional startups emerging from them.

UNITED KINGDOM

Europe's deepest quantum computing cluster,anchored by the Cambridge-Oxford corridor, with secondary strength in photonics and RF chip design.

Salience Labs · PICOCOM · Oriole · OLIX · ALPHAWAVE SEMI · ACCELERCOMM · FOREFRONTRF · SPACE FORGE · Flexciton · PHLUX · OQC · QUANTUM MOTION · QUANTINUUM · CGD · BintangChip

FRANCE

CEA-Leti in Grenible drives a focused pipeline in photonics, power semiconductors, and quantum, with strong research-to-spinout infrastructure.

Wise integration · SCINTIL PHOTONICS · SIPEARL · Aniah · ALICE & BOB · Hprobe MYCRONIC · ZADIENT

SWITZERLAND

ETH Zurich and EPFL generate technically ambitious spinouts across photonics, quantum-secure semiconductors, and precision sensing, though the commercial ecosystem remains modest in scale.

AlpsenTek · NovaViz · SEALSQ · DEEPLIGHT · spacetek · LXT



Startup Technology Domains

- Circuits and Systems
- Design, Simulation and Verification
- Devices
- Equipment
- Fabrication and Processing
- Materials
- Packaging, Assembly and Testing

NETHERLANDS

A dense cluster in quantum hardware and AI inference chips, underpinned by TU Delft and the Brainport Eindhoven ecosystem.

SEMI BLOCKS · AXELERA · QUANTWARE · QUIX QUANTUM · SEMIQURE · innatera · DELTA LIFE SCIENCE · NEARFIELD INSTRUMENTS · QBLOX · Delft Circuits

GERMANY

Silicon Saxony anchors Europe's largest fab cluster, with Fraunhofer-backed startups pushing into photonics, advanced materials and MEMS.

FMC · OQMENTED · QANT · SCANTINEL · ARIOSO SYSTEMS · Lidrotec · kiutra · black semiconductor

BELGIUM

Almost entirely anchored by imec in Leuven, with output concentrated in photonics and sensing.

spectricity · swave · MICLEDI MICRODISPLAYS

THE NORDICS

Collectively small but technically focused ecosystems, spanning quantum computing, GaN RF, mmWave communications, and advanced nanofabrication, underpinned by strong public research institutions including VTT and DTU.

BeammWave · MINIMA · ZeroPoint · comptek solutions · Devil · ATLANT 3D · IQM · ALIXLABS

Figure 5. Map of major European semiconductor corridors and local startups. Startup logos are colour coded to their technology domain.
Source: Hello Tomorrow analysis based on data from Dealroom, Crunchbase, and Hello Tomorrow proprietary database.

WHERE EUROPE'S PIPELINE STALLS

Europe may be producing startups at substantial scale, but the problem lies in conversion and an overall failure to realise startup potential in a commercial context. The primary causes are a structural shortage of growth-stage capital and an underdeveloped corporate demand layer.

Figures 6 and 7 show a profile of Europe where the continent holds 25% of global semiconductor startups but attracts roughly 7% of total funding, converts just 6% into post-Series A scaleups, and at the per-startup level, raise a median of $6.6 million over their lifetime, falling well short of the $16 million and $25.2 million that American and Chinese startups raise, respectively.

Europe's 6% post-Series A scaleup rate contrasts sharply with China's 37% and the US's 24% rates. Such stark difference is likely due to structural demand advantages through state-directed capital and procurement in China's case and hyperscale anchor customers in the US.

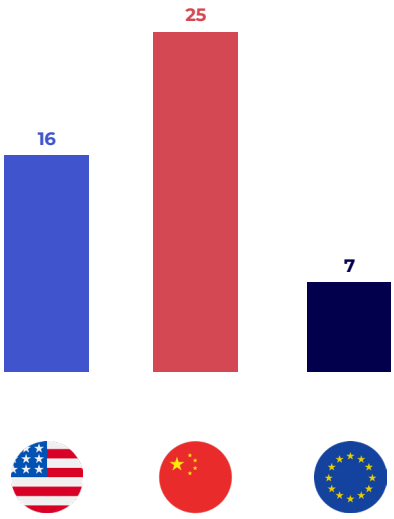


Figure 6. Median lifetime funding per startup ($M).

Source: Hello Tomorrow analysis based on data from Dealroom, Crunchbase, and Hello Tomorrow proprietary database.

Startups Distribution by Region		Scaleup Rate (Post Series A%)	Total Funding ($B)
CHINA	45%	37%	$ 56.1
EUROPE	25%	6%	$ 7.9
USA	17%	24%	$ 22.6
SOUTH KOREA	3%	24%	$ 2.5
ISRAEL	3%	29%	$ 2.9
JAPAN	2%	40%	$ 9.3
REST OF WORLD	6%	10%	$ 5.6

Figure 7. Geographical, maturity and funding share of global semiconductor startups.
Source: Hello Tomorrow analysis based on data from Dealroom, Crunchbase, and Hello Tomorrow proprietary database.

Looking to other geographies, Israel's 29% startup to post-Series A scaleup rate, despite a much smaller base, reflects a combination of long-standing public co-investment through the Israel Innovation Authority absorbing early technical risk alongside private investors, a defence-to-commercial pipeline built through decades of military technology development, and privileged access to the US market [34,35].

Japan's 40% rate could result in significant part from coordinated public-private investment, evidenced by Rapidus, a state-backed consortium co-funded by major Japanese corporations [36].

Both models share a common logic where public capital absorbs technical risk at early stages, while an established demand channel provides the commercial validation that growth-stage capital requires. Today, Europe lacks an equivalent.

The Technology Readiness Level (TRL) framework offers a sharper view of where in that journey Europe's pipeline stalls.

TRL measures technology maturity on a defined scale: TRL 1–3 covers proof of concept, TRL 4–5 covers near-realistic laboratory conditions, TRL 6–7 covers prototype demonstration in operational conditions, and TRL 8–9 covers system qualification and proven deployment [37].

An analysis of startup TRL in **Figure 8** shows that 78% of European semiconductor startups sit roughly between TRL 1–5, still at conceptual, prototype, or laboratory-validation stage. The equivalent figures are 54% in the US and 24% in China.

This demonstrates how Europe's pipeline is heavily front-loaded, and the TRL 1–5 to TRL 5–7 transition is where the ecosystem most visibly stalls. Only 3% of European startups reach TRL 8–9, against 11% in the US and 13% in China.

The TRL concentration reflects the pull mechanism deficit identified above where without anchor customers or co-development commitments generating demand, startups remain in research-stage rather than being drawn toward industrial validation.

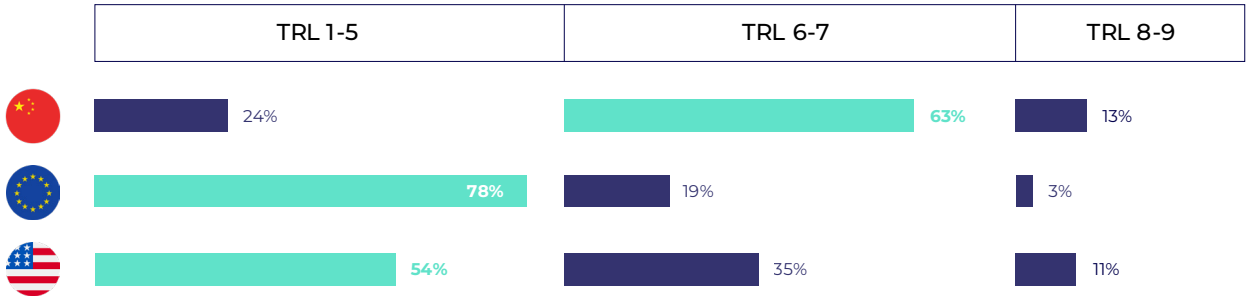


Figure 8. Semiconductor startup technical maturity distribution, by region.
Source: Hello Tomorrow analysis based on data from Dealroom, Crunchbase, and Hello Tomorrow proprietary database.

EUROPE'S CAPITAL GAP

Early-stage European startups raise a median of $3.2 million across a median of three funding rounds whereas Chinese startups at the same stage raise $13.8 million in a single round. Consequently, European founders are likely running repeated small rounds to assemble what a single transaction would deliver elsewhere, forcing them to consume management time and compress R&D focus at precisely the stage when technical progress is most critical. Therefore, the bottleneck is the absence of capital instruments sized for the transition from laboratory to industrial validation. Understanding why this bottleneck exists requires looking at who is funding European semiconductor startups and in what capacity.

Figure 9 shows that growth capital accounts for 10.8% of investor slots in European semiconductor startup rounds, against 16.1% in the US and 31.9% in China. The gap with China could result from a decade of deliberate state-directed capital deployment through vehicles that are structured as private funds but coordinated at the ecosystem level, such as their Government Guidance Funds (GGFs) [38].

Europe's gap with the US is more straightforwardly due to the continent's fewer number of large specialist funds, smaller ticket sizes, and a more fragmented limited partner (LP) base across 27 national markets. Furthermore, even where growth capital is present, individual round sizes remain smaller and deployment more incremental, which likely explains the underwhelming lifetime funding figures shown earlier.

A starker contrast between Europe and the other geographies is in university funding. University investors account for 9.7% of European investor slots against 1.7% in the US and 0.1% in China, the latter of the three cases being consistent with a model where Chinese university R&D projects are funded directly through municipal government bodies rather than the universities themselves [39]. Early-stage support adds a further 56.1%, which is consistent with the US (56.2%), and more substantial than China (48.1%) yet, as signalled earlier, is not complemented by later-stage growth capital.

The European corporate investment profile exacerbates the weaker back-end funding environment and could be the point at which momentum breaks down.

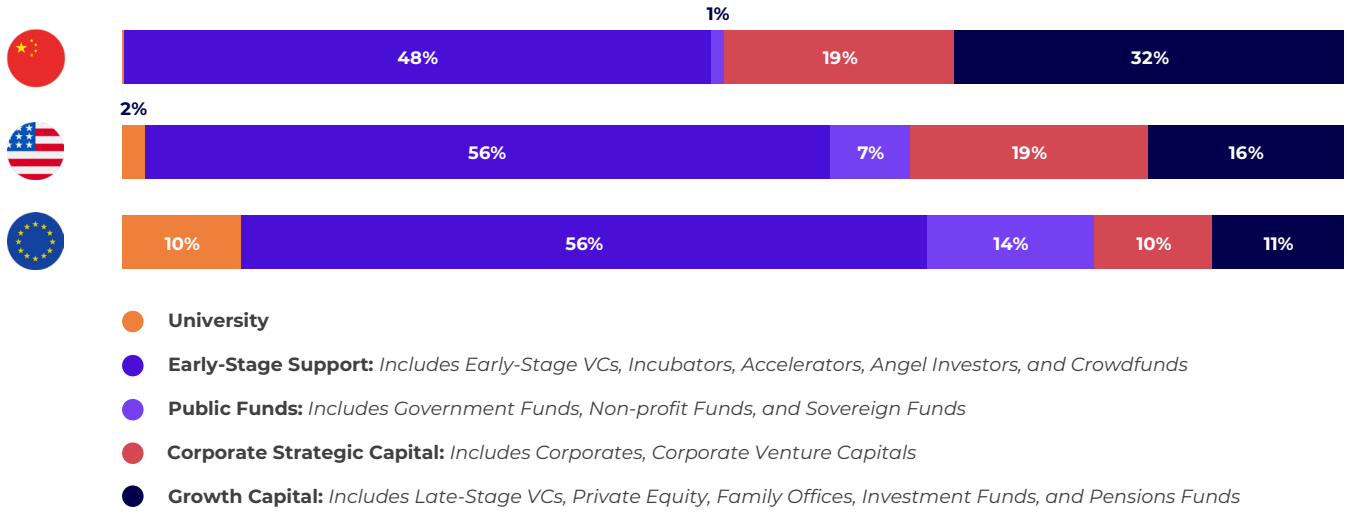


Figure 9. Investment profiles across the three major geographies.
Data represents the share of investor slots (participations), not unique investors or capital deployed; a single fund appearing in multiple rounds is counted multiple times. VC, PE, and similar vehicles invest from pre-seed through pre-IPO, therefore, grouping reflects motivation and legal structure rather than funding stage alone.
Source: Hello Tomorrow analysis based on data from Dealroom, Crunchbase, and Hello Tomorrow proprietary database.

At 9.7%, European corporate investment participation is roughly half that of the US (19.4%) and China (18.8%). With such little corporate engagement to bridge the gap, European startups arrive at Series B without the commercial validation that investors treat as a prerequisite and are thereby presenting to investors as a riskier venture [40]. This is likely due to corporate investors functioning simultaneously as backers and anchor customers, providing the revenue visibility that ultimately attracts growth capital.

In essence, the front end of the pipeline is well serviced, and capital is performing its intended function. The problem is that neither universities nor early-stage support vehicles are leading the growth rounds that semiconductor startups need to cross into scale. Europe has therefore built a well-resourced early-stage architecture that seems unequipped to support startups as they transition towards commercial maturity."

EUROPE'S DEMAND SIGNAL GAP

Illustrated in Figure 10, the three ecosystem models further suggest that the scaleup rate gap between Europe, the US, and

In the US, hyperscalers generate direct, commercially validated pull that de-risks capital at the growth stage. In China, state procurement functions as a first customer for technologies the private market has not yet adopted, while coordinated industrial policy ensures capital follows those technologies through the development cycle.

Europe's model, research-led and institutionally anchored, tends to produce a slower and more fragmented demand signal, one that sustains early-stage formation but struggles to accelerate the transition to commercial scale. The implication of this type of model would be that increasing early-stage capital alone is unlikely to close the gap. Europe's pipeline already has adequate resourcing at the front end.

What appears to be missing is the activation mechanism at the other end through anchor customers, corporate co-development partners, or procurement commitments, as shown by the Israeli or Japanese models, for example.

A question remains whether Europe's existing industrial base can play that role more deliberately.

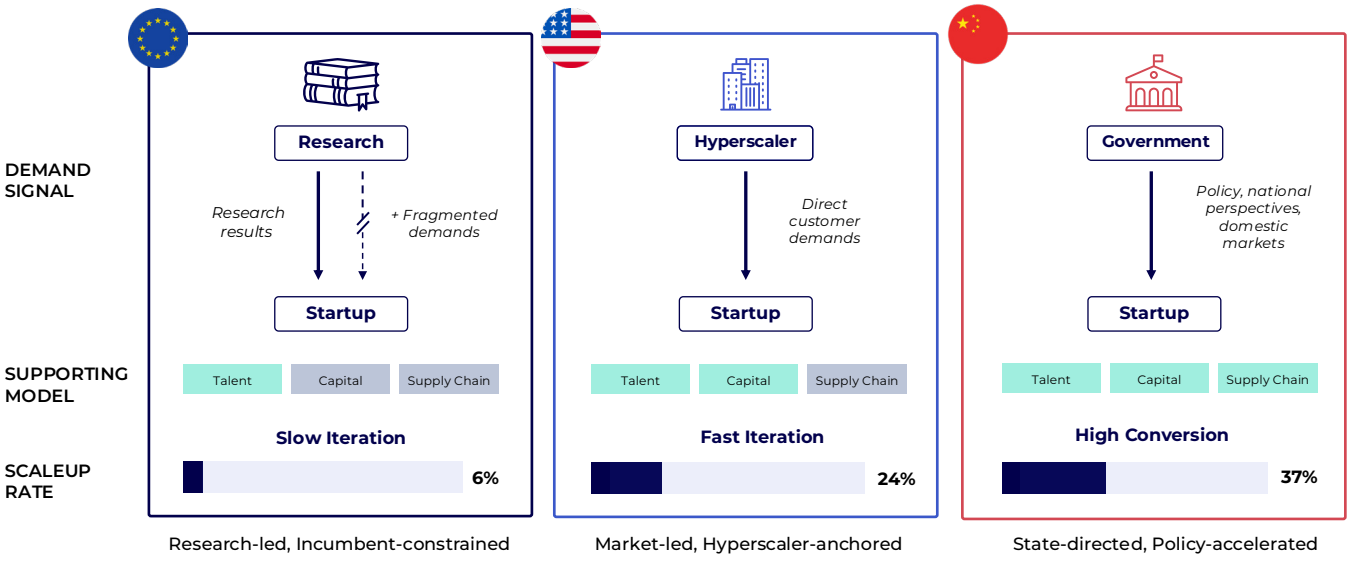


Figure 10. Structural dynamics across the three major geographies.
Source: Hello Tomorrow analysis based on data from Dealroom, Crunchbase, and Hello Tomorrow proprietary database.



CHAPTER 04

HOW EUROPE CAN BETTER SCALE ITS INNOVATIONS

- → Europe's pipeline fails at the transition from scientific credibility to commercial scale, held back by three reinforcing barriers: a shortage of growth-stage capital, a thin layer of large early customers, and exits that typically benefit non-European acquirers.

- → The binding constraint that is holding European startups from scaling is not a lack of early-stage money, but a lack of demand signal. The anchor customers and procurement commitments that pull startups across the valley of death.

- → Europe should pursue "smart sovereignty" by selectively exploiting its strengths, with corporate activation as the most actionable lever, rather than focusing on building where it lacks.

Europe's semiconductor startup pipeline fails at the transition between scientific credibility and commercial reality, finding the infrastructure to bridge this gap largely absent. There are three structural barriers that explain this absence:

- Funding velocity: European startups face a shortage of growth-stage capital, arriving at Series B without the funding velocity their US and Chinese counterparts take for granted.

- First customers: There is a demand gap, where the absence of hyperscale anchor customers means the revenue visibility that growth investors require simply does not materialise.

- Exit opportunities: When a startup does succeed and reach an exit, that exit typically benefits a non-European acquirer, removing a potential anchor company, a talent cluster, and a future customer from the continental ecosystem.

These three barriers reinforce each other: a startup without anchor customers is less likely to attract growth capital, yet without growth capital, it cannot reach the scale at which it becomes an acquisition target for a European buyer.

Yet forcing European startups to rely exclusively on European customers or acquirers would destroy the returns needed to sustain the ecosystem. This view held consistently across targeted conversations with investors and founders, carried out alongside the data analysis underpinning this report and quoted thereafter.

GAP 1: FUNDING VELOCITY

The problem European startups face is not whether capital exists, but how quickly it arrives. Sarah Luppino, Principal at Merck's corporate venture wing, M Ventures, describes it as a mathematical problem. Two identical startups launching simultaneously in Europe and the United States will look completely different two to four years later because their funding velocities diverge.

> "*Europe has improved at pre-seed and seed level. But there is a notable drop-off at Series B and C, much more pronounced than in the US. European startups end up looking to the US for growth capital anyway.*"
>
> – **Sarah Luppino, M Ventures**

Simon Thomas, CEO of the graphene-based electronic devices company Paragraf, illustrates this directly. Unable to close its Series B in the UK, it turned to the US and ultimately had its Series C led by a Middle Eastern investor.

The European market for Paragraf's technology was in question rather than the technology itself. The Scaleup Europe Fund, a multi-billion euro late-stage vehicle launched in 2025, is the most direct institutional response to date [41].

Lawrence Lundy, General Partner at the VC firm Cloudberry, adds that generalist capital previously locked in software is beginning to move toward hardware, including semiconductors, which should help close the gap over time. Sarah Luppino's assessment nonetheless remains the right note to close on: "*We're getting there, but we need more*."

GAP 2: FIRST CUSTOMERS

Capital follows customer visibility, and European semiconductor startups generally lack the customers large enough to generate it. Damien Bretegnier, Associate Partner specialising in semiconductors at Supernova, says that when evaluating a deal, the first question is whether the startup has access to real customers. In practice, "real customers" typically mean US or Taiwanese hyperscalers and advanced chip buyers, because confining a company to European buyers alone dramatically limits its commercial potential.

Sarah Luppino is equally direct: customer traction and hyperscaler network access are explicit investment criteria at Series A. Without them, the path to growth funding does not materialise. Vaire Computing (Deep Tech Pioneer – 2025), a Cambridge-based startup in the UK developing reversible computing architectures, has found its defining commercial constraint to be finding a first customer at the scale needed to validate a growth round.

Rodolfo Rosini, CEO and co-founder of Vaire Computing, explained how early adopters of advanced computing are mostly US-based, the same geography where Vaire Computing found most of its early-stage funding. The capital came from a newer generation of B2B-focused venture capital, less specialised in semiconductors than prior cohorts but drawn to hardware where enterprise customers, largely US-based, were already visible.

Damien Bretegnier observed that sensors, power electronics, photonics, and precision equipment have all shown stronger commercial trajectories, and that the common factor is established industrial customers already present on the continent. European IDMs and industrial groups in automotive, energy, and manufacturing generate the demand that pulls startups forward. The rest of the ecosystem largely lacks an equivalent.

GAP 3: EXIT OPPORTUNITIES

When European semiconductor startups reach an exit, the value typically leaves Europe with them. IonQ's $1.1 billion acquisition of Oxford Ionics (UK) in September 2025 is the most visible recent example [42]. A UK quantum computing company, built on European research, absorbed into a US corporate stack.

Sarah Luppino, Damien Bretegnier, and Lawrence Lundy all frame accepting non-European exits as a structural constraint rather than a correctable failure. Sarah Luppino notes that limiting startups to European acquirers would reduce exit values from above $1 billion to below $300 million, destroying the returns that make the asset class viable.

Damien Bretegnier goes further adding that restricting exits to European buyers would compress multiples, extend holding periods to seven to ten years or more in advanced semiconductors, and force investors to apply far stricter selection criteria when evaluating new opportunities. The practical effect would be a smaller, less ambitious European deep tech ecosystem.

The tension this creates is the critical point. Accepting non-European exits is rational at the individual transaction level and corrosive at the ecosystem level. The structural resolution is a domestic acquirer base capable of competing for these assets, built through more active corporate venture capital and patient capital instruments willing to hold through long hardware development cycles. Neither currently exists at meaningful scale, and until they do, European exits will continue to serve as the mechanism by which the ecosystem's best outcomes transfer elsewhere.

A STRATEGIC RESPONSE

The investor consensus across these conversations is deliberately pragmatic: Europe does not need to reconstruct what it lacks from scratch. The three gaps above are addressable through selective activation of what Europe already has, applied with greater deliberateness and over a longer time horizon than European policy has typically committed to.

Damien Bretegnier described it as "smart sovereignty": rather than attempting full domestic self-sufficiency, Europe should spend the next ten to fifteen years reinforcing the domains where it holds genuine advantage: quantum hardware, sensors, photonics, and wide-bandgap materials.

At the same time, the region should remain open to international capital, customers, and partnerships. The goal is reducing critical dependencies while remaining embedded in the global market.

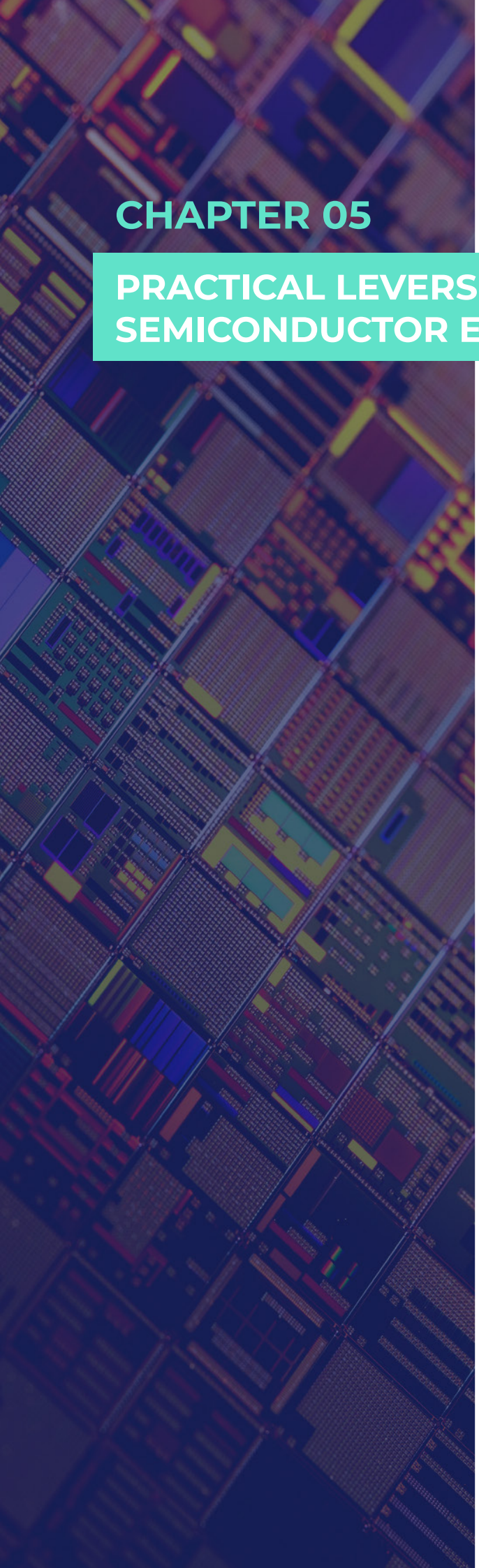
The most immediately deployable lever is corporate activation. Europe's industrial champions already have the procurement power, CVC infrastructure, and co-development relationships to function as anchor customers for early-stage startups.

Lawrence Lundy argues that the barrier to earlier engagement is less strategic than institutional: large organisations move slowly, and the startups that could accelerate them are often outside their field of view.

The example of SiPearl (France), a fabless producer of high-performance processors, demonstrates what deliberate early engagement can produce. The EIC and France 2030 funding unlocked industrial co-investment, therein pulling the startup through to scaleup territory [43].

The capital architecture takes longer to build but follows the same logic. At the pre-seed and seed stages, semiconductor hardware investments present binary risks: the hardware either works or it does not, with few intermediate outcomes that most generalist investors are not equipped to evaluate.

Damien Bretegnier points to a structure in which large corporations invest as LPs into funds of funds, deploying into specialist deep tech vehicles with the ticket sizes and holding-period tolerance that semiconductor hardware requires. Cloudberry's launch this year of a dedicated semiconductor venture fund is one early instance of that infrastructure beginning to take shape [44].



CHAPTER 05

PRACTICAL LEVERS FOR THE EUROPEAN SEMICONDUCTOR ECOSYSTEM

- → The structural gaps of the European semiconductor ecosystem can be addressed through instruments it already has, such as co-development, corporate venture capital, and pre-competitive consortia, but these are usually implemented after commercial validation, when terms are already set by others.

- → Co-development at TRL 3-6 would provide startups the industrial reference needed to unlock growth capital, while CVC extended to TRL 1-5 would enable corporates to act as both strategic early adopter and an anchor customer, and pre-competitive consortia would allow companies to share infrastructure costs without compromising their competitive position.

- → Europe still has the opportunity to establish a competitive position in areas such as integrated photonics, quantum hardware, and wide-bandgap semiconductors. Unusually for this industry, where advantages typically entrench over decades, these contests remain open, although each is closing at a different pace, and rewards whoever moves first.

The structural gaps identified are addressable through instruments already present within Europe's corporate ecosystem: co-development agreements, corporate venture capital, pre-competitive consortia, and early procurement commitments.

These instruments tend to be deployed too late in a startup's development cycle to generate the industrial validation that growth-stage capital requires, especially in the case of deep tech when company often lack a repeatable sales process [40]. The opportunity is in applying them earlier and with greater deliberateness.

The impact assessment accompanying the Chips Act 2.0 proposal, published in June 2026 by the European Commission, advances a "strategic sovereignty" framework that for the first time places demand-side measures alongside supply-side investment [5]. Lab-to-fab accelerators and innovation procurement are additions to the policy agenda, and a meaningful correction to a predecessor that directed capital primarily toward the manufacturing segment where Europe's structural disadvantage is greatest.

But the proposal is several years from full implementation, and public instruments can scaffold early commercial activity without substituting for the private anchor customer willing to co-develop and commit to procurement before the market has validated a technology.

That anchor customer already exists in latent form. Europe's IDMs and industrial groups are concentrated in the same markets European semiconductor startups are building for: power electronics, precision sensing, photonic interconnects, and quantum-adjacent instrumentation. What's missing is activation earlier in the development cycle than European corporates have so far applied.

THREE INSTRUMENTS, APPLIED EARLIER

Co-development and early procurement

Co-development agreements at TRL 3–6 generate two things simultaneously: the startup gains the industrial reference that unlocks growth capital, and the corporate gains early access to technology its own R&D cannot reach at the same speed.

The mechanism works best where there is genuine technological distance between the parties, which makes integrated photonics, quantum hardware, and wide-bandgap materials the natural domains for this approach.

The STMicroelectronics-DIAMFAB agreement is the clearest European example: DIAMFAB (Deep Tech Pioneer – 2019), a France-based manufacturer of diamond semiconductors for high-power electronics, secured the industrial reference it needed to advance to its next funding round [45]..

At the same time, STMicroelectronics gained early access to a diamond semiconductor platform beyond its existing roadmap. The ASML-imec partnership applies the same logic to shared research infrastructure.

ASML installed its full product portfolio, including its most advanced EUV systems, at imec's pilot line in Leuven, giving the broader ecosystem access to sub-2nm R&D capability while gaining a testbed for its own tools in return [46].

IonQ's acquisition of Oxford Ionics shows the cost of engaging too late, where a European quantum company was coaxed away by the US because the relevant European actors had not built the prior relationship [42].

In contrast, Merck's acquisition of Unity SC (France) shows what earlier engagement can produce [47].

The Chips Act 2.0's proposed lab-to-fab accelerators formalise this pathway at policy level, yet the corporate advantage will be in building those relationships before that infrastructure arrives [5].

CVC extended to early TRL

European IDMs have active CVC programmes but often engage after commercial validation has occurred, at the point where the startup is already competitive and the terms are set by others.

The opportunity is to extend that engagement to TRL 1–5, where 78% of European semiconductor startups are concentrated, and where a corporate investor can simultaneously function as a strategic sensing mechanism and an early anchor customer.

That combination is what Intel Capital and Qualcomm Ventures have used to track technology shifts years ahead of their product roadmaps [48]. European IDMs have that same capability and the same incentive.

Bosch Ventures' backing of iPronics at Series A is representative of current European practice where engagement occurs once a technology reaches validation, and in domains adjacent to existing product lines [49].

The funding gap this creates is structural: European investors provide on average 84% of early-stage capital but that share drops to around 50% at scaleup [50]. Earlier CVC engagement closes that gap by generating the industrial credibility a startup needs before it arrives at Series B without it.

Hardware development cycles in photonics, quantum, and wide-bandgap semiconductors typically run seven to ten years, longer than standard fund structures are designed for [51].

Secondary transactions, where a corporate investor partially exits its position to another investor rather than waiting for a full exit, provide a mechanism for maintaining strategic exposure and board presence through extended development cycles without tying up the full balance sheet [52].

The Scaleup Europe Fund is designed to lead the growth rounds that CVC alone cannot fill; the corporate role is to have built the industrial validation that makes a company viable for that capital when it arrives [41,53].

Pre-competitive consortia

Some infrastructure benefits every participant in an ecosystem equally but is difficult for any single company to justify building alone, such as shared design toolkits, testing facilities, or packaging standards, for example.

Pre-competitive consortia solve this by distributing the cost across companies with a shared interest in the capability existing, without any participant conceding competitive position.

ESMC in Dresden demonstrates the model at the production level with TSMC, Bosch, Infineon, and NXP, jointly funding shared FinFET manufacturing capacity because the strategic rationale outweighs the competitive sensitivity [16].

Sematech applied the same principle to R&D, distributing process development costs across US semiconductor companies and government to restore American competitiveness against Japan in the 1980s.

The NSTC extends it to broader ecosystem infrastructure, spanning R&D, workforce development, and technology transfer [54]. Europe is already applying this logic further upstream.

The SPINS pilot line, launched in April 2026 and coordinated by imec alongside Infineon, Siltronic, and a consortium of 25 research and industry partners, pools shared cleanroom infrastructure for semiconductor spin-qubit fabrication [55].

The EU Chips Design Platform represents an earlier instance at the design level [56]. Both examples demonstrate how Europe's fragmented ecosystem, spread across multiple countries and institutions, can be organised into a structural advantage.

The domains where shared infrastructure would have the greatest compounding effect are those where Europe's scientific leadership is deepest and where commercial infrastructure does not yet exist, such as in photonic integrated circuit PDKs or quantum hardware characterisation facilities.

The consortium that establishes these sets the standard the rest of the ecosystem builds around. That is a durable competitive position, and it is available to whoever moves first.

Table 1 brings the three instruments together against existing European precedents and the specific opportunity each presents.

THE WINDOW OF OPPORTUNITY

The competitive positions in integrated photonics, quantum hardware, and wide-bandgap semiconductors are not yet set. These are the domains where Europe's research base is deepest, where the global market structure is still forming, and where early corporate engagement can still be formative rather than reactive.

That combination is unusual in the semiconductor industry, where structural advantages tend to entrench over decades and late entry is prohibitively expensive.

Each domain has a window of opportunity that will close at a different pace: photonics is approaching commercial deployment and the positions forming now will be difficult to displace, wide-bandgap materials are moving toward industrial qualification, and quantum hardware remains further from market but is consequently less competitively contested.

Even so, Europe has what it needs in research institutions producing commercially credible companies, IDMs with the procurement power and CVC infrastructure to function as anchor customers, as well as a policy environment moving toward demand-side activation for the first time. The foundations are in place.

What determines whether they become industrial positions, or are acquired before they do, is how deliberately European corporates choose to engage in the window that remains open.

INSTRUMENT	PROBLEM ADDRESSED			BENEFITS	KEY ACTORS	EXAMPLES
	Capital -constrained at the growth stage	Absence of anchor customers	Exit patterns where value flows to overseas acquirers			
CO -DEVELOPMENT AND EARLY PROCUREMENT	✓	✓		Translate lab research into commercial products Share infrastructure costs Provide the industrial reference needed for growth Create revenue visibility for early-stage startups in soverei-gnty-sensitive markets Position corporations as natural acquirers before external buyers set valuations	Corporations Public institutions (Procurement bodies, EU agencies)	STMicroelectronics - DIAMFAB ASML-imec EIC Pre-Commercial Procurement European Defence Fund
CORPORATE VENTURE CAPITAL (INVESTMENT, M&A, JV)		✓	✓	Build strategic positions in adjacent technology domains Generate foresight into transitions relevant to core customer sectors Encourage European-centric M&A, prevent value leakage to non-EU acquirers Acquire strategic capabilities and talent through M&A before they are commoditised or captured by external buyers	Corporations	Bosch Ventures / iPronics Infineon Ventures NXP Ventures
PRE -COMPETITIVE CONSORTIA	✓			Distribute the cost of capital-intensive shared infrastructure Provide manufactu-ring and design capacity certainty for startups across the value chain Establish shared standards to shape what the ecosystem builds around	Corporations Research Institutes Startups	ESMC SPINS quantum pilot EU Chips Design Platform

Table 1. Three instruments and their application to the ecosystem



ABOUT HELLO TOMORROW

Hello Tomorrow is a global deep tech organisation working at the intersection of science, industry, and investment to accelerate the translation of breakthrough technologies into commercial impact. Our work spans three connected capabilities: ecosystem intelligence, innovation strategy, and programme execution.

Over the past decade, Hello Tomorrow has built one of the world's largest deep tech ecosystems, with its annual Summit and Investor Day convening startups, corporates, and investors, as well as a network of ecosystem partners, including research centres, incubators, accelerators, and tech transfer offices across Europe, Asia, and Americas.

With over 20,000 deep tech solutions scouted across eleven editions of the Hello Tomorrow Challenge, the company maintains one of the world's most comprehensive startup databases across semiconductors, quantum hardware, advanced materials, medical devices, biotechnology, renewable energy, and beyond.

Our consulting practice helps corporates make the right deep tech bets and turn them into measurable business impact. We work with strategy, R&D, innovation, and business leaders to identify where breakthrough technologies can create competitive advantage, prioritise the opportunities that matter most, and translate them into actionable investment and innovation decisions.

Beyond strategic recommendations, we help organisations access the right technologies, startups, and partners from our global ecosystem, while supporting the design and execution of collaborations that deliver tangible outcomes.

Whether through venture clienting, strategic partnerships, technology validation, or pilot deployment, our focus is not simply to identify opportunities, but to ensure they generate measurable value and long-term competitive advantage.

METHODOLOGY

The analysis in CHAPTER 3 draws on a database of approximately 1,550 semiconductor startups featuring funding, development stage, and investor data, compiled from Dealroom and Crunchbase, and supplemented by Hello Tomorrow's own scouting network. As Dealroom and Crunchbase provide only financial data and company descriptions, each company was reviewed and tagged by the Hello Tomorrow analyst team against three frameworks:

- Position in the semiconductor value chain
- Primary technology domain
- Target market

The geographic aspect of the analysis focuses on Europe, the United States, and China, as they account for approximately 87% of the startups in the database. Other geographies with major semiconductor industry presence, notably Japan, South Korea, Taiwan, and Singapore, hold strengths that sit primarily in established incumbents rather than VC-backed startups, and are consequently less centre-stage in this analysis.

A few limitations are worth stating. Coverage in both Dealroom and Crunchbase skews toward funded, formally registered companies, meaning very early-stage or grant-only ventures are likely underrepresented, particularly in Europe where public funding often precedes any equity round. However, this limitation has been partially mitigated by Hello Tomorrow's broader-reaching database.

TRL were assigned by analysts based on available information rather than self-reported by companies, introducing a degree of subjectivity at the margins. Where relevant, TRL is cross-referenced with funding data to assess whether technical maturity translates into capital velocity.

Other frameworks such as Commercial Readiness Level (CRL) and Manufacturing Readiness Level (MRL) would round this picture out further, but available information relating to these aspects is limited.

The database is large enough to be structurally representative and the patterns it reveals are consistent with publicly available information. As stated in the chapter, some geographies, particularly China, may be underrepresented where the details of state-funded ventures are not publicly disclosed.

Otherwise, companies absent from the analysis fall into one of three categories: those operating in stealth, those that did not provide sufficient credible information to be considered relevant, and those without a defined semiconductor-native direction, meaning startups that develop explicitly for the semiconductor ecosystem rather than adjacent technology markets.

Finally, tracking the country of origin of each funding organisation was too granular to include systematically in this analysis. Although this is important in understanding the ecosystem, considering ticket size and structure as a measure of opportunity suffices for the purpose of the conclusions made in this report.

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